

# SYNC separator IC with AFC

## BA7062F

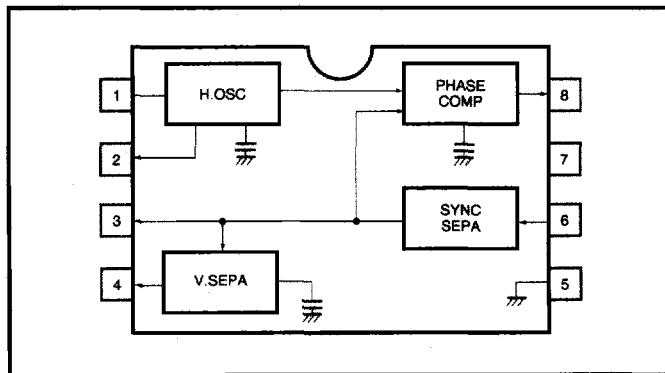
The BA7062F separates the synchronization signals from a video signal and outputs the horizontal and vertical synchronization signals ( $H_b$  and  $V_b$ ), and the composite synchronization signal (Sync-out). The  $H_b$  and  $V_b$  pulse widths are different.

● Applications  
TV and VCR

● Features

- 1) Built-in AFC circuit.
- 2) Low power dissipation (approx. 21mW).
- 3) Low external parts count.
- 4) SOP 8-pin package.
- 5) Horizontal free-run frequency does not require adjustment.

● Block diagram



● Internal circuits

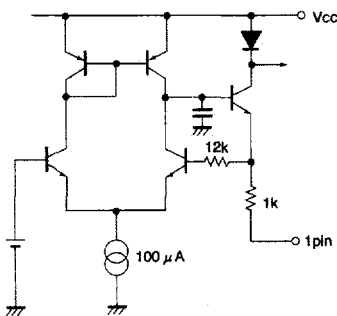


Fig. 1

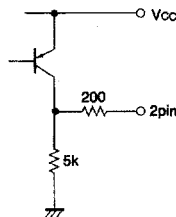


Fig. 2

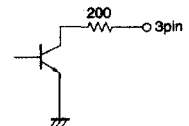


Fig. 3

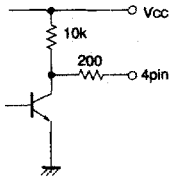


Fig. 4

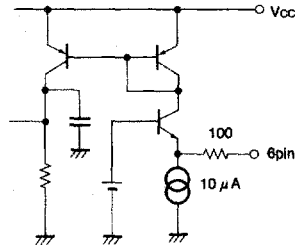


Fig. 5

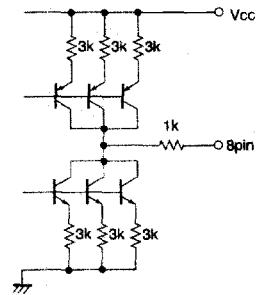


Fig. 6

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>CC Max.</sub>	8.0	V
Power dissipation	P <sub>d</sub>	350 *	mW
Operating temperature	T <sub>opr</sub>	-20~75	°C
Storage temperature	T <sub>stg</sub>	-55~125	°C

\* When mounted on a 50mm × 50mm PCB, reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

● Pin descriptions

Pin No.	Function
1	Horizontal oscillator resistor
2	H <sub>D</sub> output
3	SYNC output (open collector)
4	V <sub>D</sub> output
5	GND
6	Video input
7	Power supply
8	Phase comparator output

● Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V <sub>cc</sub>	4.5	—	5.5	V

●Electrical characteristics (Unless otherwise specified :Ta=25°C and Vcc=5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Quiescent current	I <sub>Q</sub>	2.0	4.1	6.2	mA	Pin 3 open	Fig.7
Minimum SYNC separation level	V <sub>syn-Min.</sub>	—	0.08	0.15	V <sub>P-P</sub>	Pin 6 terminated with 75Ω resistor	
Pulse voltage, Low	V <sub>P-L</sub>	—	0.1	0.3	V	2, 4 pin	
Pulse voltage, High	V <sub>P-H</sub>	4.7	4.9	—	V	2, 4 pin	
(Horizontal) free-running frequency	f <sub>H-O</sub>	13.9	15.7	17.5	kHz	No input signal, I <sub>1</sub> = open	
Capture range	Δf <sub>CAP</sub>	±2.1	±2.9	—	kHz		
Lock-in phase	T <sub>HPH</sub>	-1.0	0	+1.0	μs	2pin ↓ -6pin ↓	
H <sub>D</sub> pulse width	T <sub>HD</sub>	10.5	11.5	12.5	μs	2pin ↓	
V <sub>D</sub> pulse width	T <sub>VD</sub>	200	260	320	μs	4pin ↓	

○Not designed for radiation resistance.

●Measurement circuit

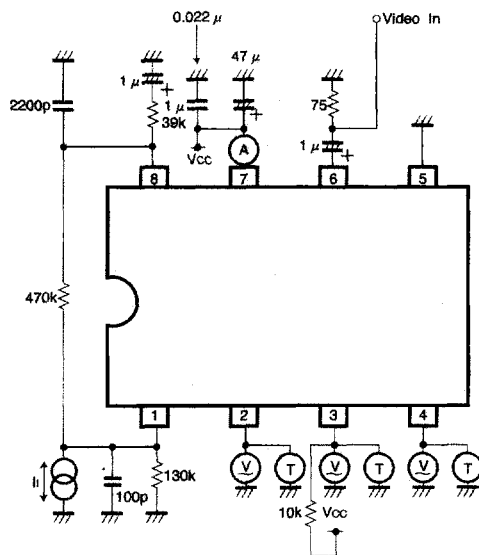


Fig. 7

● Electrical characteristic curves

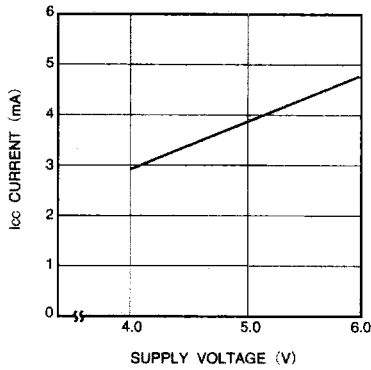


Fig. 8 Quiescent current vs. supply voltage

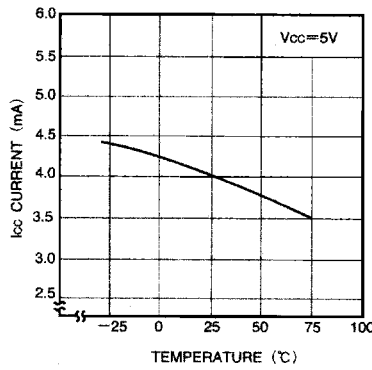


Fig. 9 Quiescent current vs. temperature

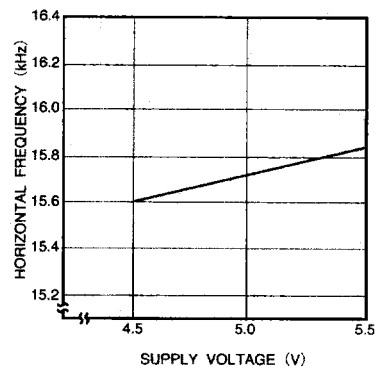


Fig. 10 Horizontal free-running frequency vs. supply voltage

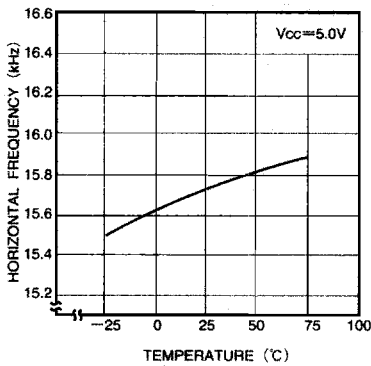


Fig. 11 Horizontal free-running frequency vs. temperature

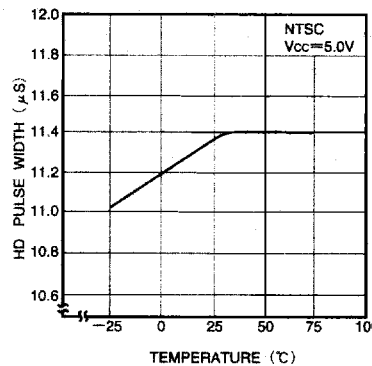


Fig. 12 H<sub>d</sub> pulse width vs. temperature

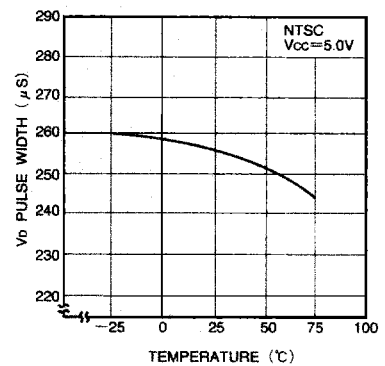


Fig. 13 V<sub>d</sub> pulse width vs. temperature

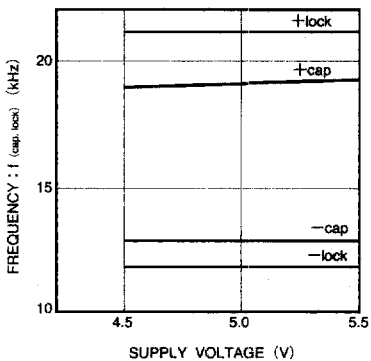


Fig. 14 Capture range/lock range vs. supply voltage

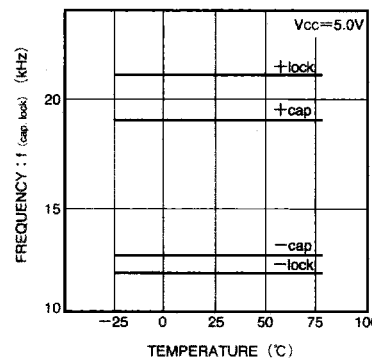


Fig. 15 Capture range/lock range vs. temperature

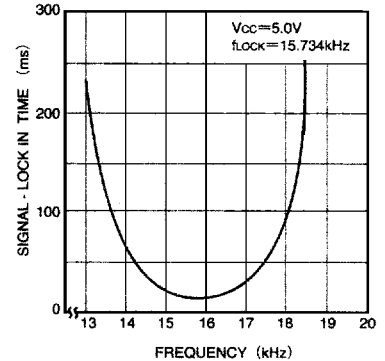


Fig. 16 Time from no signal to pull in

SYNC separator ICs

Multimedia video

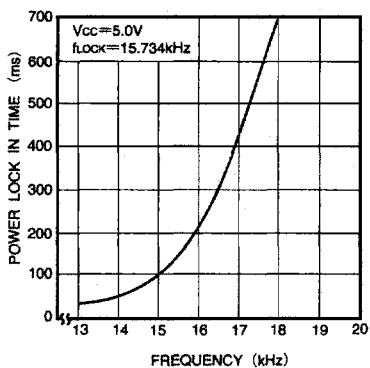


Fig. 17 Time from power on to pull in

#### ● Circuit operation

##### (1) Synchronization separation circuit

Detects the charging current to an externally-connected capacitor, and performs synchronization separation.

##### (2) Horizontal oscillation circuit

When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor R<sub>1</sub>.

$$f_{H-O} = \frac{2.05E6}{R_1} \text{ [kHz]}$$

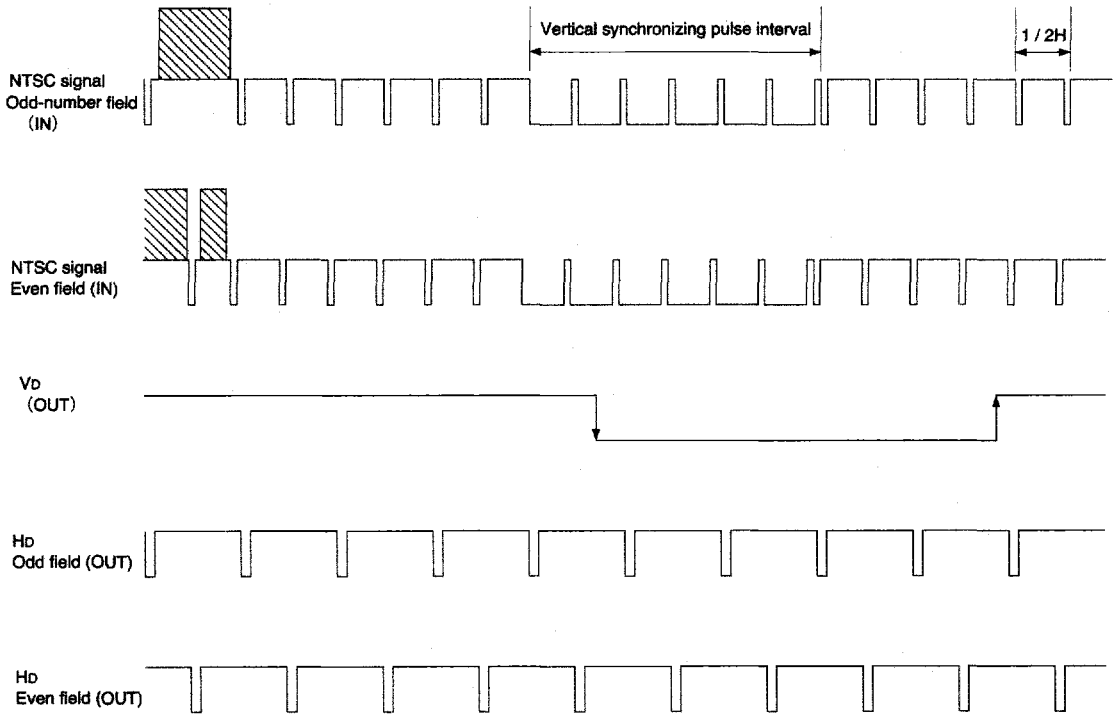
##### (3) Vertical synchronization separation circuit

When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

#### ● Operation notes

- Make the ground line as thick as possible.
- Keep power supply noise to a minimum.

●  $V_{IN}$ ,  $H_D$ , and  $V_D$  timing charts



1. The rise and fall positions for  $V_D$  are basically the same for both odd and even fields.
2.  $H_D$  shifts by  $1/2H$  during the odd and even field interval.

## ●Application example

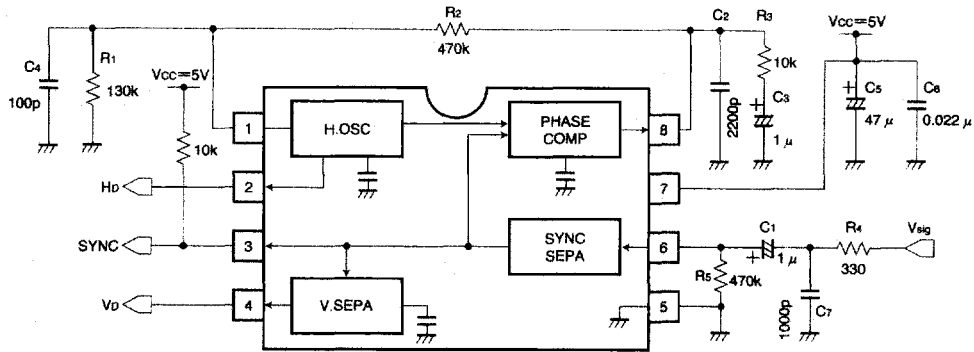


Fig. 18

- When SYNC SEPA output only is used. HD and VD unused.

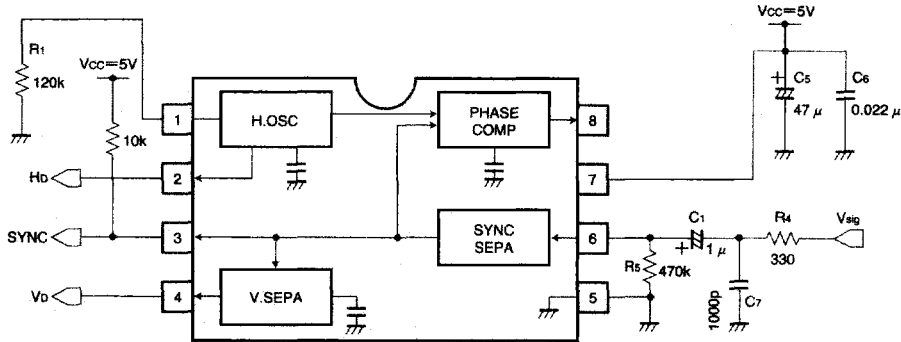


Fig. 19

1. Connect pin 1 to GND via a 120k  $\Omega$  (approx.) resistor. Leave pins 2, 4 and 8 open.
2. SYNC output polarity (pin 3) is positive.
3. The delay time for rising edge of the SYNC output (pin 3) with respect to the falling edge of Sync for the Vsig input signal (pin 6) is 850ns (reference value).
4. The delay time for falling edge of the SYNC output (pin 3) with respect to the rising edge of Sync for the Vsig input signal (pin 6) is 450ns (reference value).

## ●External components

Resistor R<sub>1</sub> should have a tolerance of  $\pm 2\%$ , and a temperature coefficient of 100ppm or lower.

● External dimensions (Units: mm)

