800MHz Band LNA GaAs MMIC

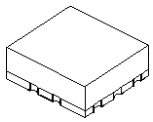
■ GENERAL DESCRIPTION

The NJG1127HB6 is a LNA IC designed for 800MHz band CDMA2000 cellular phone, and this LNA IC suited for 760MHz V2X applications.

The NJG1127 has LNA bypasses function, and high gain mode or low gain mode can be selected. High IIP3 and a low noise are achieved at the High gain mode. And low current consumption can be achieved at the low gain mode because LNA enters the state of the standby.

A small and thin package of USB8-B6 is adopted.

■PACKAGE OUTLINE



NJG1127HB6

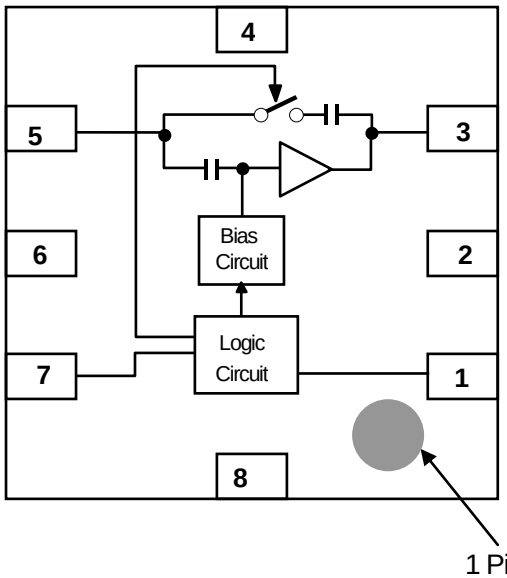
■ FEATURES

●Operation voltage	2.65V～4.0V.	
●High Gain	15.0dB typ.	@f=880MHz, V_{DD}=2.8V
	16.0dB typ.	@f=760MHz, V_{DD}=3.3V
●Low noise figure	1.4dB typ.	@f=880MHz, V_{DD}=2.8V
	1.2dB typ.	@f=760MHz, V_{DD}=3.3V
●High Input IP3	+11.0dBm typ.	@f=880MHz, V_{DD}=2.8V
	+8.0dBm typ.	@f=760MHz, V_{DD}=3.3V
●Small & thin package	USB8-B6 (Package size: 1.5mm x1.5mm x 0.55mm typ.)	

●RoHS compliant and Halogen Free, MSL1

■ PIN CONFIGURATION

(Top View)



1 Pin INDEX

Pin Connection
1.V_{INV}
2.GND
3.RF OUT
4.GND
5.RF IN
6.GND
7. V_{CTL}
8. GND

Note: Specifications and description listed in this catalog are subject to change without prior notice.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	V_{DD}		5.0	V
Inverter supply voltage	V_{INV}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{in}	V_{DD}=3.3V	+22	dBm
Power dissipation	P_D	on PCB board, Tjmax=150°C	160	mW
Operating temperature	T_{opr}		-40~+105	°C
Storage temperature	T_{stg}		-55~+150	°C

■ **ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)**

(General Conditions: T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		2.65	-	4.0	V
Inverter supply voltage	V_{INV}		2.65	-	4.0	V
Control voltage (High)_1	V_{CTL}(H)_1	V_{DD}=2.8V	1.80	1.85	V_{DD+}0.3	V
Control voltage (High)_2	V_{CTL}(H)_2	V_{DD}=3.3V	1.80	3.3	V_{DD+}0.3	V
Control voltage (Low)	V_{CTL}(L)		0	0	0.3	V
Operating current 1(1) (LNA High Gain Mode)	I_{DD}1(1)	RF OFF V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V	-	10.0	16.0	mA
Operating current 1(2) (LNA Low Gain Mode)	I_{DD}1(2)	RF OFF V_{DD}=V_{INV}=2.8V, V_{CTL}=0V	-	1	5	uA
Operating current 2(1) (LNA High Gain Mode)	I_{DD}_2(1)	RF OFF V_{DD}=V_{INV}=3.3V, V_{CTL}=3.3V	-	13.0	21.0	mA
Operating current 2(2) (LNA Low Gain Mode)	I_{DD}_2(2)	RF OFF V_{DD}=V_{INV}=3.3V, V_{CTL}=0V	-	1	6	µA
Inverter current 1(1) (LNA High Gain Mode)	I_{INV}_1(1)	RF OFF V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V	-	150	240	µA
Inverter current 1(2) (LNA Low Gain Mode)	I_{INV}_1(2)	RF OFF V_{DD}=V_{INV}=2.8V, V_{CTL}=0V	-	15	40	µA
Inverter current 2(1) (LNA High Gain Mode)	I_{INV}_2(1)	RF OFF V_{DD}=V_{INV}=3.3V, V_{CTL}=3.3V	-	170	300	µA
Inverter current 2(2) (LNA Low Gain Mode)	I_{INV}_2(2)	RF OFF V_{DD}=V_{INV}=3.3V, V_{CTL}=0V	-	20	50	µA
Control current_1	I_{CTL}_1	RF OFF, V_{CTL}=1.85V	-	5	15	µA
Control current_2	I_{CTL}_2	RF OFF, V_{CTL}=3.3V	-	40	80	µA

■ **ELECTRICAL CHARACTERISTICS 2 (LNA High Gain Mode 1)**

(General Conditions: V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, f_{RF}=880MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit 1)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain_1(1)	Gain_1(1)		13.5	15.0	17.0	dB
Noise figure_1(1)	NF_1(1)	Exclude PCB & connector losses (IN: 0.04dB)	-	1.4	1.8	dB
1dB gain compression output power_1(1)	P-1dB_1(1)		+4	+9	-	dBm
3rd order Input Intercept Point_1(1)	IIP3_1(1)	f1=f_{RF}, f2=f_{RF}+100kHz, P_{in}=-25dBm	+8	+11	-	dBm
RF IN VSWR_1(1)	$VSWR_i$_1(1)		-	1.5	2.0	
RF OUT VSWR_1(1)	$VSWR_o$_1(1)		-	1.5	2.0	

■ **ELECTRICAL CHARACTERISTICS 3 (LNA Low Gain Mode 1)**

(General Conditions: V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, f_{RF}=880MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit 1)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain_1(2)	Gain_1(2)		-4.0	-2.5	0	dB
Noise figure_1(2)	NF_1(2)	Exclude PCB & connector losses (IN: 0.04dB)	-	2.5	5.0	dB
1dB gain compression output power_1(2)	P-1dB_1(2)		+1	+8	-	dBm
3rd order Input Intercept Point_1(2)	IIP3_1(2)	f1=f_{RF}, f2=f_{RF}+100kHz, P_{in}=-12dBm	+15	+19	-	dBm
RF IN VSWR_1(2)	$VSWR_i$_1(2)		-	2.3	2.7	
RF OUT VSWR_1(2)	$VSWR_o$_1(2)		-	1.8	2.1	

■ **EL ECTRICAL CHARACTERISTICS 4 (LNA High Gain Mode 2)**

(General Conditions: V_{DD}=V_{INV}=V_{CTL}=3.3V, f_{RF}=760MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit 2)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain _2(1)	Gain_2(1)		13.5	16.0	18.5	dB
Noise figure _2(1)	NF_2(1)	Exclude PCB & connector losses (IN: 0.04dB)	-	1.2	1.8	dB
1dB gain compression output power__2(1)	P-1dB_2(1)		+4.0	+11.0	-	dBm
Output Power	P_{out}	P_{in}=-40~+22dBm	-	-	+15.5	dBm
3rd order Input Intercept Point _2(1)	IIP3_2(1)	f1=f_{RF}, f2=f_{RF}+100kHz, P_{in}=-25dBm	+6.0	+8.0	-	dBm
Gain Settling time_(1)	Ts_(1)	Low gain to high gain mode to be within 1dB of the final gain	-	0.5	2.5	μs
RF IN VSWR _2(1)	$VSWR_i$_2(1)		-	1.6	2.0	
RF OUT VSWR_ 2(1)	$VSWR_o$_2(1)		-	1.3	2.0	

■ **ELECTRICAL CHARACTERISTICS 5 (LNA Low Gain Mode 2)**

(General Conditions: V_{DD}=V_{INV}=3.3V, V_{CTL}=0V, f_{RF}=760MHz, T_a=+25°C, Z_s=Z_l=50Ω, with application circuit 2)

項目	記号	条件	最小	標準	最大	単位
Small signal gain_2(2)	Gain_2(2)		-4.5	-2.5	0	dB
Noise figure_2(2)	NF_2(2)	Exclude PCB & connector losses (IN: 0.04dB)	-	2.5	5.5	dB
1dB gain compression output power _2(2)	P-1dB_2(2)		+1.0	+7.5	-	dBm
3rd order Input Intercept Point_2(2)	IIP3_2(2)	f1=f_{RF}, f2=f_{RF}+100kHz, P_{in}=-12dBm	+15.0	+21.0	-	dBm
Gain Settling time_(2)	Ts_(2)	High gain to low gain mode to be within 1dB of the final gain	-	1.0	2.5	μs
RF IN VSWR_2(2)	$VSWR_i$_2(2)		-	2.1	3.0	
RF OUT VSWR_2(2)	$VSWR_o$_2(2)		-	1.6	2.1	

■TERMINAL INFOMATION

No.	SYMBOL	DESCRIPTION
1	VINV	Supply voltage terminal for internal logic circuit (inverter). Please place a bypass capacitor between this and GND for avoiding RF noise from outside.
2	GND	Ground terminal.
3	RFOUT	RF signal comes out from this terminal, and goes through an external matching circuit connected to this. Inductor L4 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA. Capacitor C2 as shown in the application circuit is a bypass capacitor.
4	GND	Ground terminal.
5	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. A DC blocking capacitor is not required.
6	GND	Ground terminal.
7	VCTL	Control port. A logic control signal is required to select High or Low gain mode of LNA. This terminal is set to more than +1.8V of logical high level for High gain mode of LNA, and set to 0~+0.3V of logical low level for Low gain mode.
8	GND	Ground terminal.

CAUTION

1) Ground terminal (No.2, 4, 6, 8) should be connected to the ground plane as close as possible for excellent RF performance, because distance to GND makes parasitic inductance.

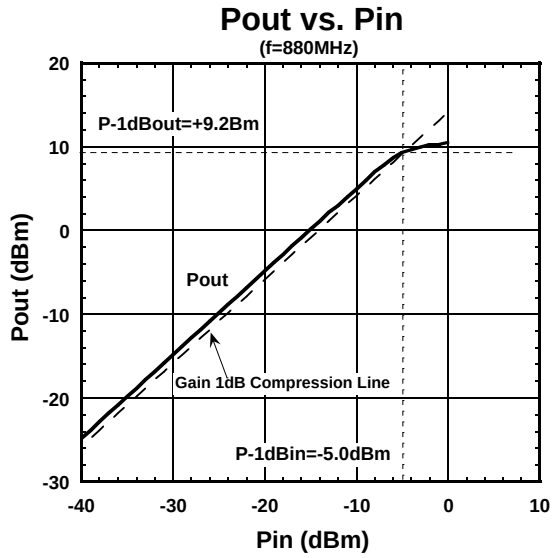
■ TRUTH TABLE

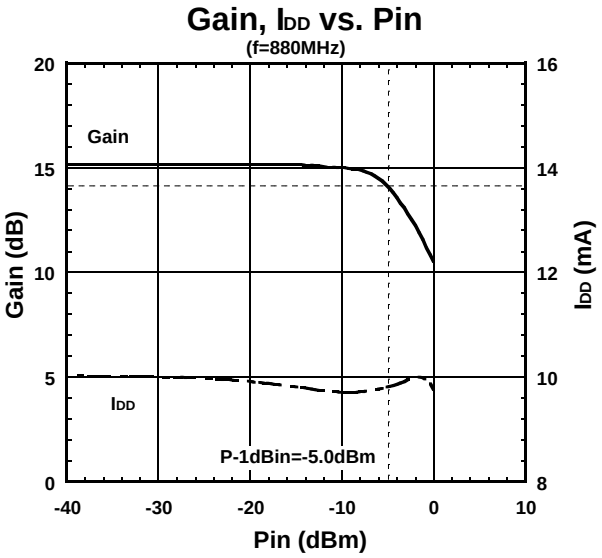
"H"=V_{CTL}(H), "L"=V_{CTL}(L)

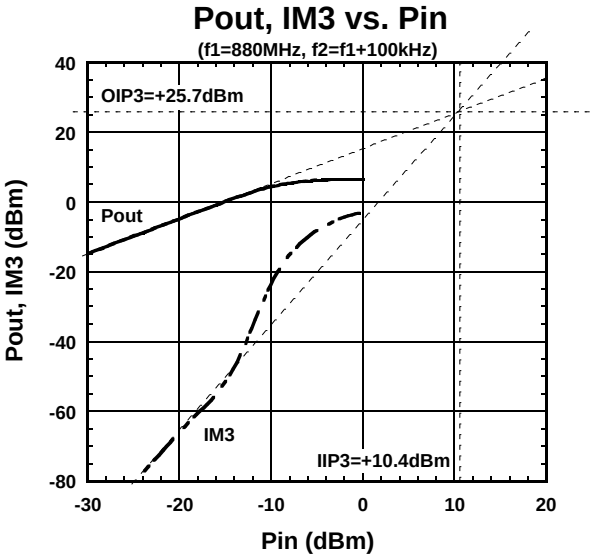
V_{CTL}	Gain Mode	LNA
L	Low	bypass
H	High	pass

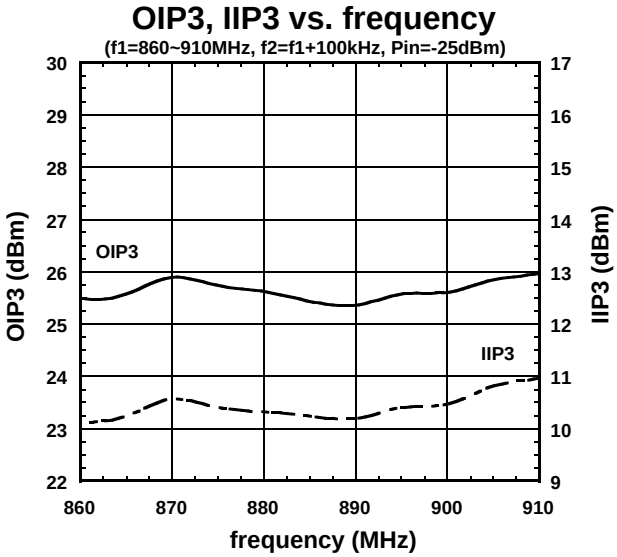
■ ELECTRICAL CHARACTERIS TICS (LNA High Gain Mode 1)

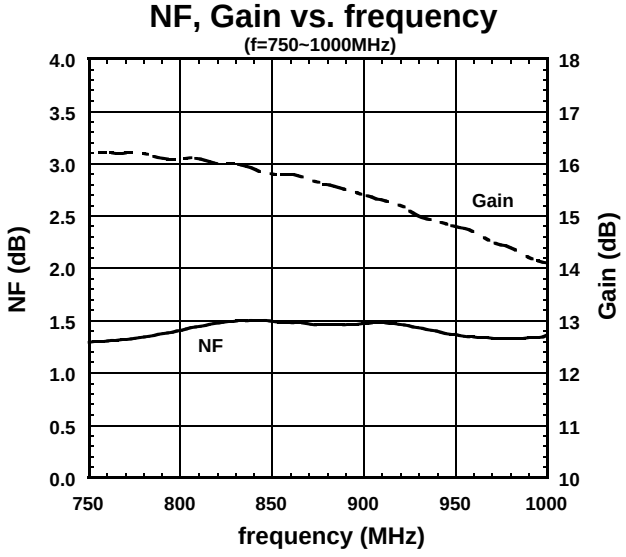
(General Conditions: Ta=+25°C, f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω, with application circuit 1)







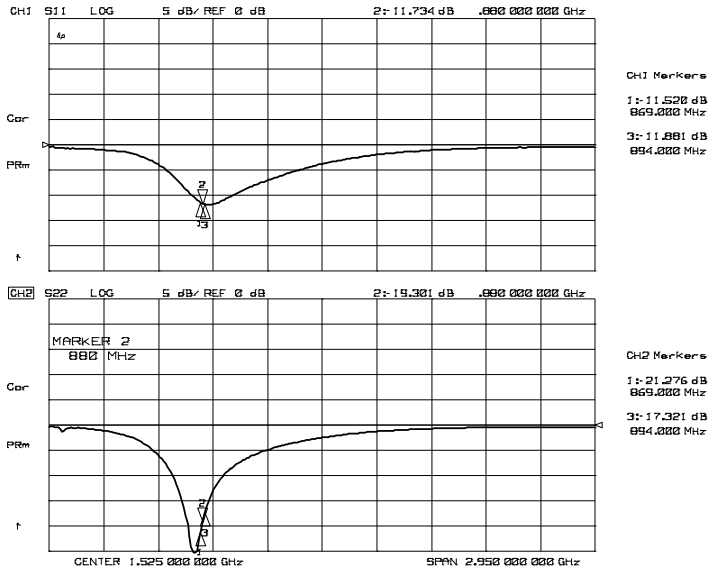




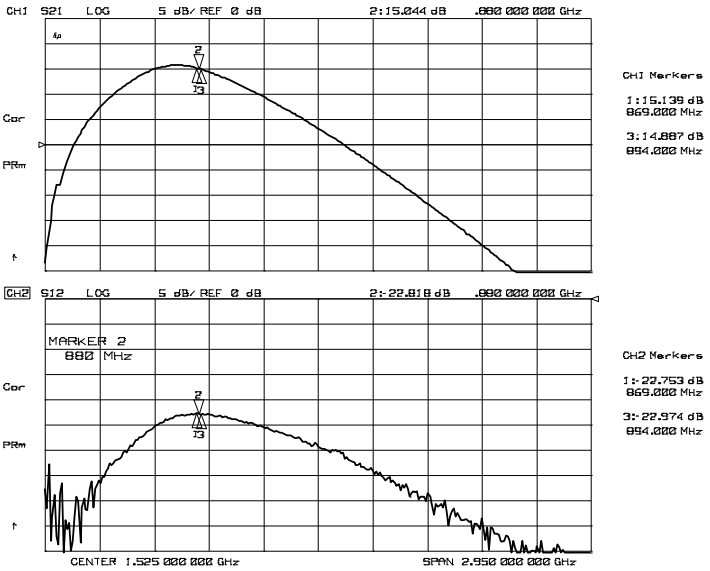
■ ELECTRICAL CHARACTERISTICS (LNA High Gain Mode 1)

(General Conditions:

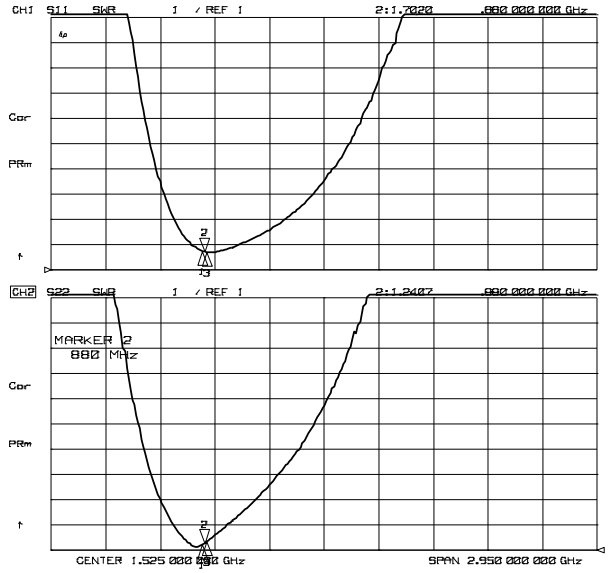
Ta=+25°C, f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω, with application circuit 1)



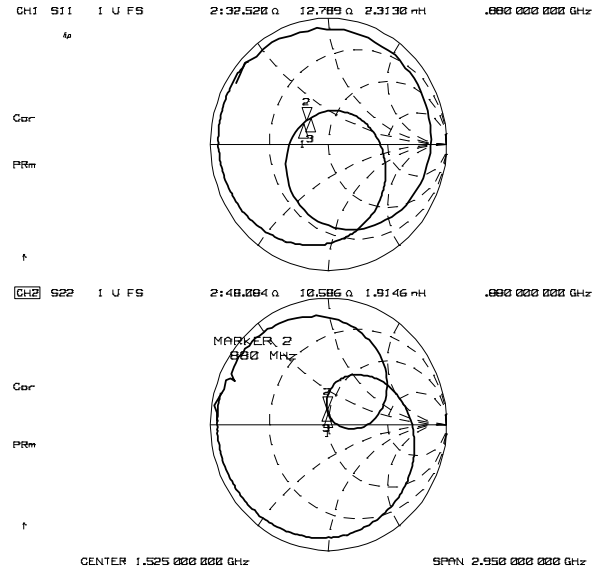
S11, S22



S21, S12



VSWR



Zin, Zout

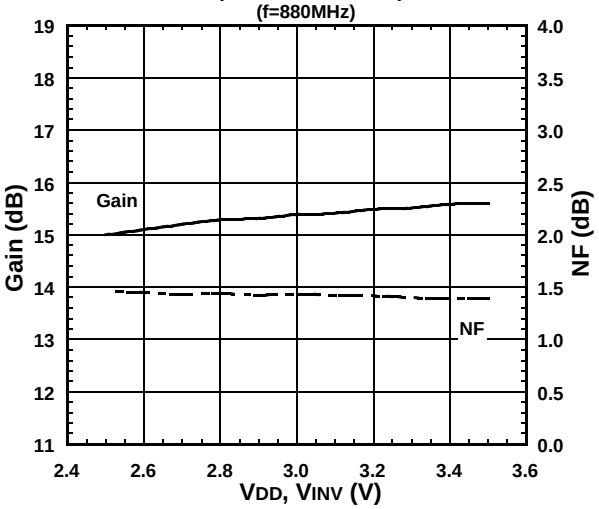
■ ELECTRICAL CHARACTERISTICS (LNA High Gain Mode 1)

(General Conditions:

Ta=+25°C, f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω, with application circuit 1)

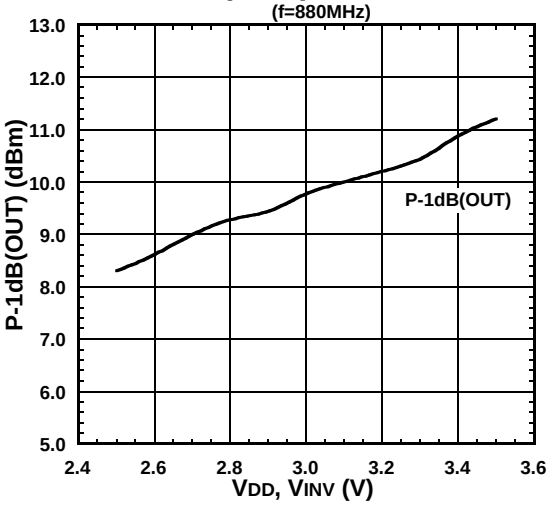
Gain, NF vs. VDD, VINV

(f=880MHz)



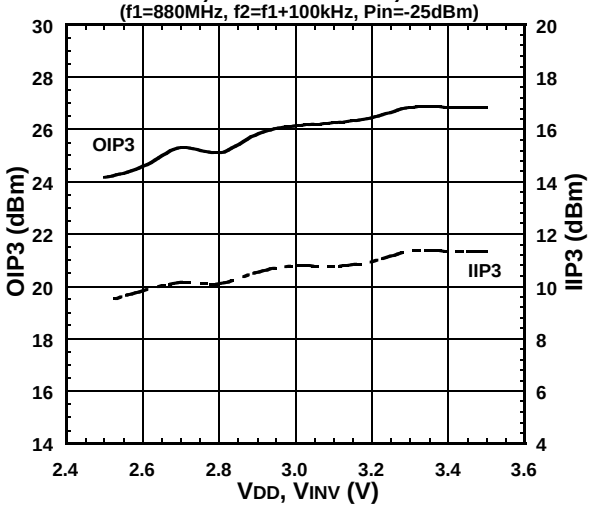
P-1dB(OUT) vs. VDD, VINV

(f=880MHz)



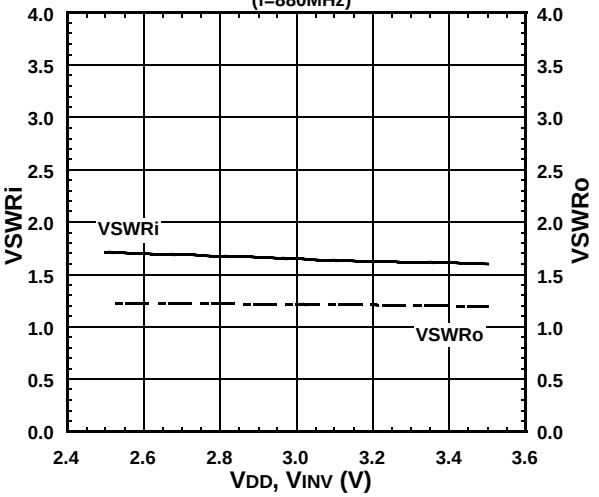
OIP3, IIP3 vs. VDD, VINV

(f1=880MHz, f2=f1+100kHz, Pin=-25dBm)



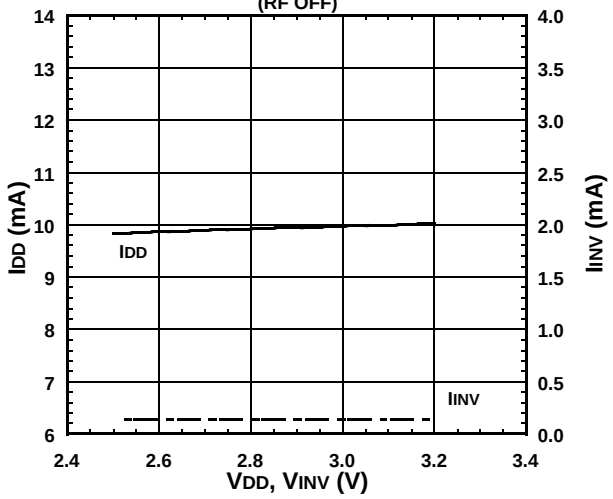
VSWRi, VSWRo vs. VDD, VINV

(f=880MHz)



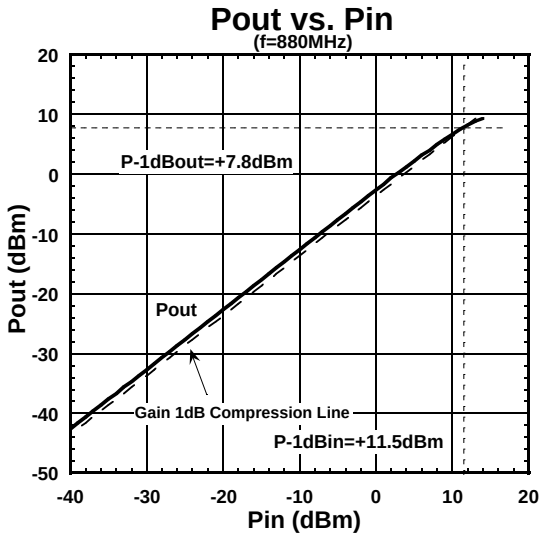
IDD, IINV vs. VDD, VINV

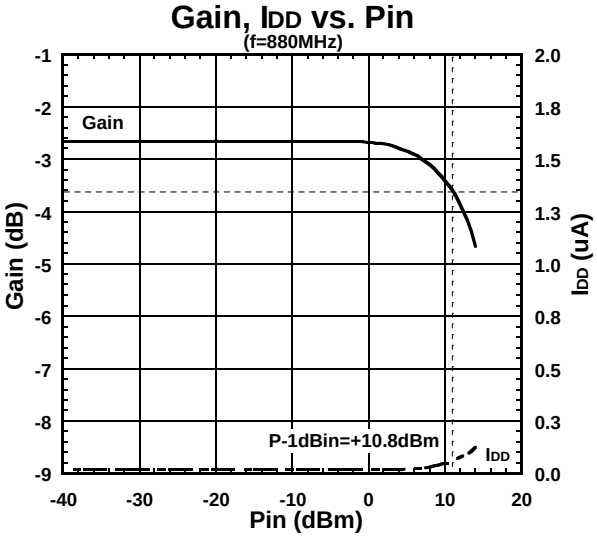
(RF OFF)

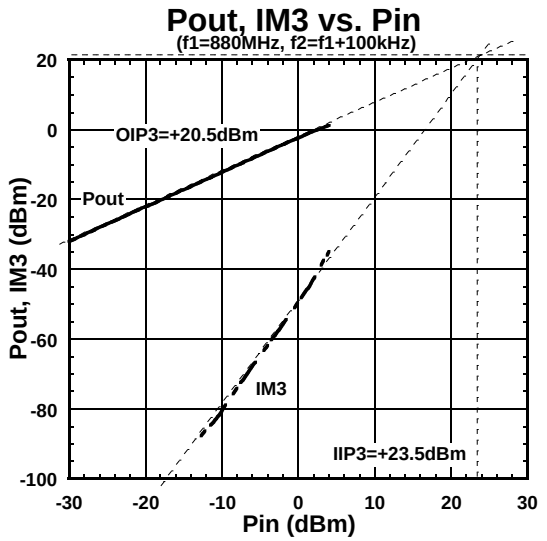


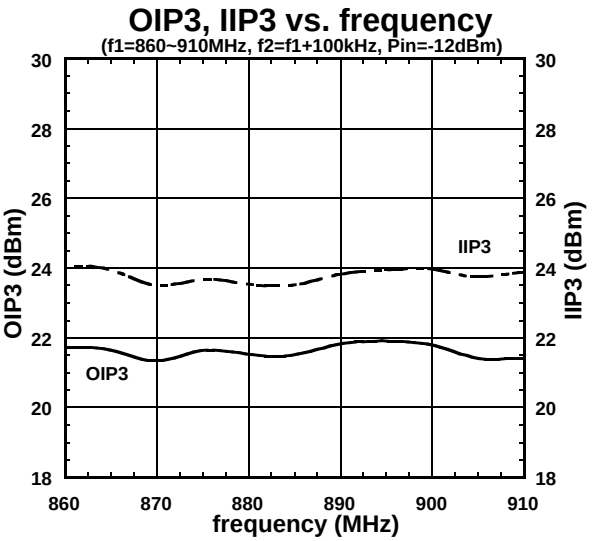
■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 1)

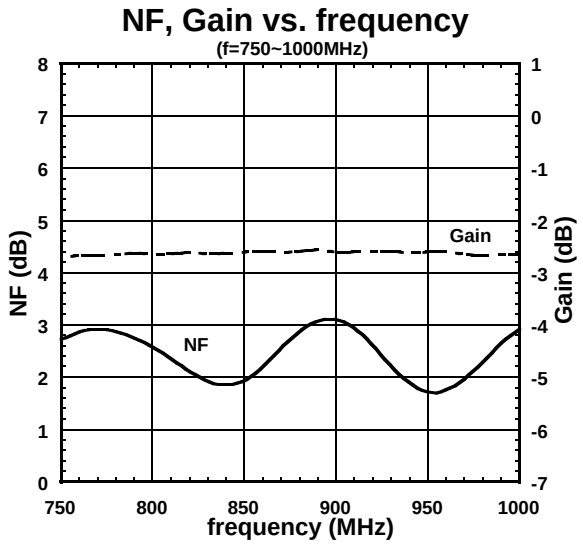
(General Conditions: Ta=+25°C, f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 1)





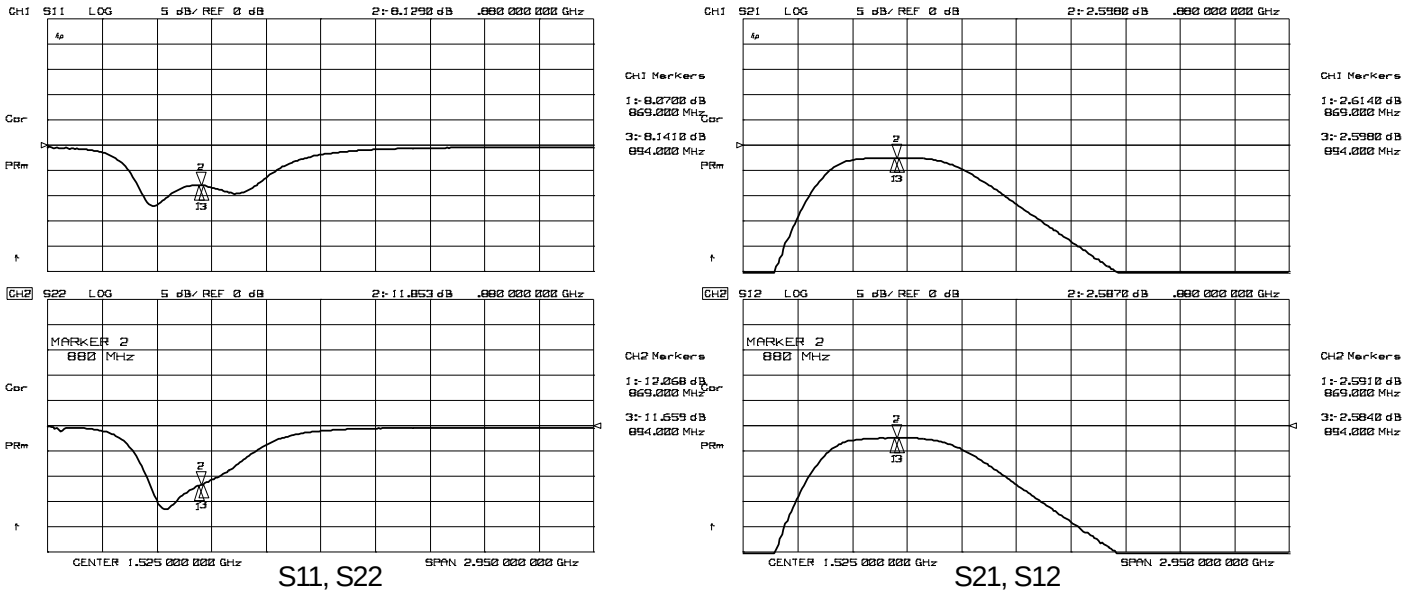




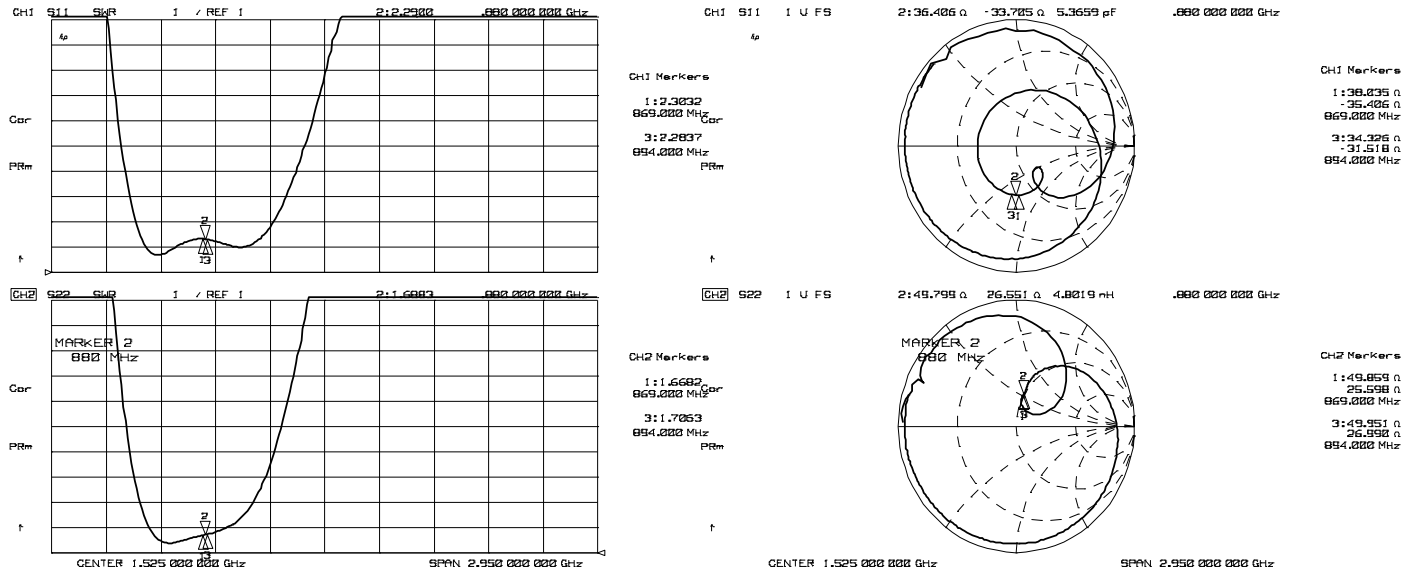


■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 1)

(General Conditions: Ta=+25°C, f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 1)



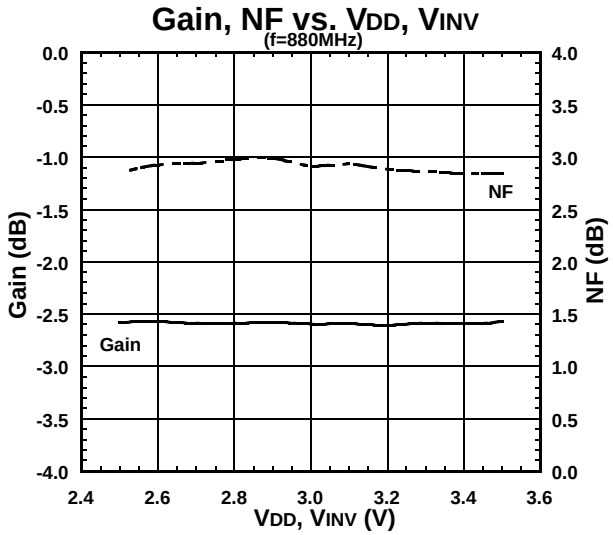
S11, S22 S21, S12

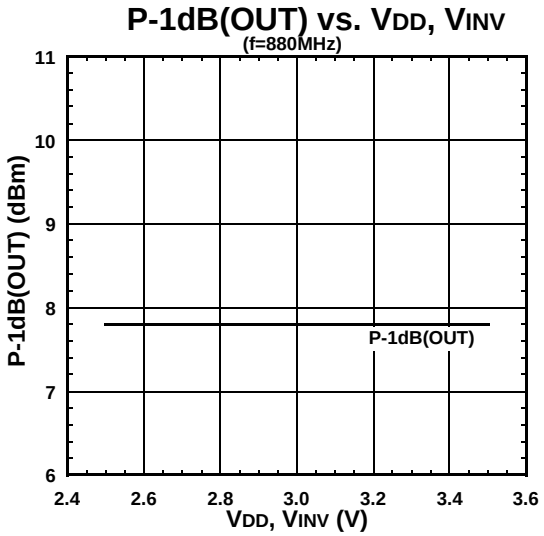


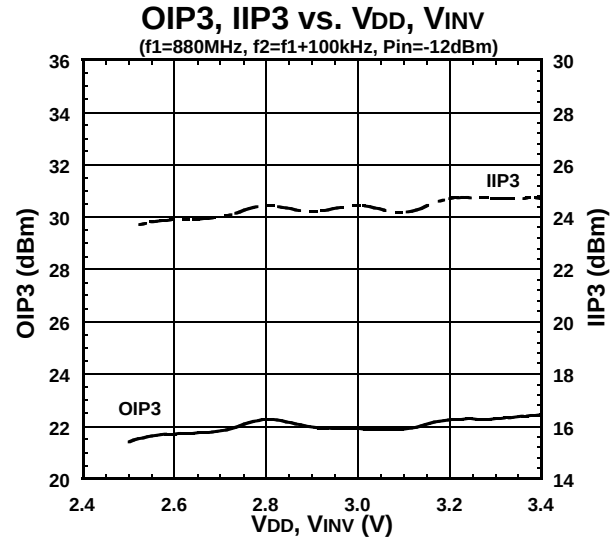
VSWR Zin, Zout

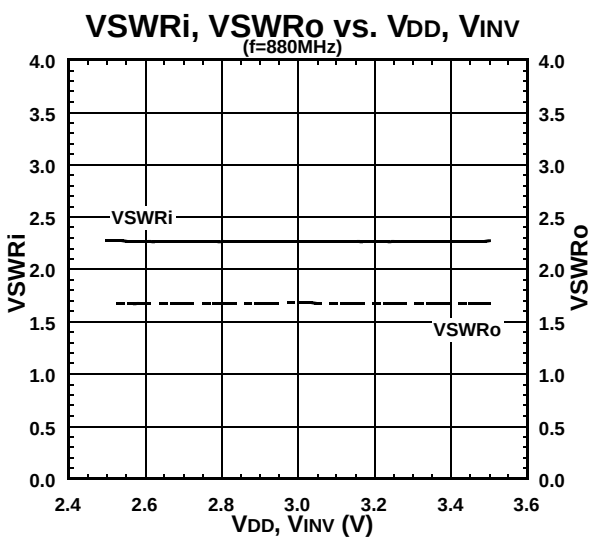
■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 1)

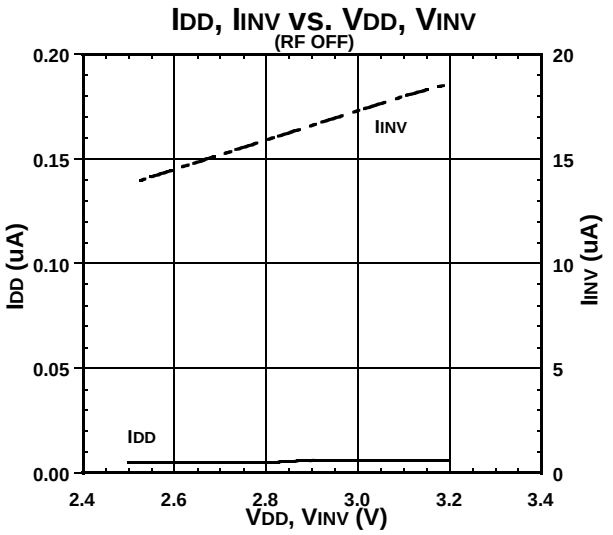
(General Conditions: Ta=+25°C, f_{RF} =880MHz, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 1)







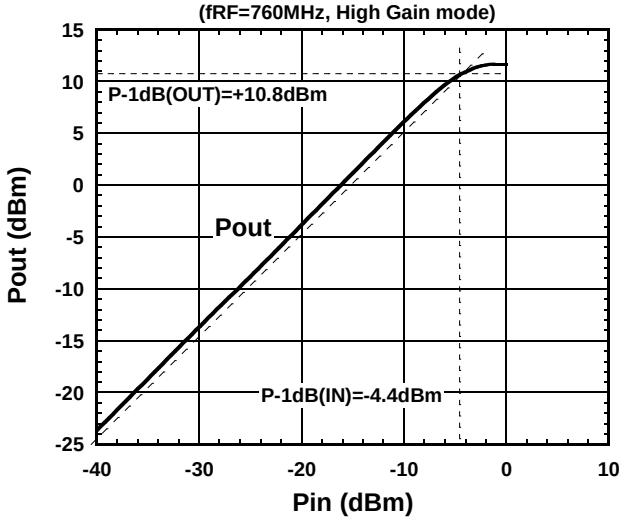




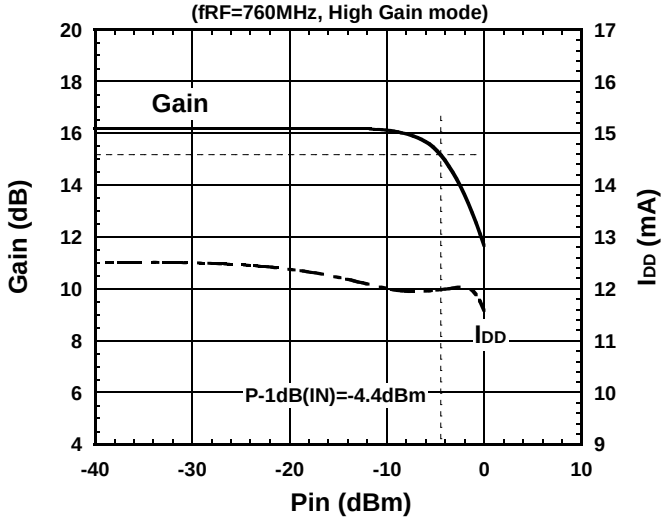
■ ELECTRICAL CHARACTERISTICS (LNA High Gain Mode 2)

(General Conditions: T_a=+25°C, f_{RF}=760MHz, V_{DD}=V_{INV}=V_{CTL}=3.3V, Zs=Zl=50Ω, with application circuit 2)

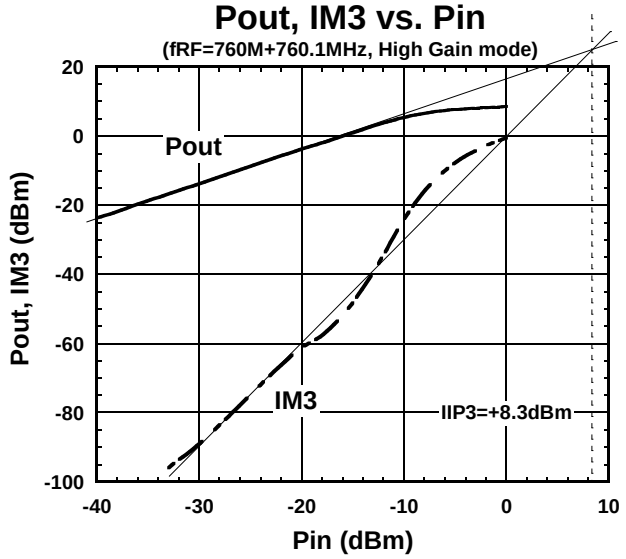
Pout vs. Pin



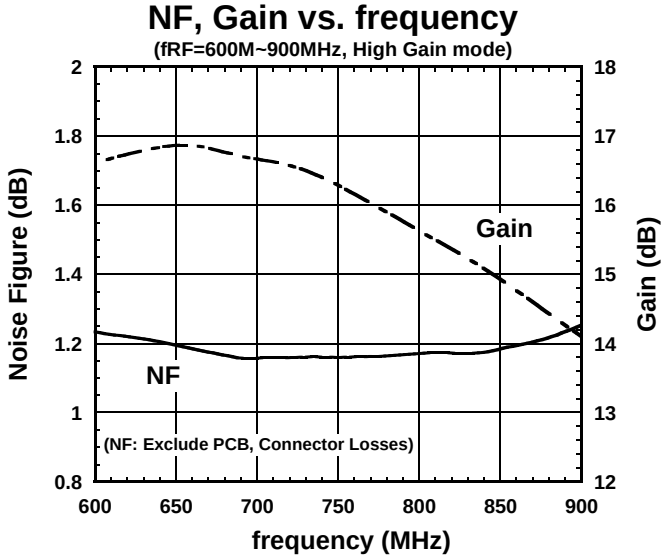
Gain, IDD vs. Pin



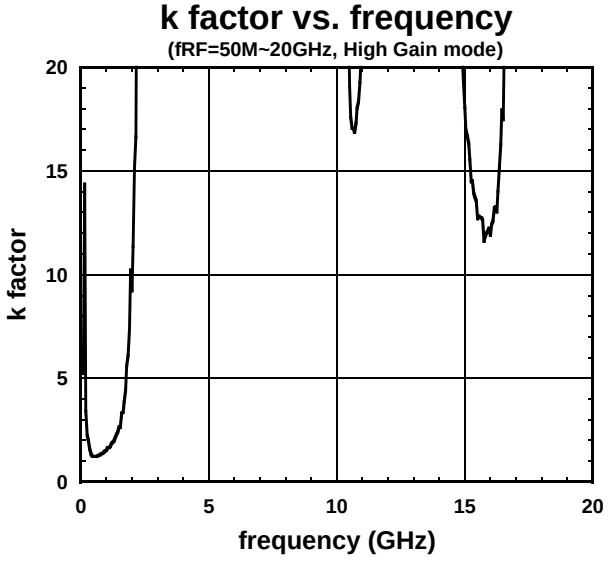
Pout, IM3 vs. Pin



NF, Gain vs. frequency

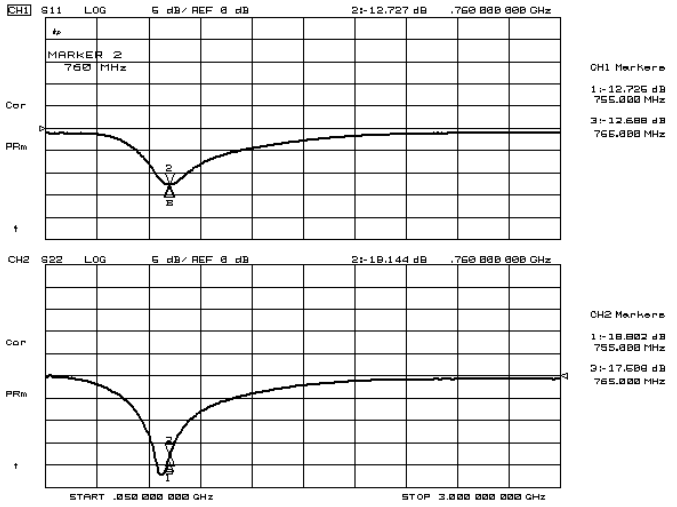


k factor vs. frequency

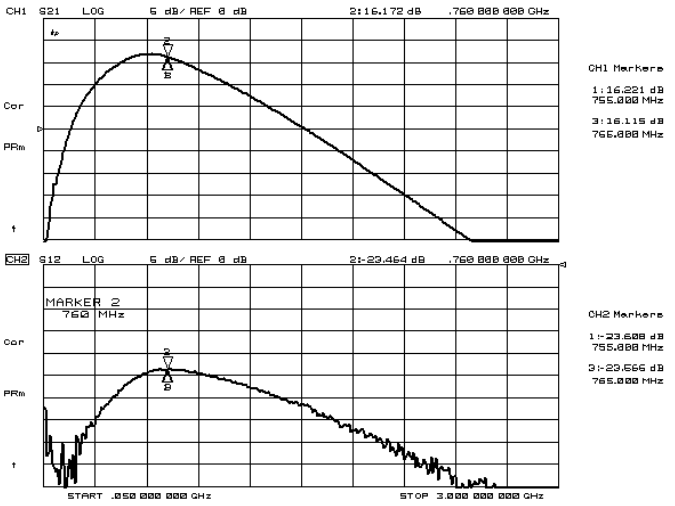


■ ELECTRICAL CHARACTERISTICS (LNA High Gain Mode 2)

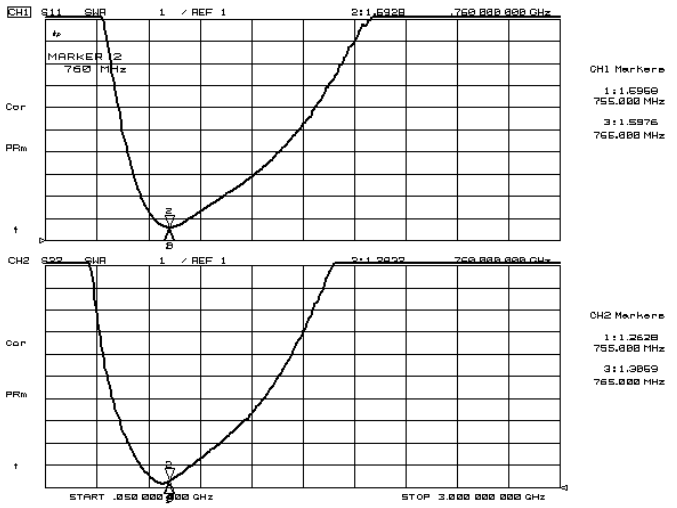
(General Conditions: T_a=+25°C, f_{RF} =760MHz, V_{DD}=V_{INV}=V_{CTL}=3.3V, Zs=Zl=50Ω, with application circuit 2)



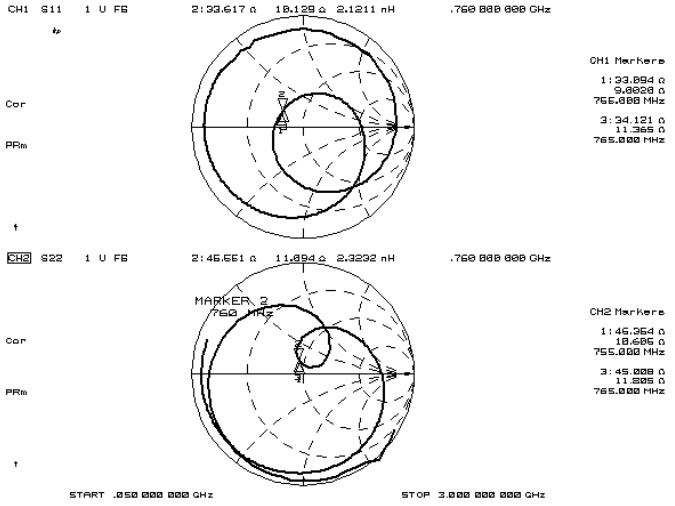
S11, S22



S21, S12



VSWR



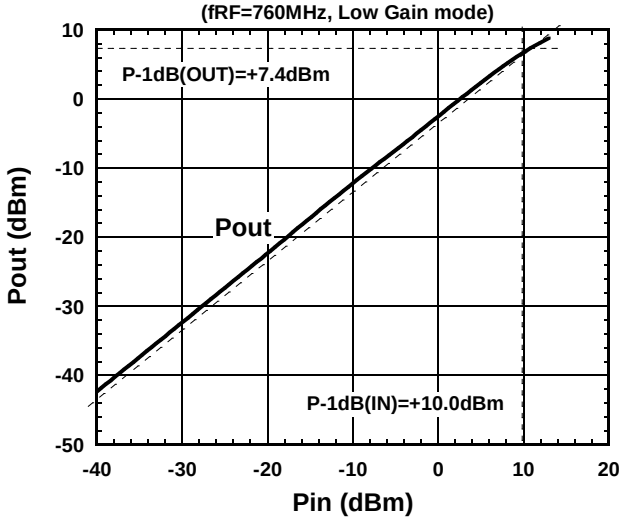
Zin, Zout

■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 2)

(General Conditions: T_a=+25°C , f_{RF} =760MHz, V_{DD}=V_{INV}=3.3V, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 2)

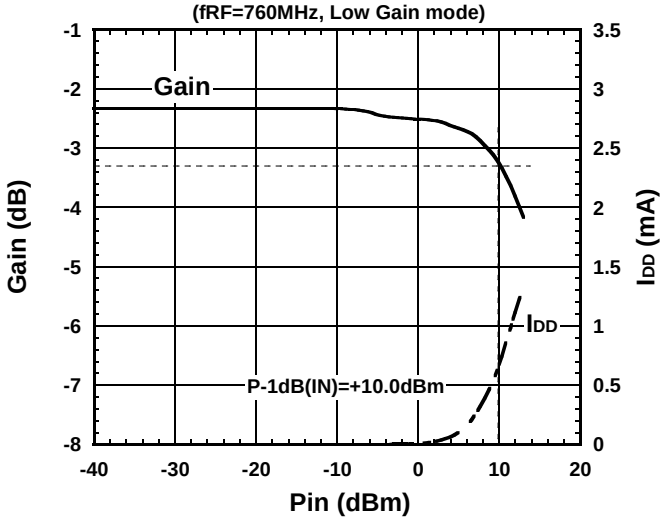
Pout vs. Pin

(fRF=760MHz, Low Gain mode)



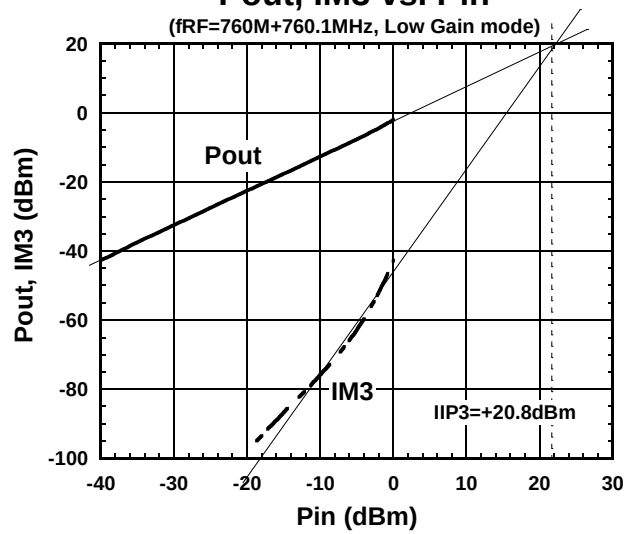
Gain, IDD vs. Pin

(fRF=760MHz, Low Gain mode)



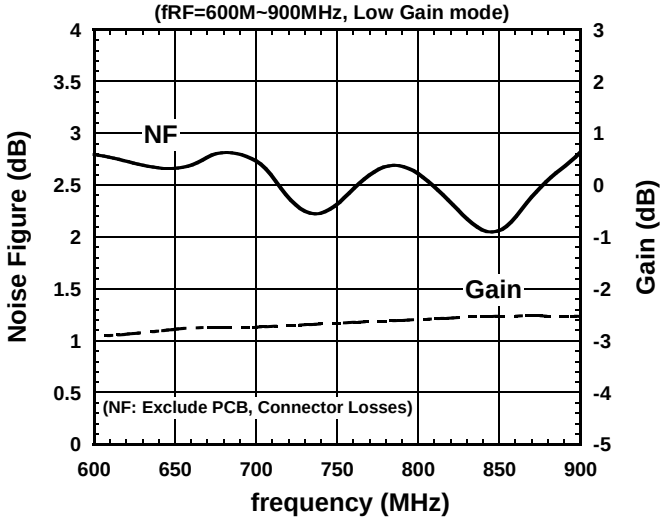
Pout, IM3 vs. Pin

(fRF=760M+760.1MHz, Low Gain mode)



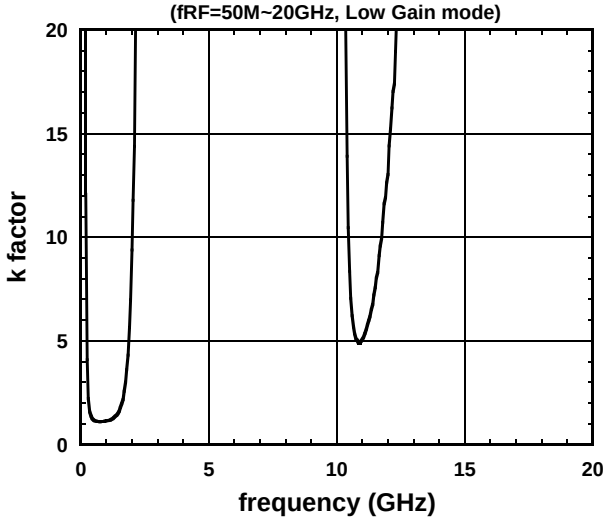
NF, Gain vs. frequency

(fRF=600M~900MHz, Low Gain mode)



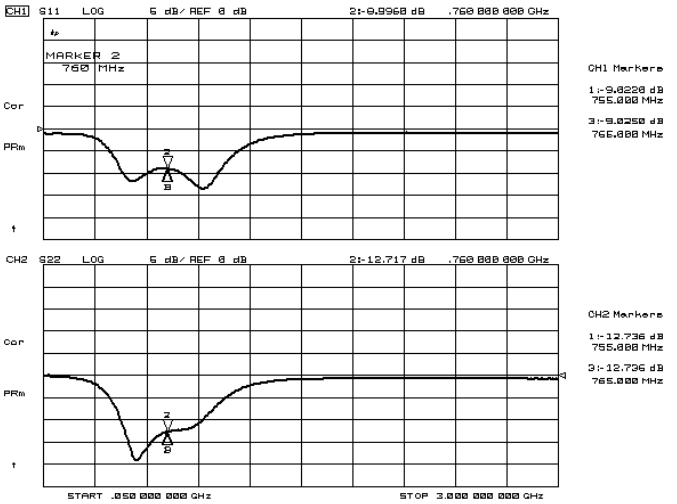
k factor vs. frequency

(fRF=50M~20GHz, Low Gain mode)

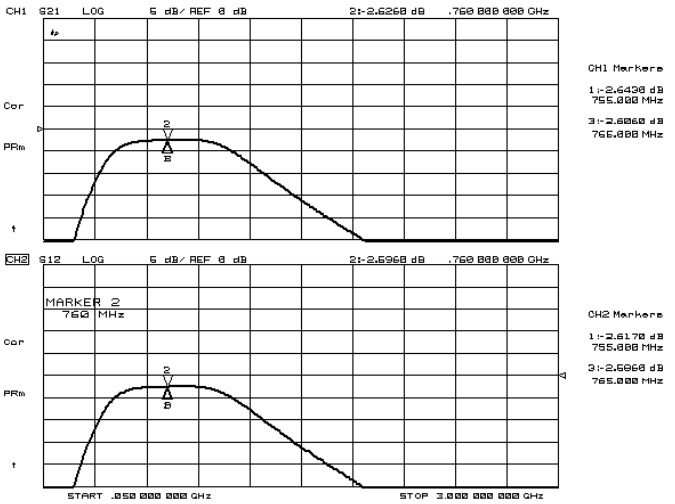


■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 2)

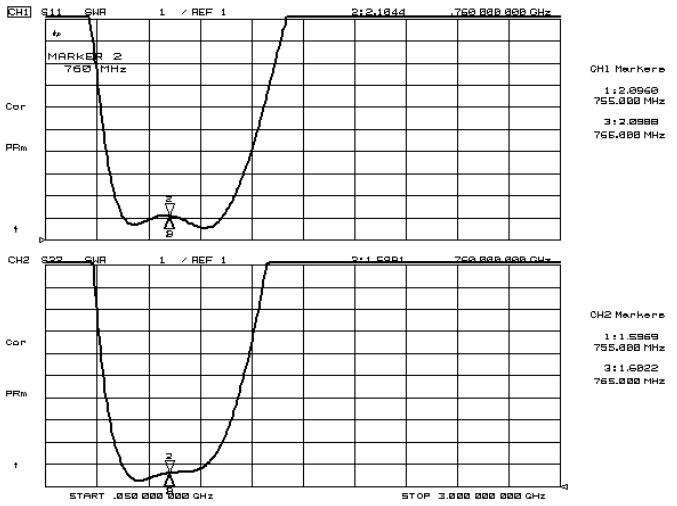
(General Conditions: T_a=+25°C, f_{RF} =760MHz, V_{DD}=V_{INV}=3.3V, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 2)



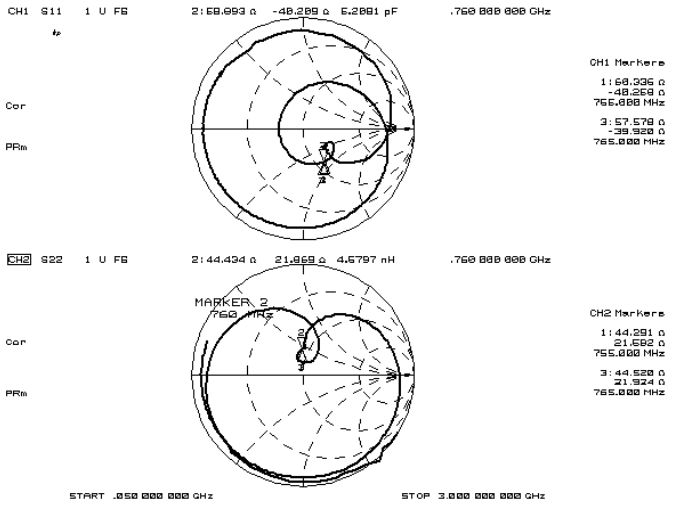
S11, S22



S21, S12



VSWR



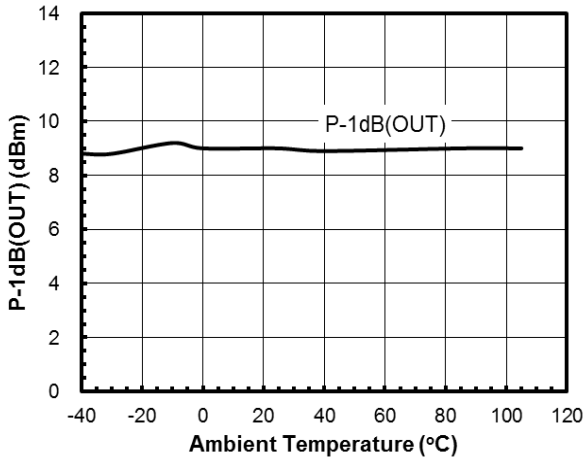
Zin, Zout

■ ELECTRICAL CHARACTERISTICS (LNA High Gain Mode 1)

(General Conditions: f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω, with application circuit 1)

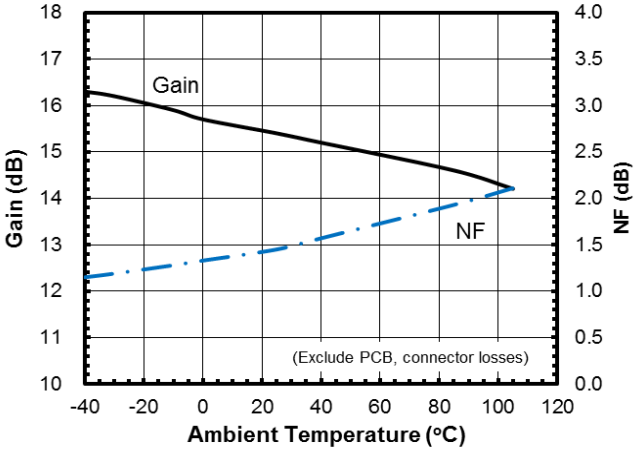
P-1dB(OUT) vs. Ambient Temperature

(f=880MHz)



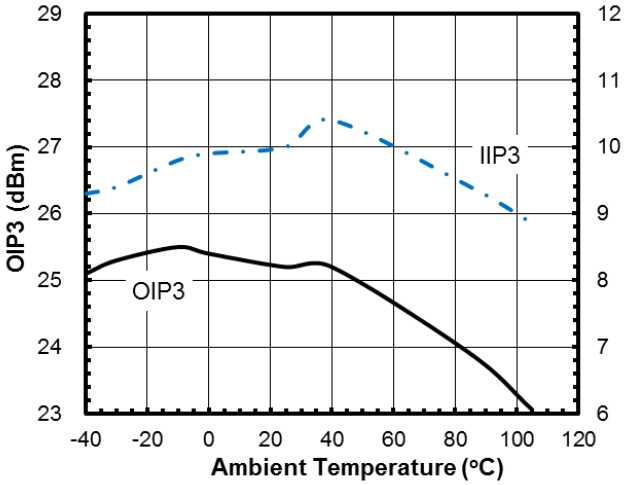
Gain, NF vs. Ambient Temperature

(f=880MHz)



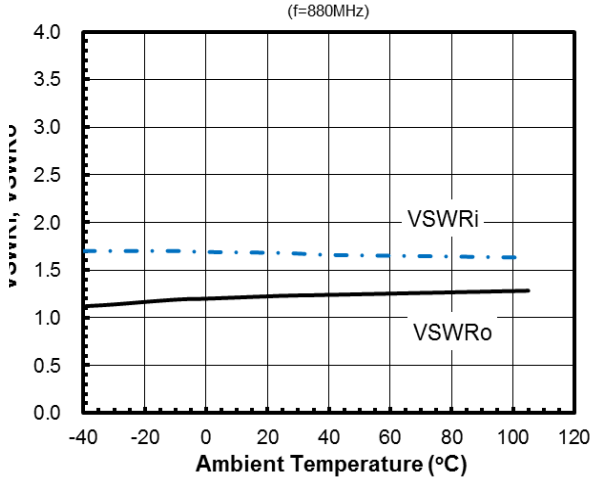
OIP3, IIP3 vs. Ambient Temperature

(f1=880MHz,f2=f1+100kHz, Pin=-25dBm)



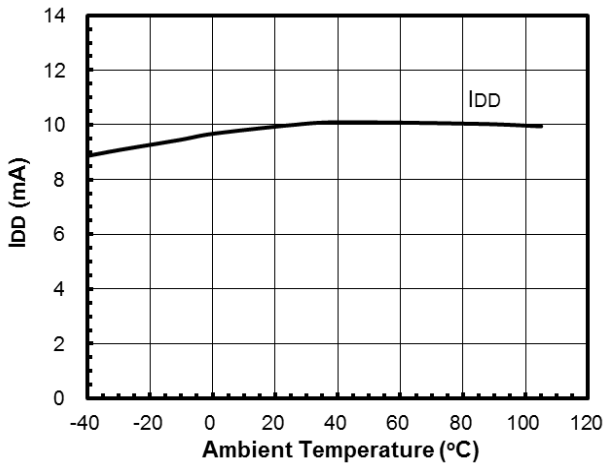
VSWRi, VSWRo vs. Ambient Temperature

(f=880MHz)



IDD vs. Ambient Temperature

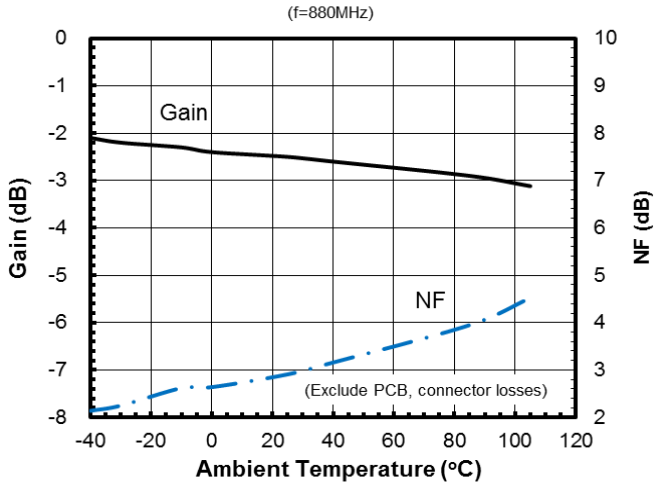
(RF OFF)



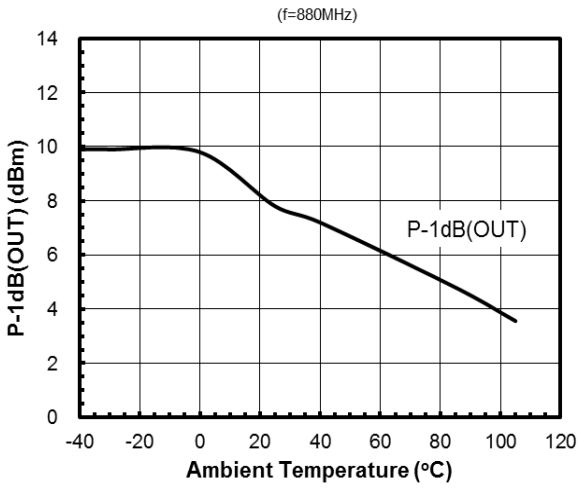
■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 1)

(General Conditions: f_{RF} =880MHz, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 1)

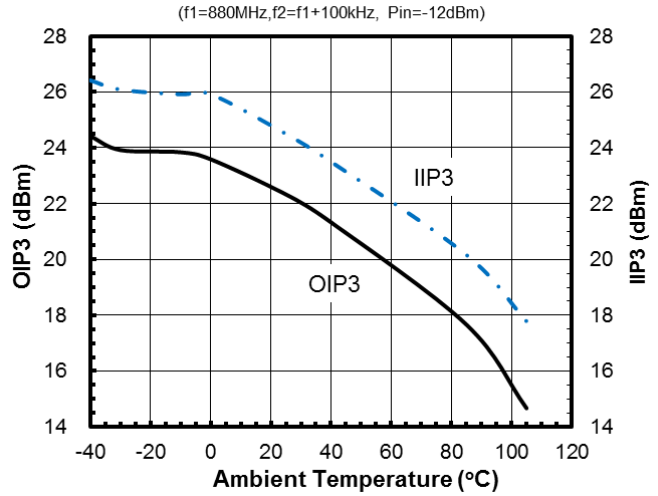
Gain, NF vs. Ambient Temperature



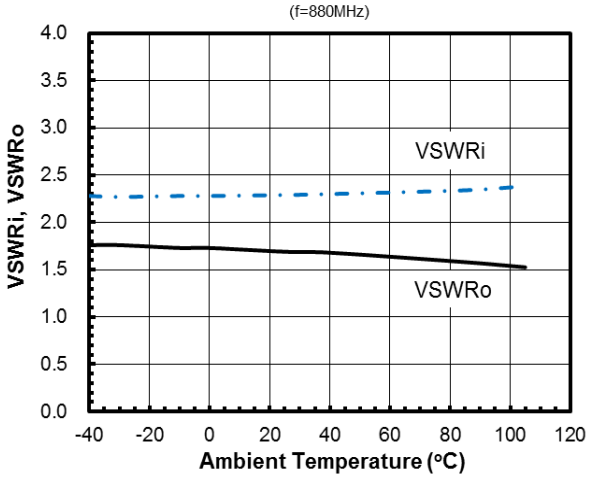
P-1dB(OUT) vs. Ambient Temperature



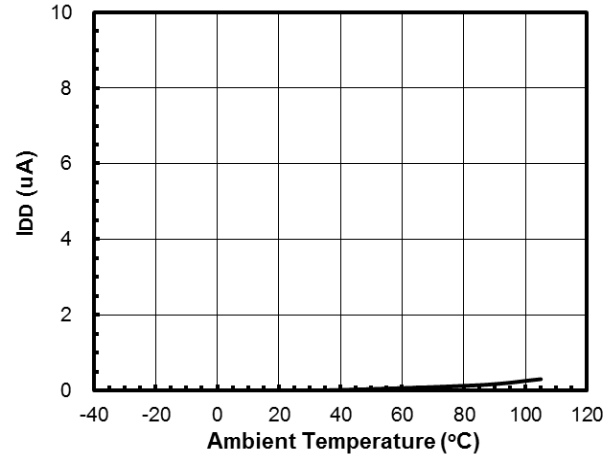
OIP3, IIP3 vs. Ambient Temperature



VSWRi, VSWRo vs. Ambient Temperature



IDD vs. Ambient Temperature

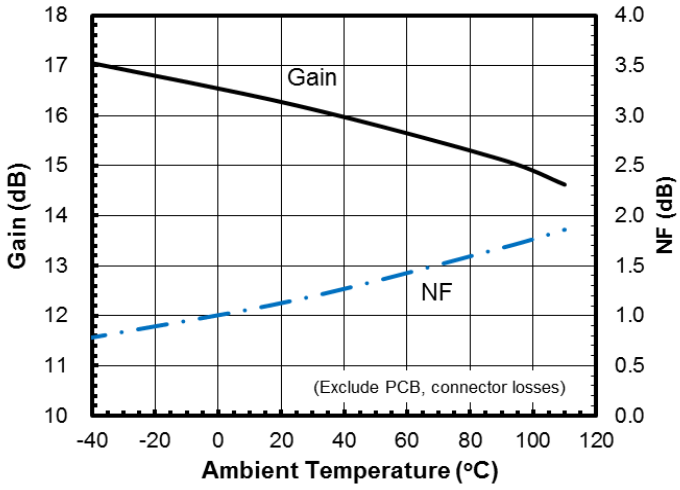


■ ELECTRICAL CHARACTERISTICS (LNA High Gain Mode 2)

(General Conditions: f_{RF}=760MHz, V_{DD}=V_{INV}=V_{CTL}=3.3V, Zs=Zl=50Ω, with application circuit 2)

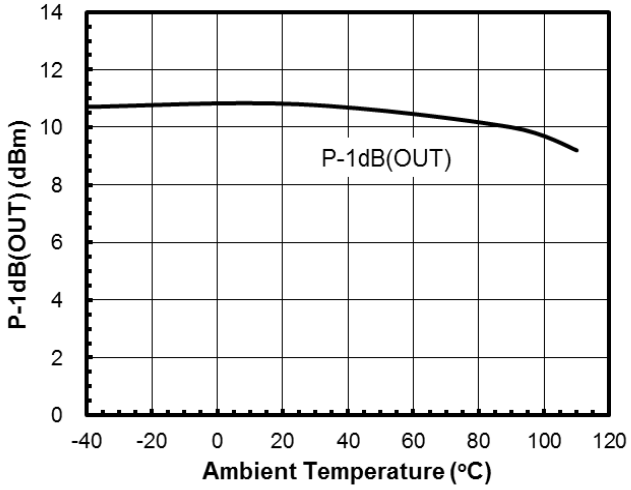
Gain, NF vs. Ambient Temperature

(f=760MHz)



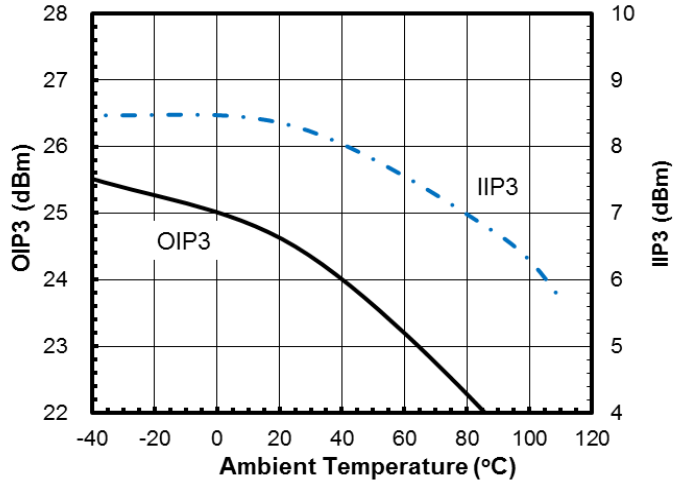
P-1dB(OUT) vs. Ambient Temperature

(f=760MHz)



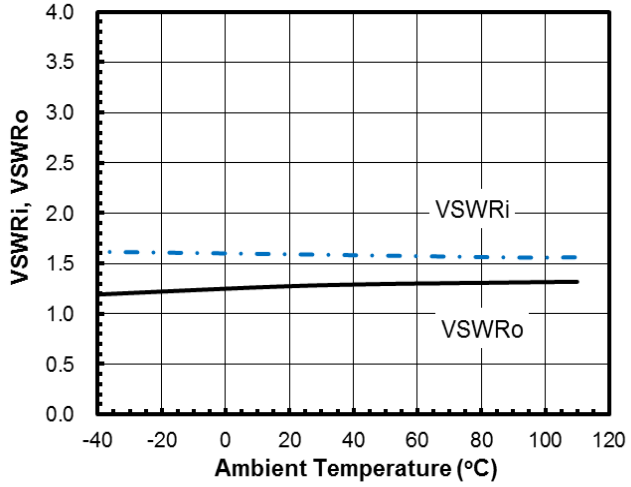
OIP3, IIP3 vs. Ambient Temperature

(f1=760MHz,f2=f1+100kHz, Pin=-25dBm)



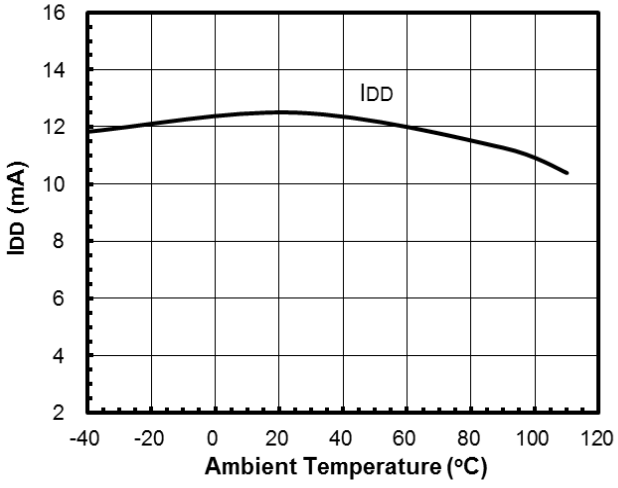
VSWRi, VSWRo vs. Ambient Temperature

(f=760MHz)



IDD vs. Ambient Temperature

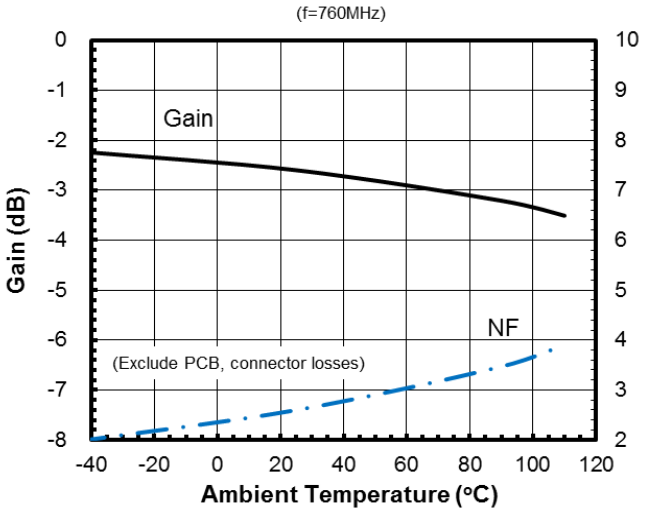
(RF OFF)



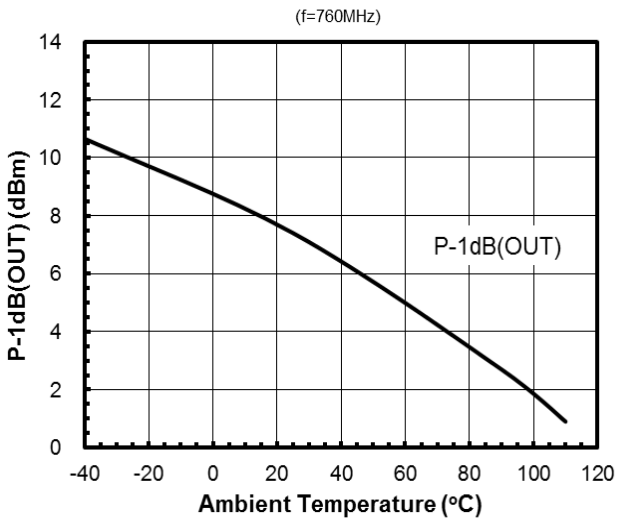
■ ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode 2)

(General Conditions: f_{RF}=760MHz, V_{DD}=V_{INV}=3.3V, V_{CTL}=0V, Zs=Zl=50Ω, with application circuit 2)

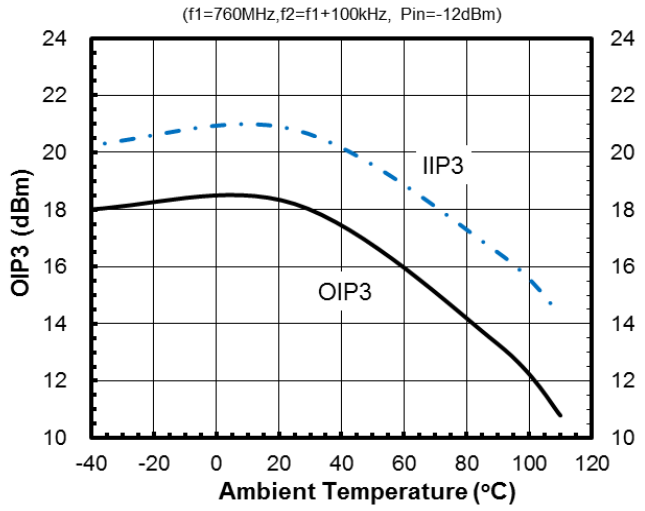
Gain, NF vs. Ambient Temperature



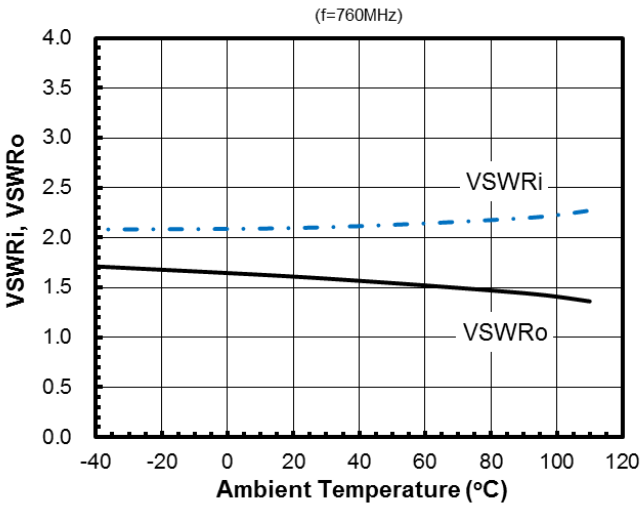
P-1dB(OUT) vs. Ambient Temperature



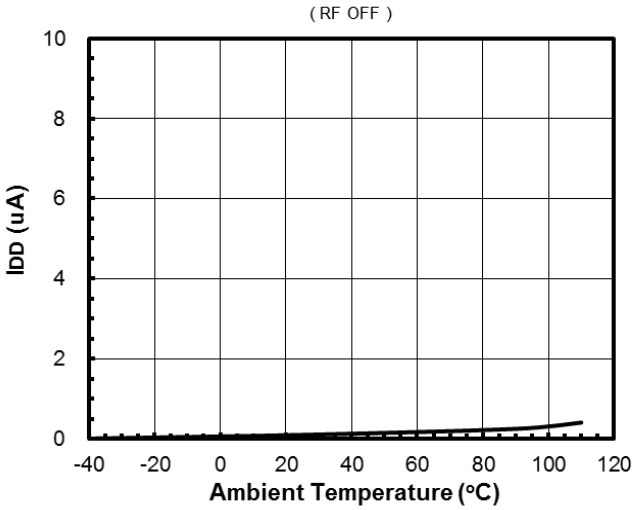
OIP3, IIP3 vs. Ambient Temperature



VSWRi, VSWRo vs. Ambient Temperature

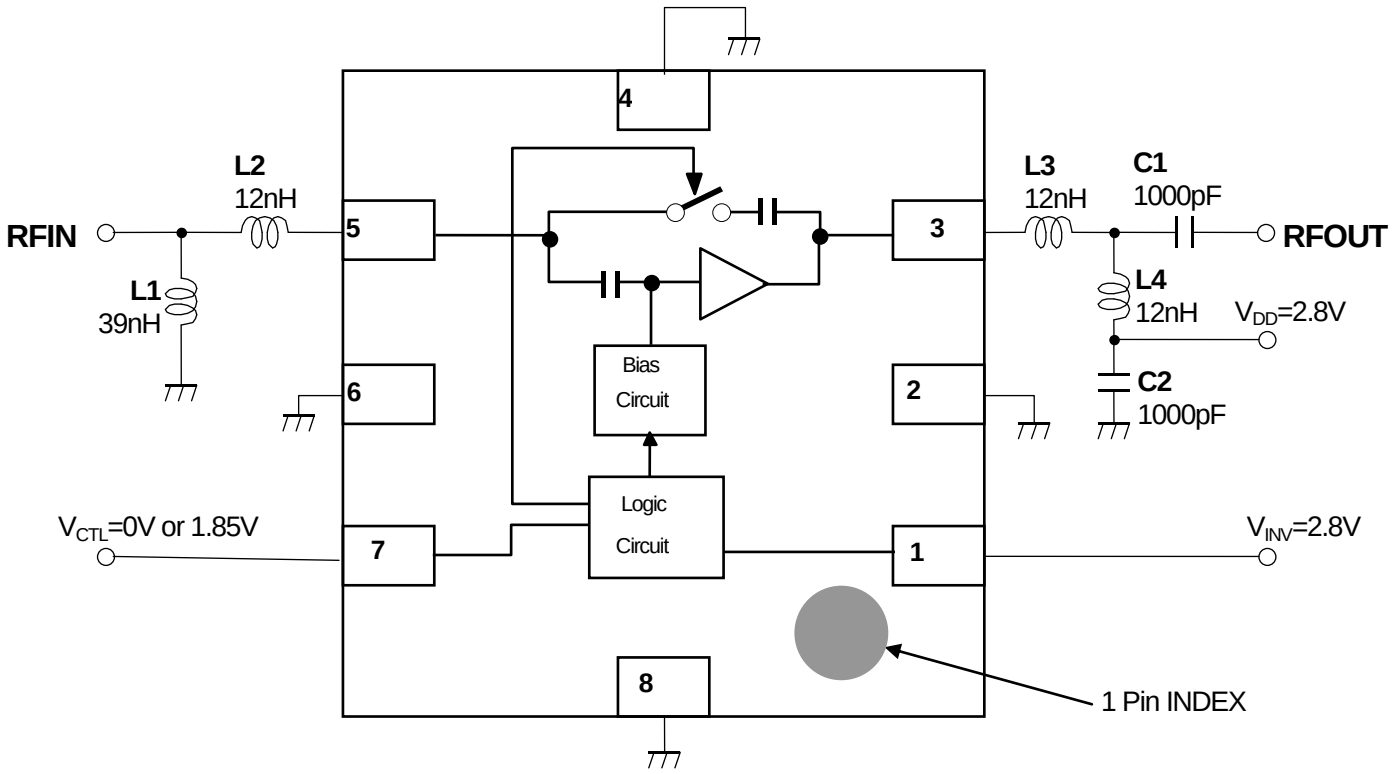


IDD vs. Ambient Temperature



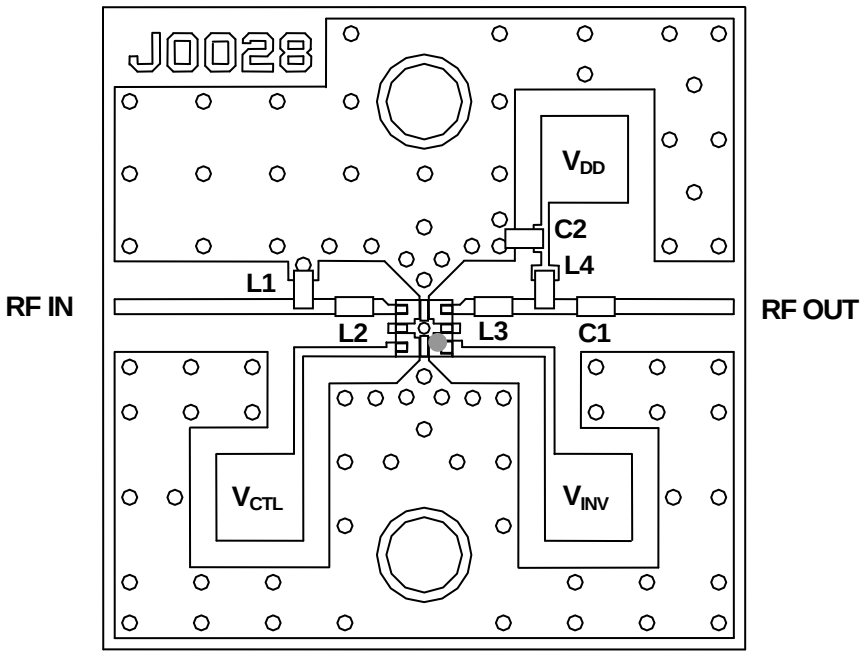
■ APPLICATION CIRCUIT 1(f_{RF}= 880MHz)

(Top View)



■ EVALUATION BOARD PCB LAYOUT 1(f_{RF}= 880MHz)

(Top View)

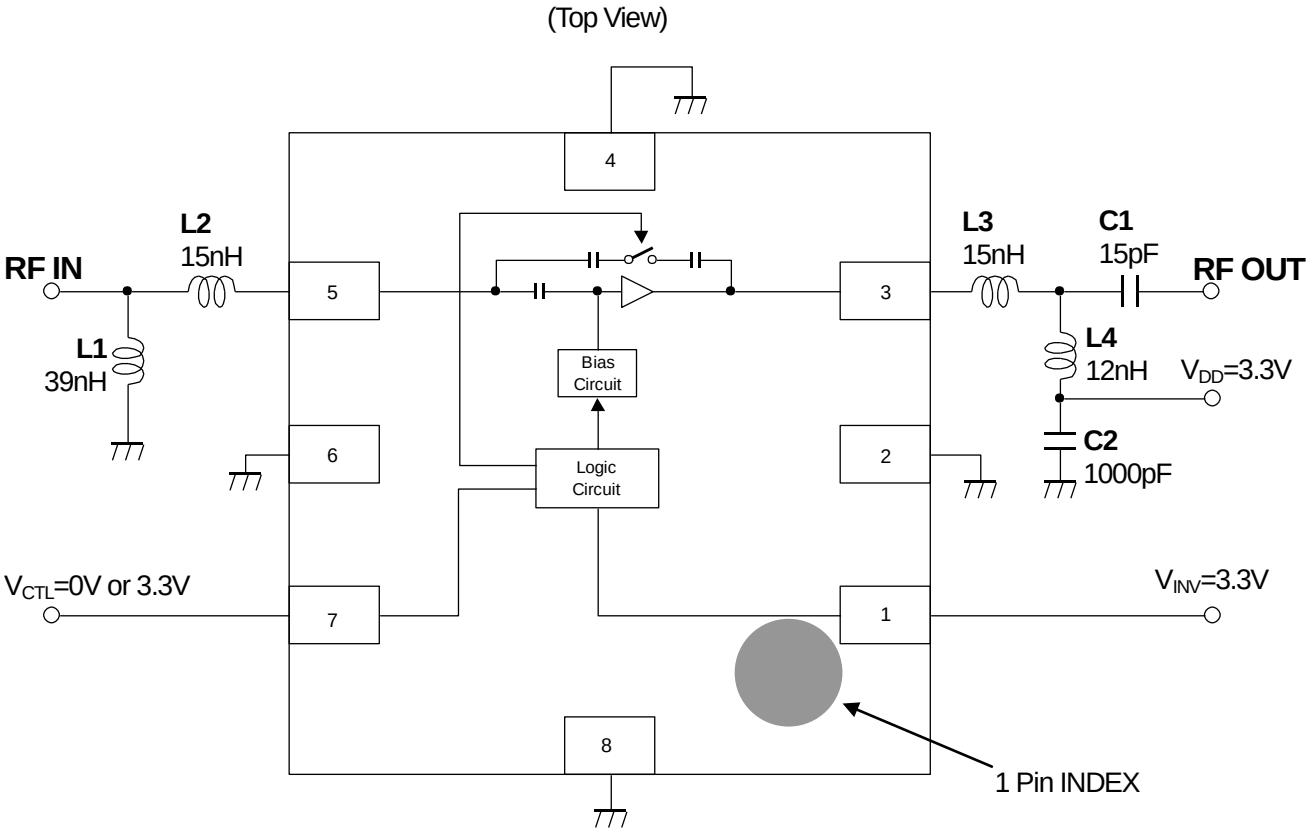


■ Parts List 1(f_{RF}= 880MHz)

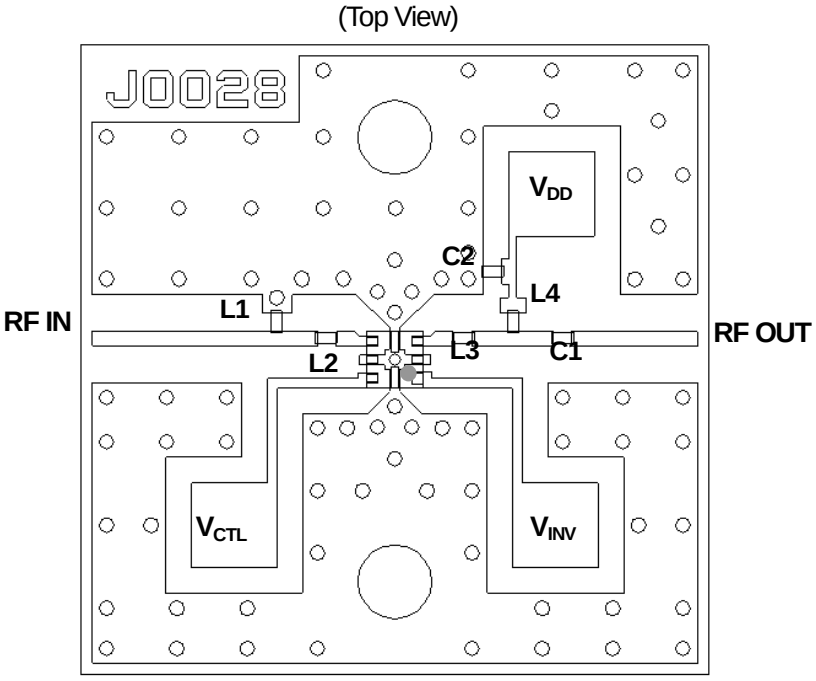
Parts ID	Notes
L1~L4	TAIYO-YUDEN (HK1005 series)
C1,C2	MURATA (GRM15 series)

PCB (FR-4) :
t=0.2mm
MICROSTRIP LINE WIDTH
=0.4mm (Z_0=50Ω)
PCB SIZE =17.0mm X 17.0mm

■ APPLICATION CIRCUIT 2(f_{RF}= 760MHz)



■ EVALUATION BOARD PCB LAYOUT 2(f_{RF}= 760MHz)

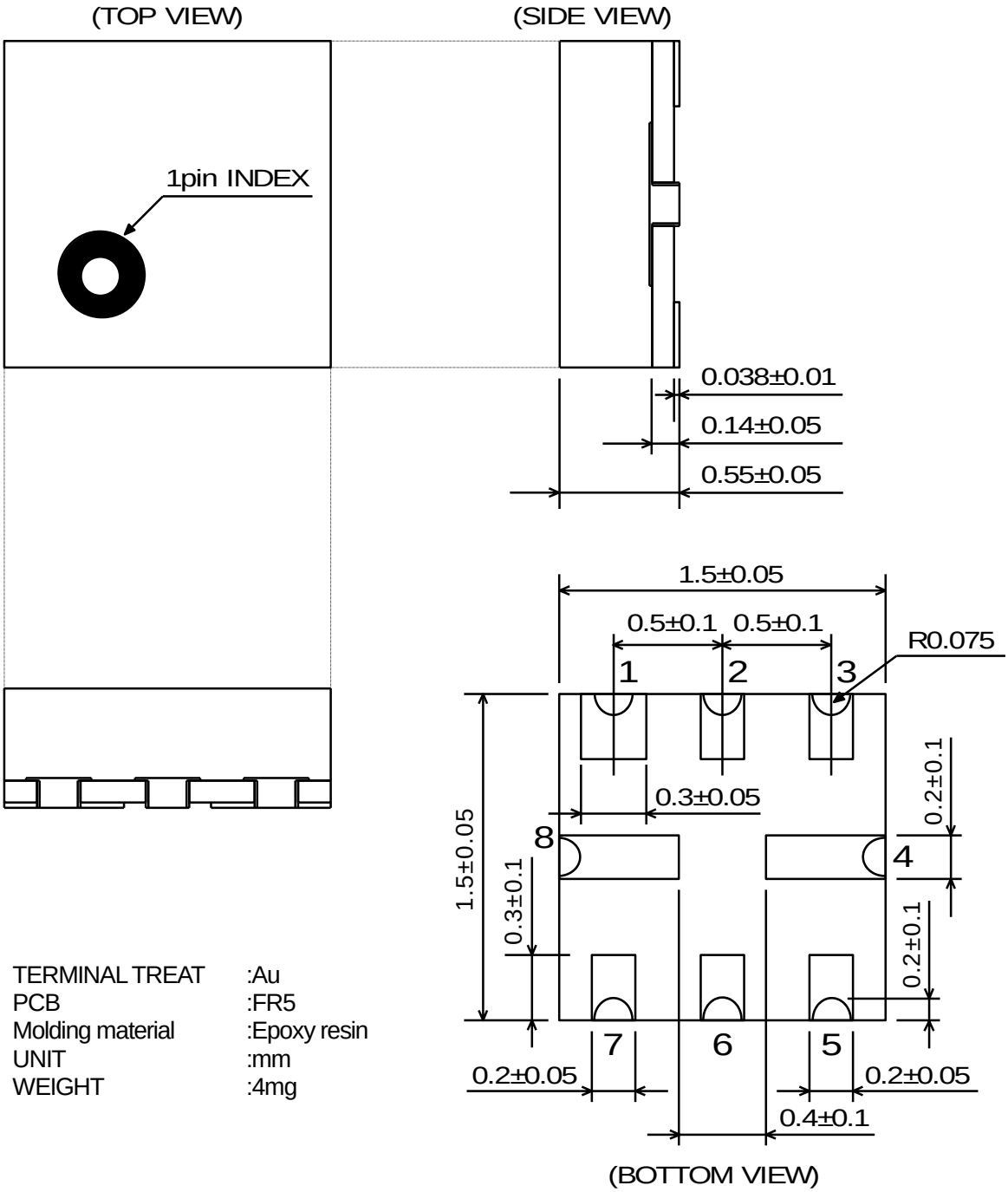


■ Parts List 2 (f_{RF}=760MHz)

Parts ID	Notes
L1 ~ L4	MURATA (LQP03T_02 Series)
C1,C2	MURATA (GRM03 Series)

PCB (FR-4) :
t=0.2mm
MICROSTRIP LINE WIDTH
=0.4mm (Z_0=50Ω)
PCB SIZE =17.0mm X 17.0mm

■**PACKAGE OUTLINE** (USB8-B6)



TERMINAL TREAT	:Au
PCB	:FR5
Molding material	:Epoxy resin
UNIT	:mm
WEIGHT	:4mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.