HB526R864ESN-10H/10/12

4,194,304-word × 64-bit (Non Parity)× 2-bank Synchronous Dynamic RAM Module

HITACHI

ADE-203-671C (Z)
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Description

The HB526R864ESN belongs to 8 byte DIMM (Dual In-line Memory Module) family, and has been developed a as optimized main memory solution for 8 byte processor applications. The HB526R864ESN is a 4M × 64 × 2 banks Synchronous Dynamic RAM module, mounted 32 pieces of 16-Mbit SDRAM (HM5216405) sealed in TCP package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). An outline of the HB526R864ESN is 168-pin socket type package (dual lead out). Therefore, the HB526R864ESN makes high density mounting possible without surface mount technology. The HB526R864ESN provides common data inputs and outputs. Decoupling capacitors are mounted beside each TCP on the module board.

Features

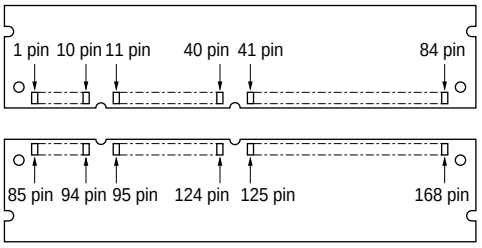
- 168-pin socket type package (dual lead out)
  - Lead pitch : 1.27 mm
- 3.3 V (±0.3 V) power supply
- Clock frequency : 100 MHz / 83 MHz
- JEDEC standard outline unbuffered 8-byte DIMM
- LVTTL interface
- Data bus width: × 64 (non parity)bit
- Single pulsed $\overline{RAS}$
- 2 Banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8/full page
- Programmable burst sequence
  - Sequential/interleave
- Full page burst length capability
  - Sequential burst
  - Burst stop capability
- Programmable $\overline{CAS}$ latency: 2/3
- 4096 refresh cycles: 64 ms
- 2 variations of refresh

— Auto refresh
— Self refresh

Ordering Information

Type No.	Frequency	Package	Contact pad
HB526R864ESN-10H	100 MHz	168-pin dual lead out socket type	Gold
HB526R864ESN-10	100 MHz		
HB526R864ESN-12	83 MHz		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	NC	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	V_{SS}	106	NC	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	A11 (BS)	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	NC	168	V_{DD}

Pin Description

Pin name	Function
A0 to A11	Address input Row address A0 to A10 Column address A0 to A9 Bank select address A11
DQ0 to DQ63	Data-input/output
$\overline{S0}$ to $\overline{S3}$ ($\overline{CS}$0 to $\overline{CS}$3)	Chip select
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQMB0 to DQMB7 (DQM0 to DQM7)	Input/output mask
CK0 to CK3 (CLK0 to CLK3)	Clock input
CKE0/CKE1	Clock enable
SDA	Data-input/output for serial PD
SCL	Clock input for serial PD
SA0 to SA2	Serial address input
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

Serial PD Matrix*[1]

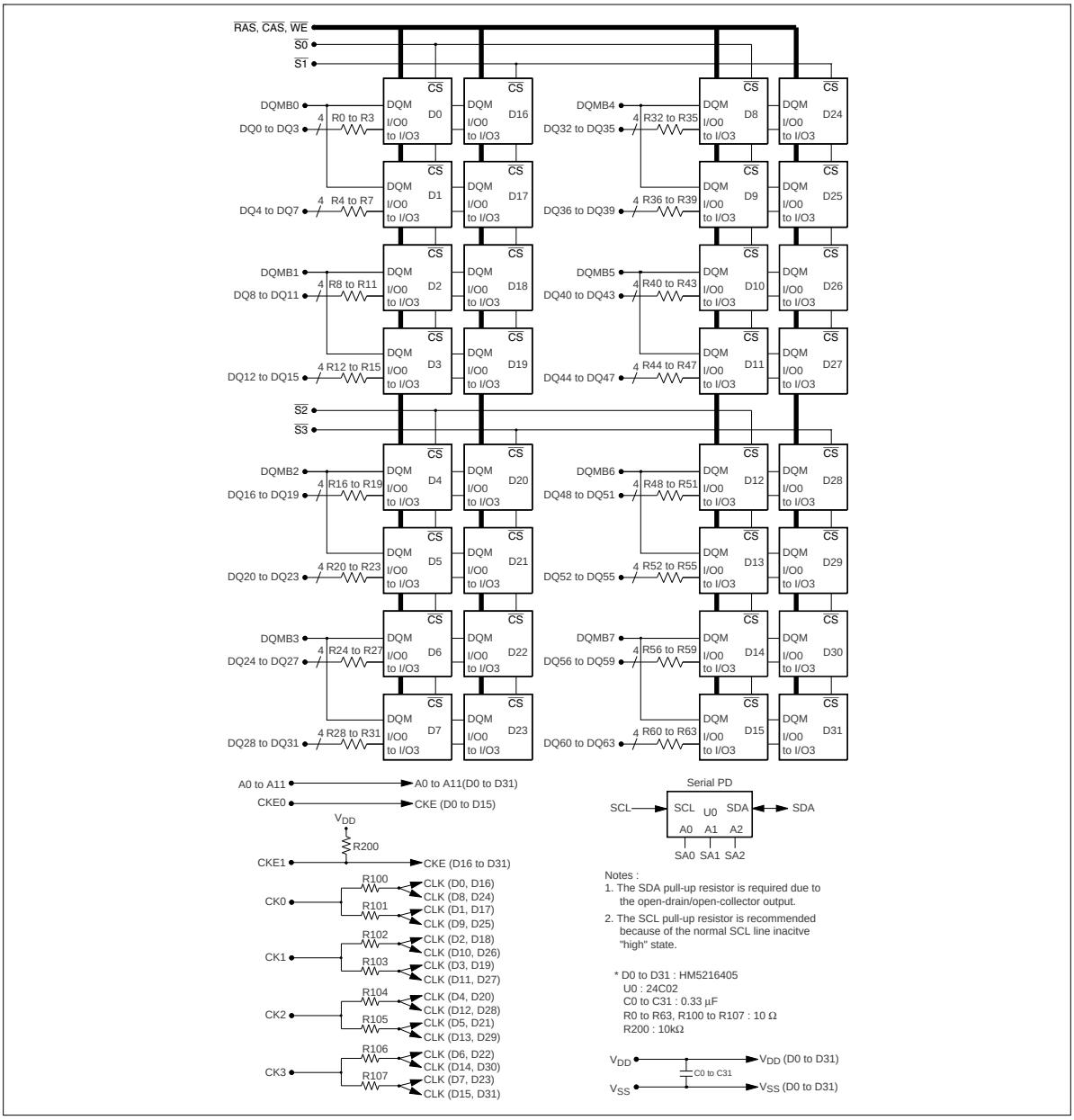
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	0	1	1	0B	11
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	1	0	02	2
6	Module data width	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest $\overline{CE}$ latency)										
	-10H, -10 (10 ns)	1	0	1	0	0	0	0	0	A0	CL = 3
	-12 (12 ns)	1	1	0	0	0	0	0	0	C0	
10	SDRAM access from Clock (highest $\overline{CE}$ latency)										
	-10H, -10 (8 ns)	1	0	0	0	0	0	0	0	80	
	-12 (9.5 ns)	1	0	0	1	0	1	0	1	95	
11	Module configuration type	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type	1	0	0	0	0	0	0	0	80	Normal (15.625 μs) Self refresh
13	SDRAM width	0	0	0	0	0	1	0	0	04	× 4
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00	—
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	8F	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	0	1	0	02	2
18	SDRAM device attributes: $\overline{CE}$ latency	0	0	0	0	0	1	1	0	06	2, 3

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
19	SDRAM device attributes: $\overline{CS}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{W}$ latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00	Non buffer
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	$V_{CC} \pm 10\%$
23	SDRAM cycle time (2nd highest $\overline{CE}$ latency)										
	-10H, -10 (15 ns)	1	1	1	1	0	0	0	0	F0	CL = 2
	-12 (18 ns)	0	0	1	1	0	0	0	0	30	
24	SDRAM access from Clock (2nd highest $\overline{CE}$ latency)										
	-10H (9 ns)	1	0	0	1	0	0	0	0	90	
	-10 (9.5 ns)	1	0	0	1	0	1	0	1	95	
	-12 (10 ns)	1	0	1	0	0	0	0	0	A0	
25	SDRAM cycle time (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
26	SDRAM access from Clock (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time										
	-10H, -10	0	0	0	1	1	1	1	0	1E	30 ns
	-12	0	0	1	0	0	1	0	0	24	36 ns
28	Row active to row active min										
	-10H, -10	0	0	0	1	0	1	0	0	14	20 ns
	-12	0	0	0	1	1	0	0	0	18	24 ns
29	$\overline{RE}$ to $\overline{CE}$ delay min	0	0	0	1	1	1	1	0	1E	30 ns
30	Minimum $\overline{RE}$ pulse width										
	-10H, -10	0	0	1	1	1	1	0	0	3C	60 ns
	-12	0	1	0	0	1	0	0	0	48	72 ns
31	Density of each bank on module	0	0	0	0	1	0	0	0	08	32M byte
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	0	0	0	0	1	01	Rev.1
63	Checksum for bytes 0 to 62										
	-10H	0	1	0	0	0	1	0	1	45	
	-10	0	1	0	0	1	0	1	0	4A	
	-12	1	1	1	0	0	0	0	0	E0	

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	ASCII-8bit code*[2]
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
78	Manufacturer's part number	0	1	0	1	0	0	1	0	52	R
79	Manufacturer's part number	0	0	1	1	1	0	0	0	38	8
80	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number	0	0	1	1	0	1	0	0	34	4
82	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
83	Manufacturer's part number	0	1	0	1	0	0	1	1	53	S
84	Manufacturer's part number	0	1	0	0	1	1	1	0	4E	N
85	Manufacturer's part number	0	1	0	1	1	1	1	1	5F	—
86	Manufacturer's part number	0	0	1	1	0	0	0	1	31	1
87	Manufacturer's part number -10H, -10	0	0	1	1	0	0	0	0	30	0
	-12	0	0	1	1	0	0	1	0	32	2
88	Manufacturer's part number -10H	0	1	0	0	1	0	0	0	48	H
	-10, -12	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (binary) *[3]
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (binary) *[4]
95 to 98	Assembly serial number	*[5]									
99 to 125	Manufacturer specific data	*[6]									
126	Intel specification frequency	0	1	1	0	0	1	1	0	66	66 MHz
127	Intel specification $\overline{CE}$# latency support	0	0	0	0	0	1	1	0	06	CL = 2, 3

Notes: 1. All serial PD data are not protected. 0: Serial data, “Low level”, 1: Serial data, “High level”
2. Byte72 is manufacturing location code. (ex: in case of Japan, byte72 is 4Ah. 4Ah shows “J” on ASCII code.)
3. Byte 93 (Manufacturing date-year code) ex: 61h shows year 97, 62h shows year 98.
4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11, 24h shows week 36.
5. Bytes 95 through 98 are assembly serial number.
6. All bits of 99 through 125 are not defined (“1” or “0”).

Block Diagram



Notes :
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D31 : HM5216405
U0 : 24C02
C0 to C31 : 0.33 µF
R0 to R63, R100 to R107 : 10 Ω
R200 : 10kΩ

Command Operation, Mode Resistor Configuration and Operation

Refer to the HM5216405 Series data sheet.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{DD}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	16	W
Operating temperature	Topr	0 to +65	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	3.0	3.3	3.6	V	1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	—	4.6	V	1, 2
Input low voltage	V_{IL}	–0.3	—	0.8	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns
3. V_{IL} (min) = –1.0 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to +65°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526R864ESN						
		-10H/-10		-12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	2320	—	2000	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	—	96	—	96	mA	CKE = V_{IL}, t_{CK} = min	5
		—	64	—	64	mA	CKE = V_{IL} CLK = V_{IL} or V_{IH} Fixed	6
		—	1280	—	1120	mA	CKE = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	224	—	224	mA	CKE = V_{IL}, t_{CK} = min, I/O = High-Z	1, 2
		—	1440	—	1280	mA	CKE = V_{IH}, NOP command t_{CK} = min, I/O = High-Z	1, 2, 3
Burst operating current (CL = 2)	I_{CC4}	—	2320	—	2000	mA	t_{CK} = min, BL = 4	1, 2, 4
(CL = 3)	I_{CC4}	—	3120	—	2640	mA		
Auto refresh current	I_{CC5}	—	2080	—	1760	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	64	—	64	mA	$V_{IH} \geq V_{DD}$ – 0.2 V 0 V ≤ V_{IL} ≤ 0.2 V	7
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 ≤ Vin ≤ V_{DD}	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 ≤ Vout ≤ V_{DD} I/O = disable	
Output high voltage	V_{OH}	2.4	V_{DD}	2.4	V_{DD}	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = +25°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	180	pF	1, 3
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	C_{I2}	—	180	pF	1, 3
Input capacitance ($\overline{CS}$)	C_{I3}	—	60	pF	1, 3
Input capacitance (CLK)	C_{I4}	—	60	pF	1, 3
Input capacitance (DQM)	C_{I5}	—	40	pF	1, 3
Input/output capacitance (DQ0 to DQ63)	$C_{I/O1}$	—	27	pF	1, 2, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +65°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526R864ESN					
		-10H/-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
System clock cycle time							
(CL = 2)	t_{CK}	15	—	18	—	ns	1
(CL = 3)	t_{CK}	10	—	12	—	ns	
CLK high pulse width	t_{CKH}	3	—	4	—	ns	1
CLK low pulse width	t_{CKL}	3	—	4	—	ns	1
Access time from CLK							
(CL = 2) (-10H)	t_{AC}	—	9	—	12	ns	1, 2
(CL = 2) (-10)	t_{AC}	—	9.5	—	12	ns	
(CL = 3)	t_{AC}	—	8	—	9.5	ns	
Data-out hold time	t_{OH}	3	—	3	—	ns	1, 2
CLK to Data-out low impedance	t_{LZ}	0	—	0	—	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2, 3)	t_{HZ}	—	7	—	9	ns	1, 4
Data-in setup time	t_{DS}	2	—	3	—	ns	1
Data in hold time	t_{DH}	1	—	1	—	ns	1
Address setup time	t_{AS}	2	—	3	—	ns	1
Address hold time	t_{AH}	1	—	1	—	ns	1
CKE setup time	t_{CES}	2	—	3	—	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	—	3	—	ns	1
CKE hold time	t_{CEH}	1	—	1	—	ns	1

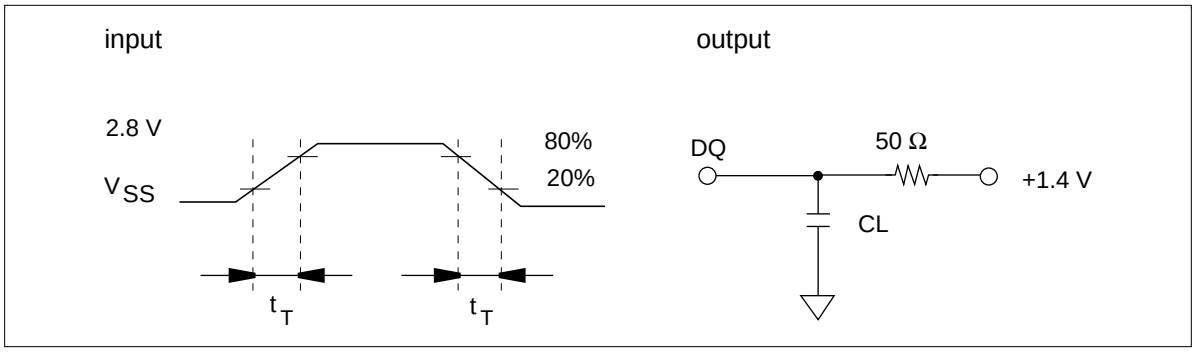
AC Characteristics (Ta = 0 to 65°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

		HB526R864ESN					
		-10H/-10		-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Command setup time	t_{CS}	2	—	3	—	ns	1
Command hold time	t_{CH}	1	—	1	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	—	108	—	ns	
Active to precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to precharge on full page mode	t_{RASC}	—	120000	—	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	36	—	ns	1
Precharge to active command period	t_{RP}	30	—	36	—	ns	1
Write recovery or data-in to precharge command	t_{DPL}	15	—	18	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	—	24	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is C_L = 50 pF with current source.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE setup time to CKE rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		HB526R864ESN						
		-10H/-10			-12			
Frequency (MHz)		**100**	**66**	**33**	**83**	**55**	**28**	
t_{CK} (ns)	**Symbol**	**10**	**15**	**30**	**12**	**18**	**36**	**Notes**
Active command to column command (same bank)	t_{RCD}	3	2	1	3	2	1	1
Active command to active command (same bank)	t_{RC}	9	6	3	9	6	3	= [t_{RAS} + t_{RP}] 1
Active command to precharge command (same bank)	t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)	t_{RP}	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)	t_{DPL}	2	1	1	2	1	1	1
Active command to active command (different bank)	t_{RRD}	2	2	1	2	2	1	1
Self refresh exit time	I_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	I_{APW}	5	3	2	5	3	2	= [t_{DPL} + t_{RP}]
Self refresh exit to command input	I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance ($\overline{CAS}$ latency = 3)	I_{HZP}	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	I_{HZP}	—	2	2	—	2	2	
Last data out to active command (auto precharge) (same bank)	I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge) ($\overline{CAS}$ latency = 3)	I_{EP}	–2	–2	–2	–2	–2	–2	
($\overline{CAS}$ latency = 2)	I_{EP}	—	–1	–1	—	–1	–1	
Column command to column command	I_{CCD}	1	1	1	1	1	1	
Write command to data in latency	I_{WCD}	0	0	0	0	0	0	
DQM to data in	I_{DID}	0	0	0	0	0	0	
DQM to data out	I_{DOD}	2	2	2	2	2	2	
CKE to CKE disable	I_{CLE}	1	1	1	1	1	1	

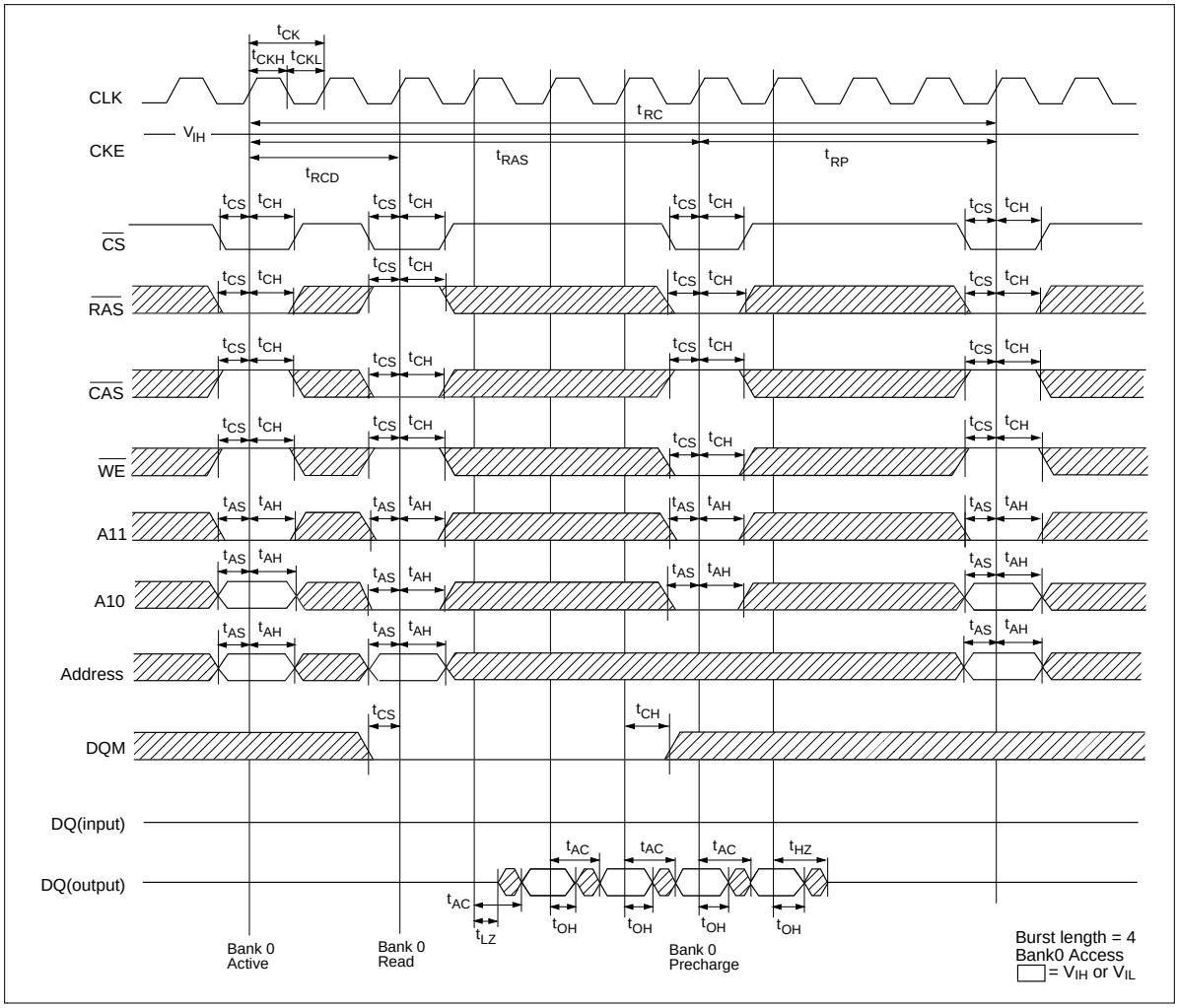
Relationship Between Frequency and Minimum Latency (cont)

Parameter	Symbol	HB526R864ESN -10H/-10			-12			Notes
Frequency (MHz)		**100**	**66**	**33**	**83**	**55**	**28**	
t_{CK} (ns)		**10**	**15**	**30**	**12**	**18**	**36**	
Register set to active command	t_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable	I_{CDD}	0	0	0	0	0	0	
Power down exit to command input	I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold ($\overline{CAS}$ latency = 3)	I_{BSR}	2	2	2	2	2	2	
($\overline{CAS}$ latency = 2)	I_{BSR}	—	1	1	—	1	1	
Burst stop to output high impedance ($\overline{CAS}$ latency = 3)	I_{BSH}	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	I_{BSH}	—	2	2	—	2	2	
Burst stop to write data ignore	I_{BSW}	0	0	0	0	0	0	

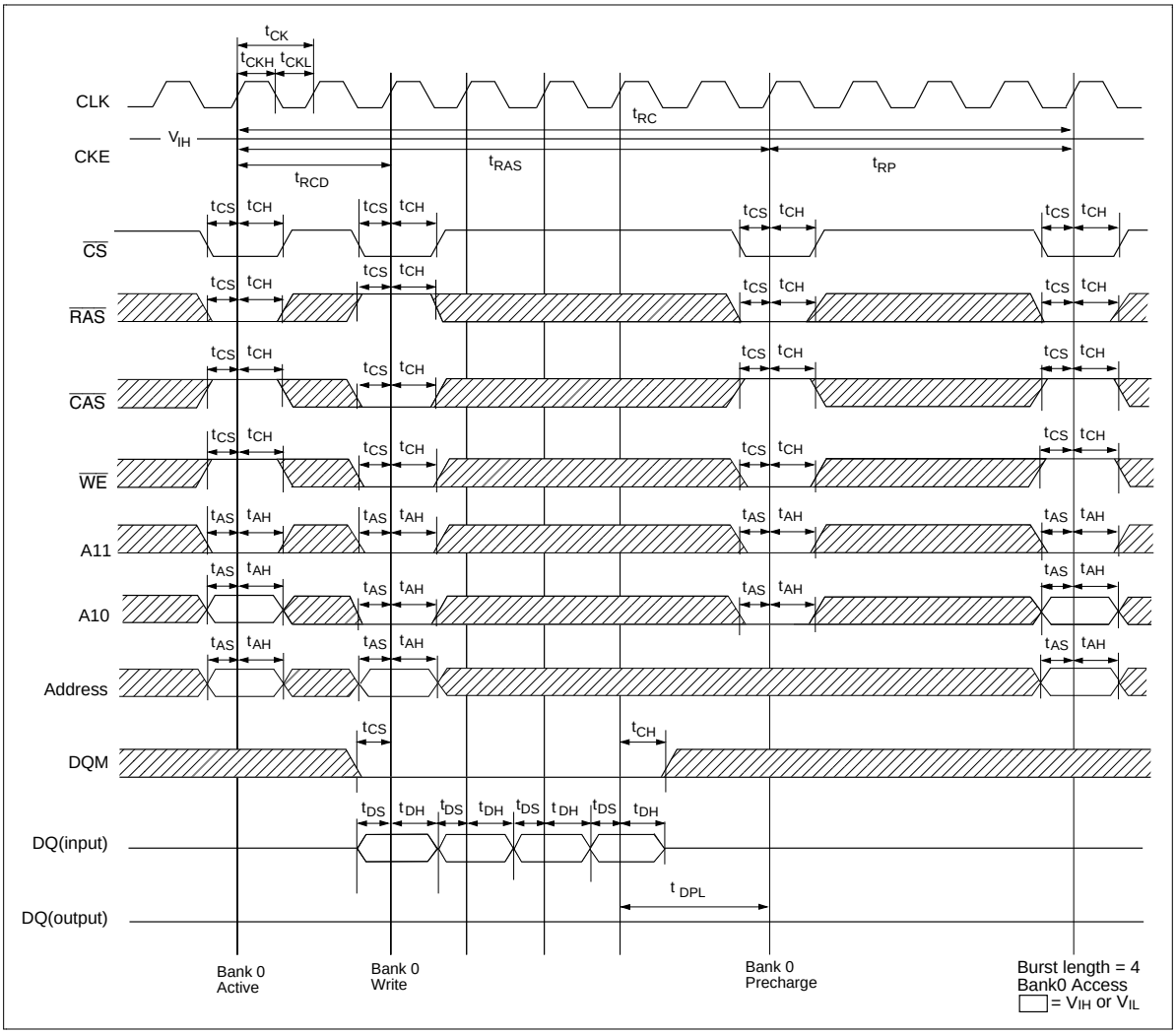
Notes: 1. t_{RCD} to t_{RRD} are recommended value.
2. When self refresh exit is executed, CKE should be kept “H” longer than I_{SREX} from exit cycle.

Timing Waveforms

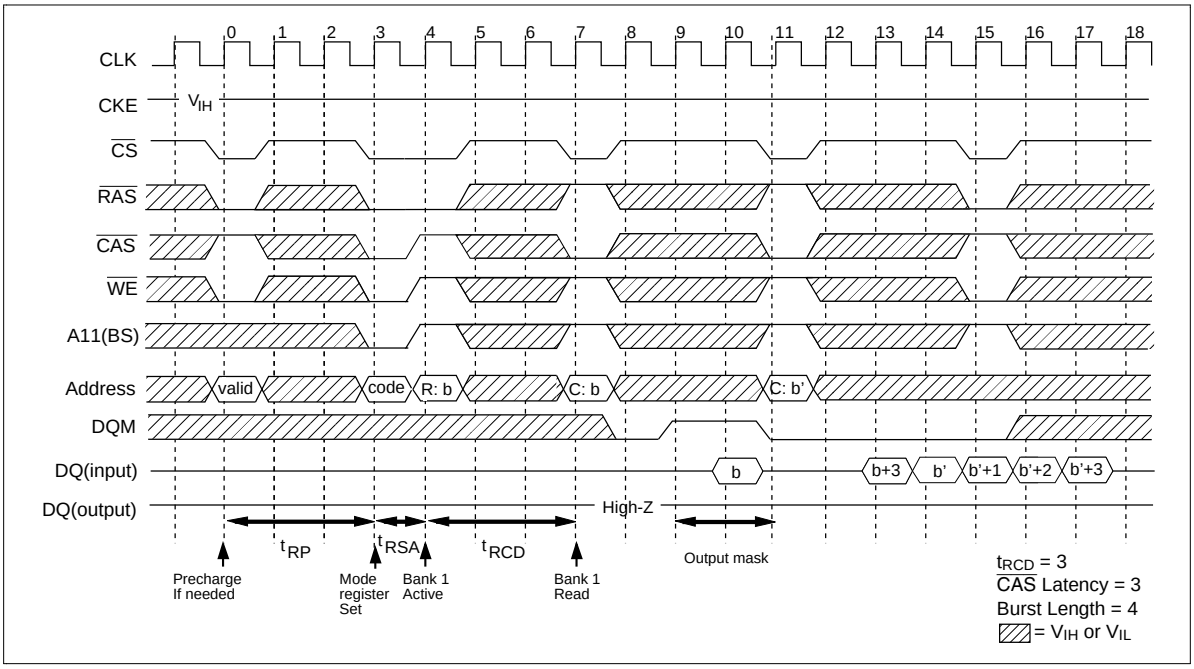
Read Cycle



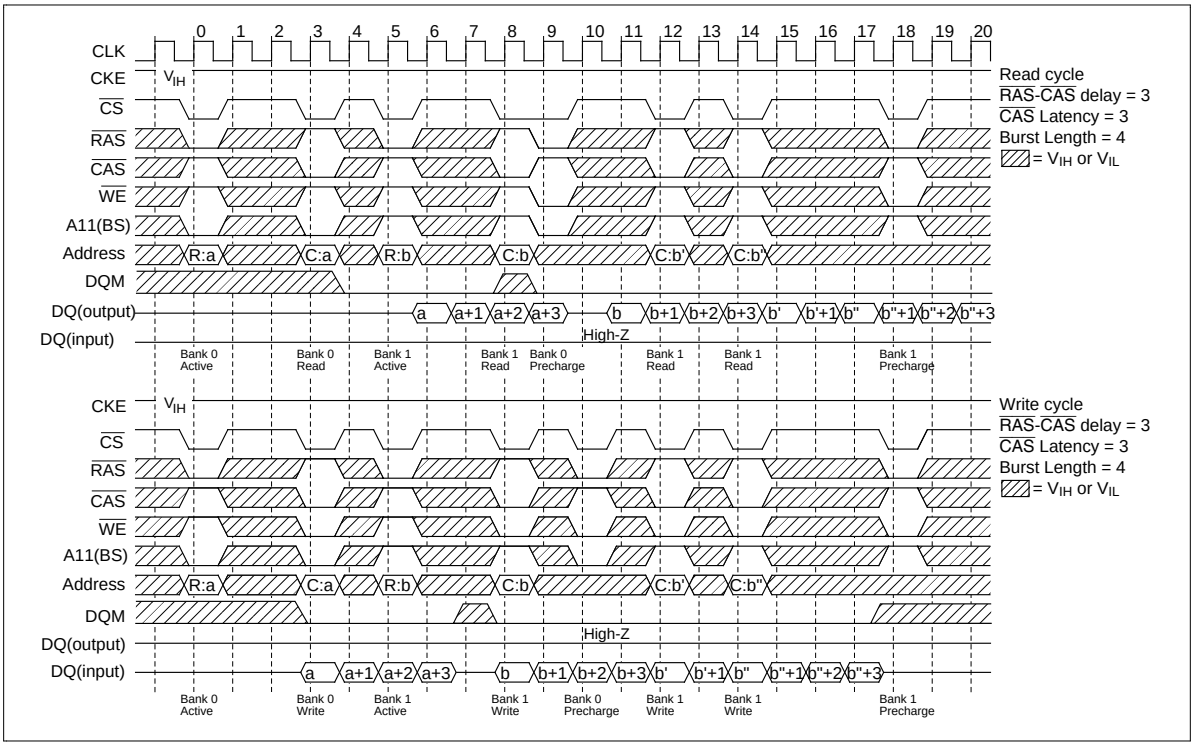
Write Cycle


tCK
tCKH tCKL
CLK
tRC
VIH
CKE
tRAS
tRP
tRCD
tCS tCH
CS
RAS
CAS
WE
tAS tAH
A11
A10
Address
DQM
tDS tDH
DQ(input)
t DPL
DQ(output)
Bank 0 Active
Bank 0 Write
Bank 0 Precharge
Burst length = 4
Bank0 Access
= VIH or VIL

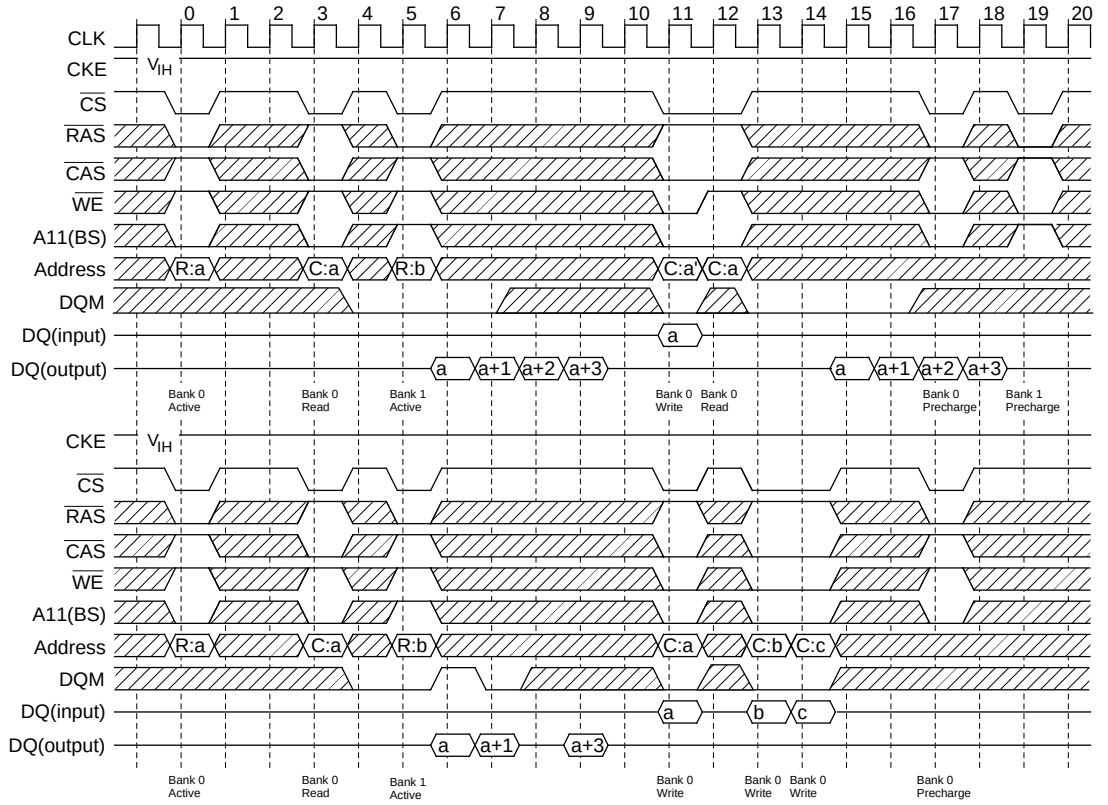
Mode Register Set Cycle



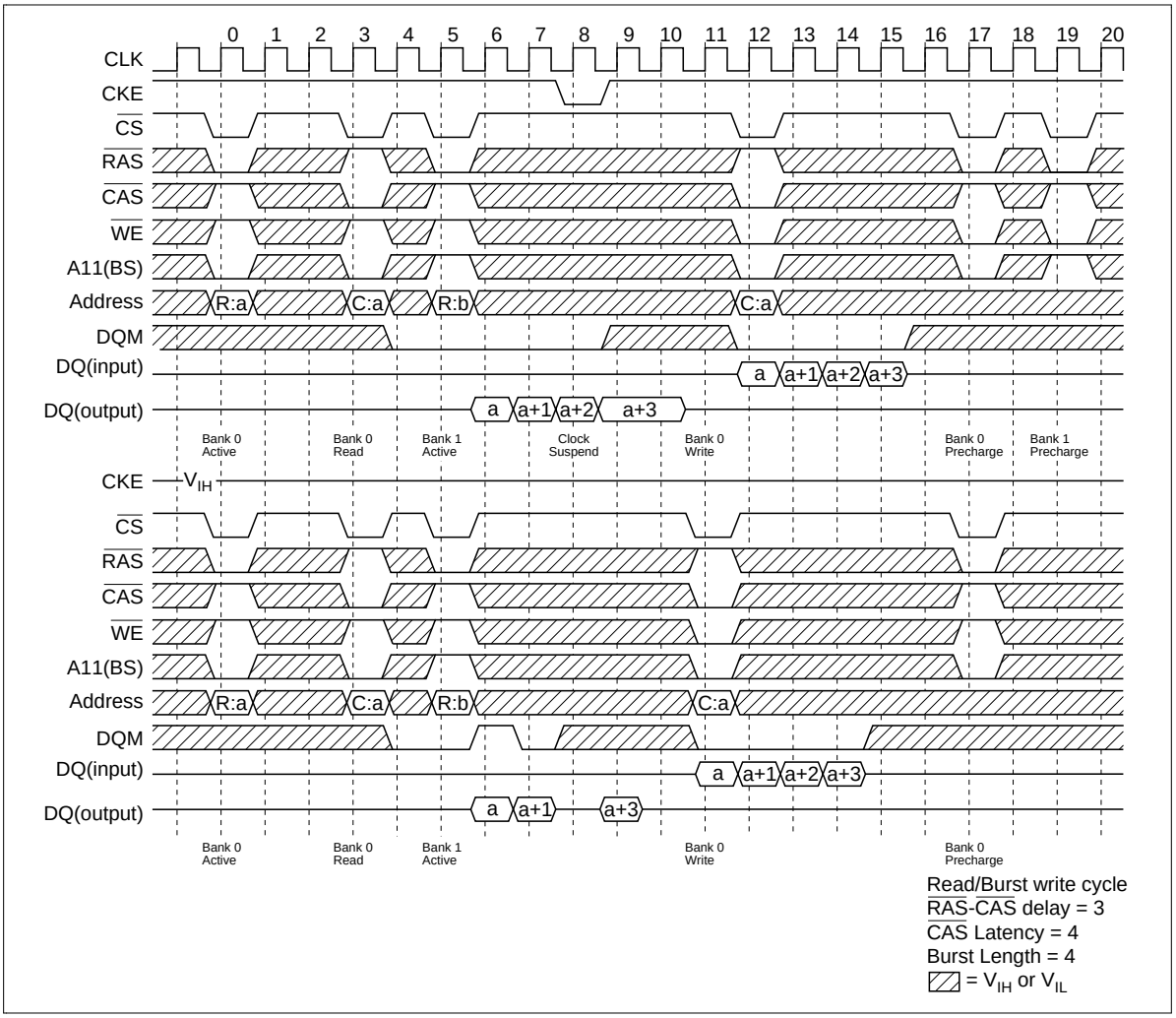
Read Cycle/Write Cycle



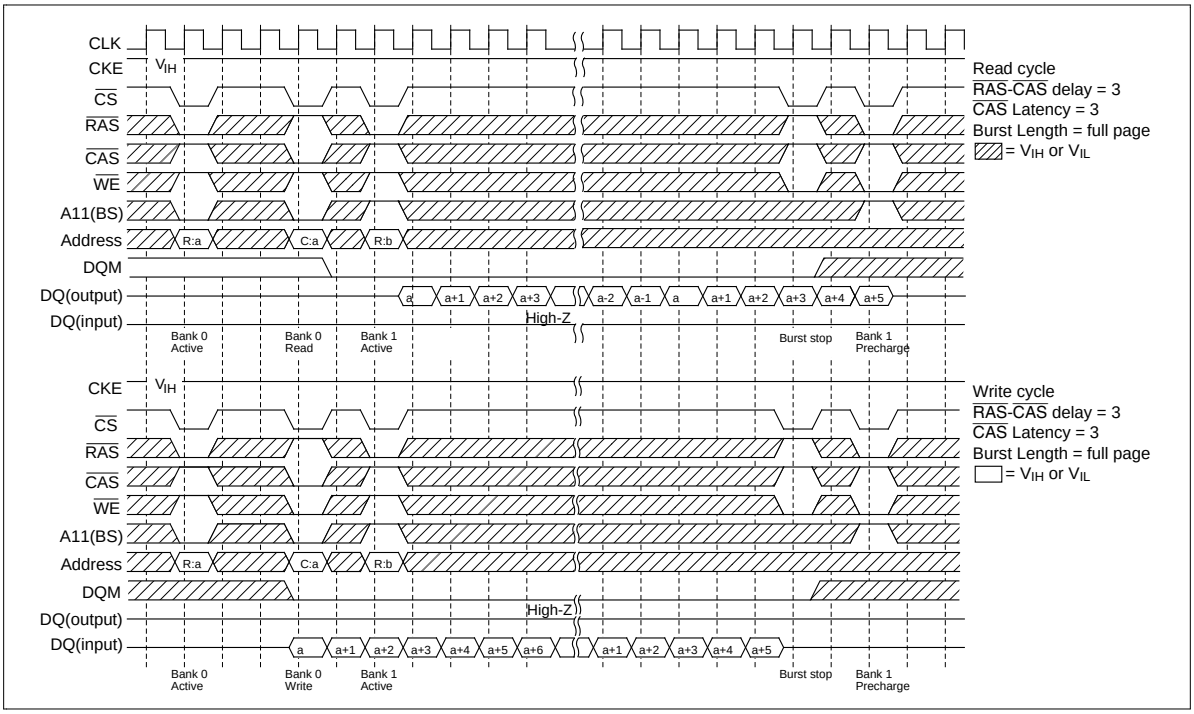
Read/Single Write Cycle



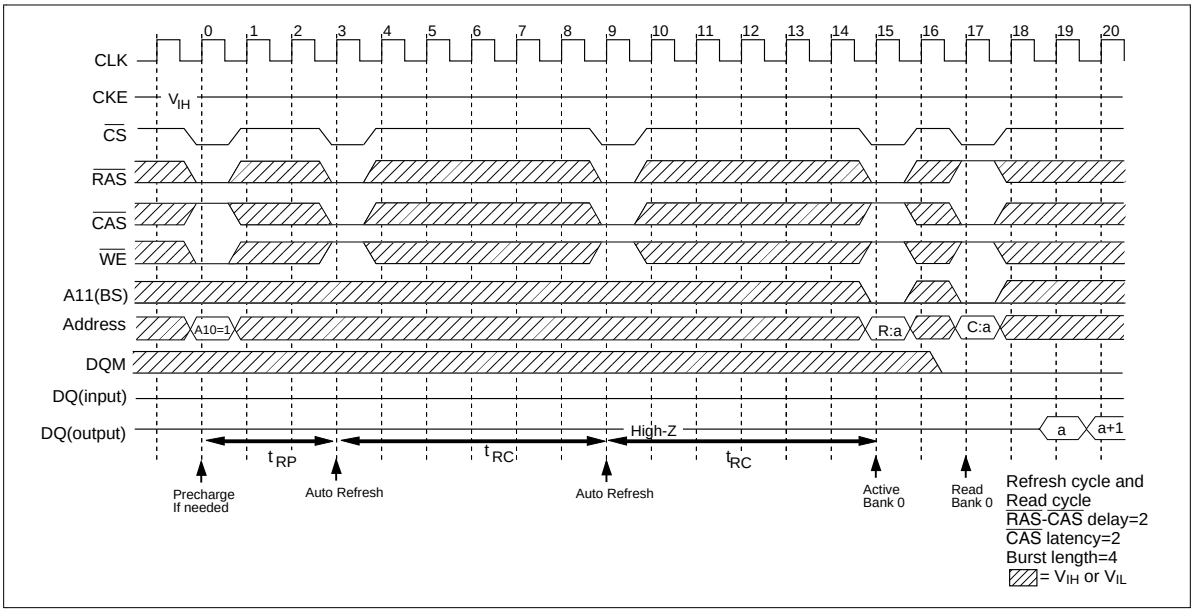
Read/Burst Write Cycle



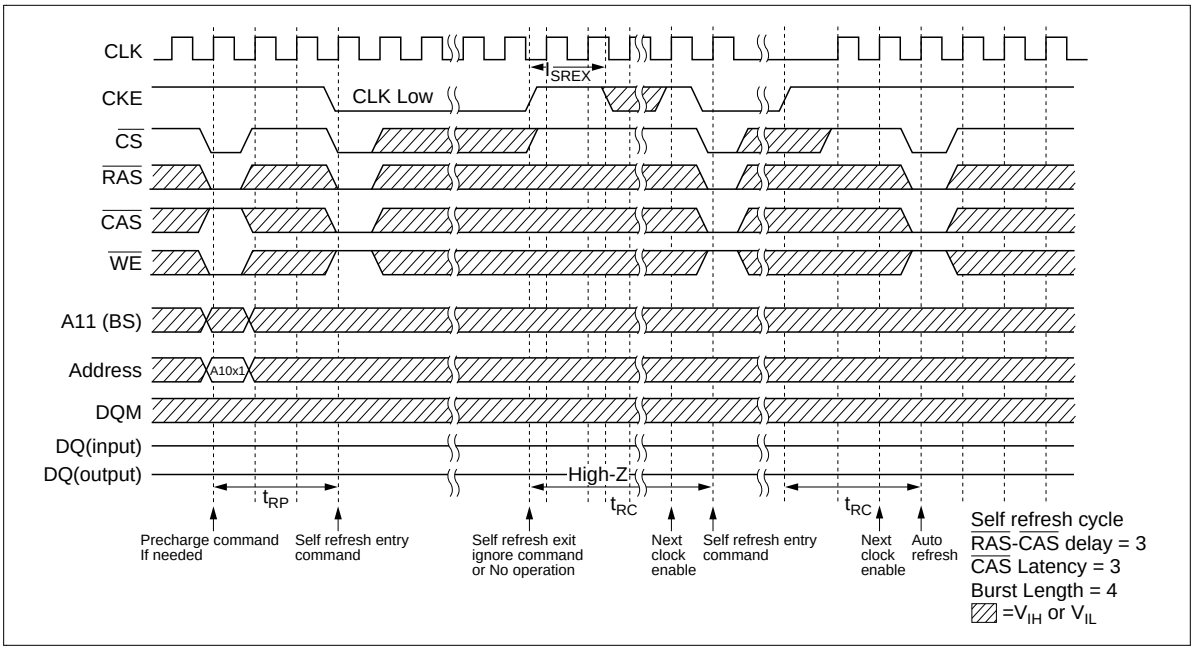
Full Page Read/Write Cycle



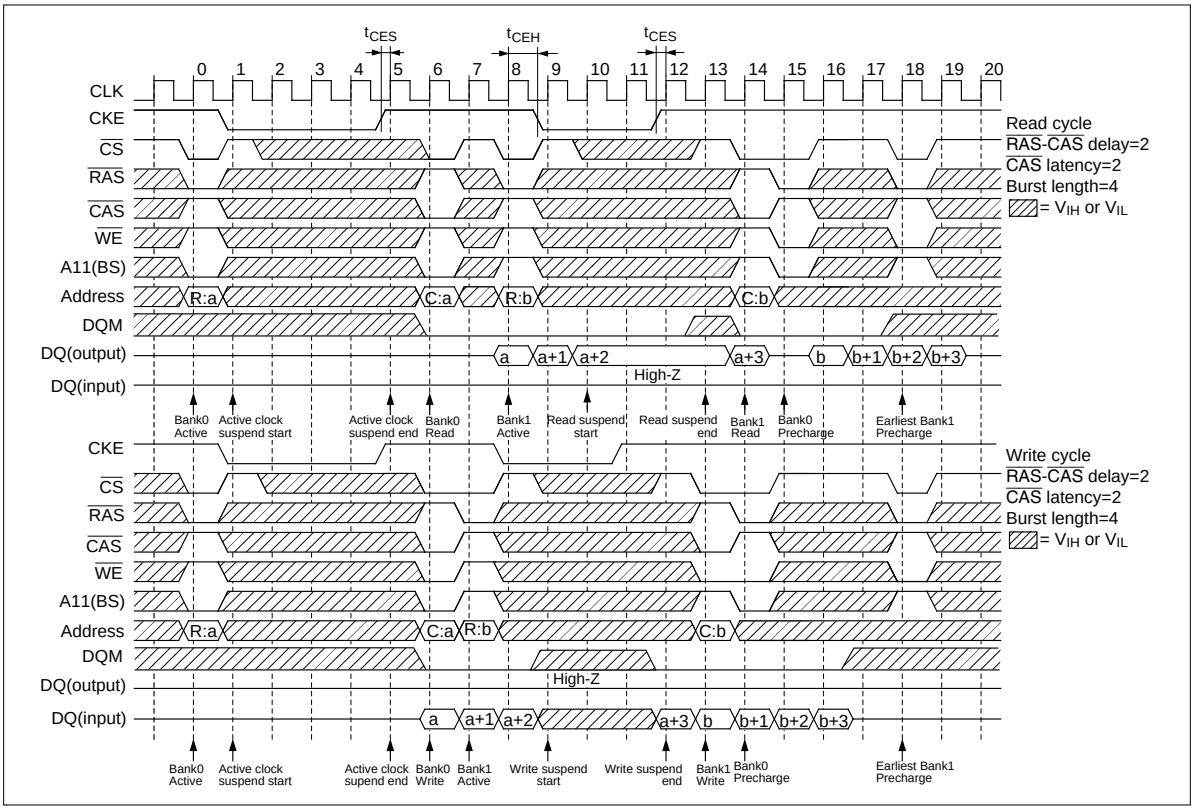
Auto Refresh Cycle



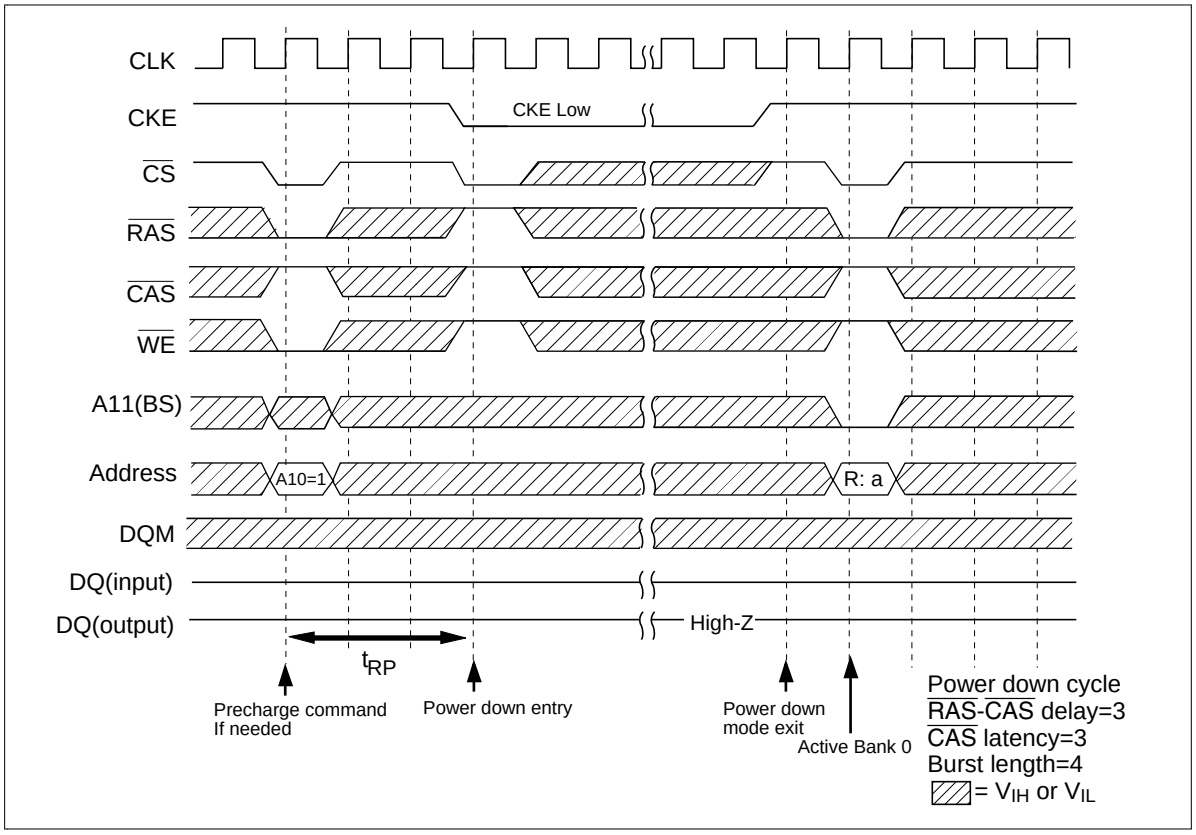
Self Refresh Cycle



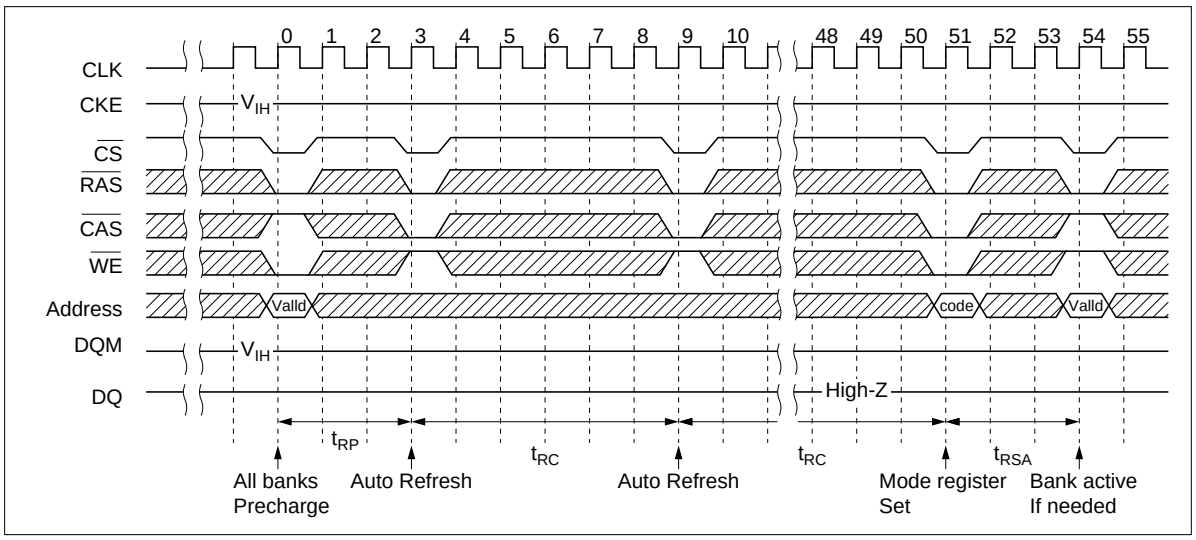
Clock Suspend Mode



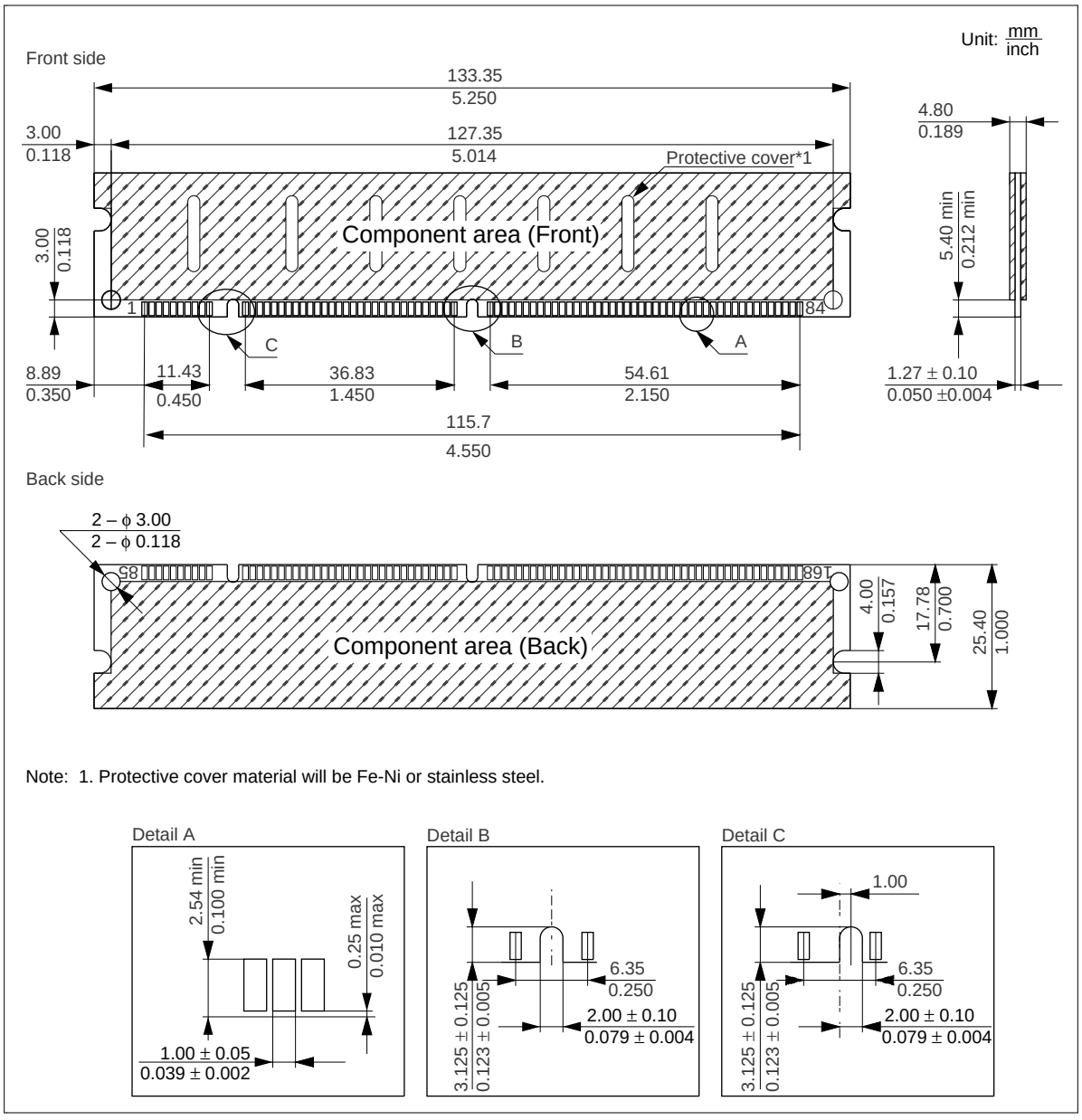
Power Down Mode



Power Up Sequence



Physical Outline



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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Oct. 8, 1996	Initial issue	T. Sugano	K. Inoue
1.1	Feb. 20, 1997	Addition of HB526R864ESN-10H Series Correct error The type number of SDRAM in Block diagram : HM5216805 to HM5216405 AC Characteristics Addition of t_{AC} (CL = 2) (HB526R864ESN-10H) max: 9.0/12 ns Change of symbol: t_{RWL} to t_{DPL}	K. Tsuneda	K. Tsuneda
2.0	Jun. 3, 1997	(referred to HM5216405/HM5216805 Series Rev.3.0) Change of Serial PD matrix AC Characteristics t_{AC} (CL = 3) max: 8/9.5 ns to 7.5/9 ns	S. Tsukui	K. Yoshizaki
3.0	Jul. 25, 1997	(referred to HM5216405/HM5216805 Series Rev.4.0) Change of Serial PD matrix AC Characteristics t_{AC} (CL = 3) max: 7.5/9 ns to 8/9.5 ns		