

T6A02/03

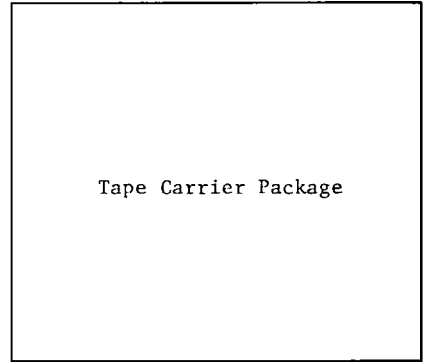
TFT-LCD GATE DRIVER

T6A02/T6A03 is a Gate Driver LSI for driving TFT-LCD Panel, which achieves high voltage operation and low power consumption.

T6A02/T6A03 enables to output a plus or a negative voltage by Level Shifter.

T6A03 is the mirror type reversed T6A02.

- . TFT-LCD Gate Driver LSI.
- . TFT-LCD controlling pins: 280 outputs(pins).
- . High Voltage Operation: TFT-LCD controlling signal $V_{SS}+27V$ (Max.).
- . T6A02 has T6A03 of the mirror type in order to facilitate LCD wiring.
- . It enables to output a negative voltage of TFT-LCD Panel controlling signals by level shifter.
- . The package is a tape carrier package (TCP).
- . TFT-LCD data drivers (T6A00/T6A01) can be used with T6A02/T6A03.



Unit : mm

T6A02 T6A03	LEAD PITCH	
	IN, I/O	OUT
(TA)	1.50	0.17

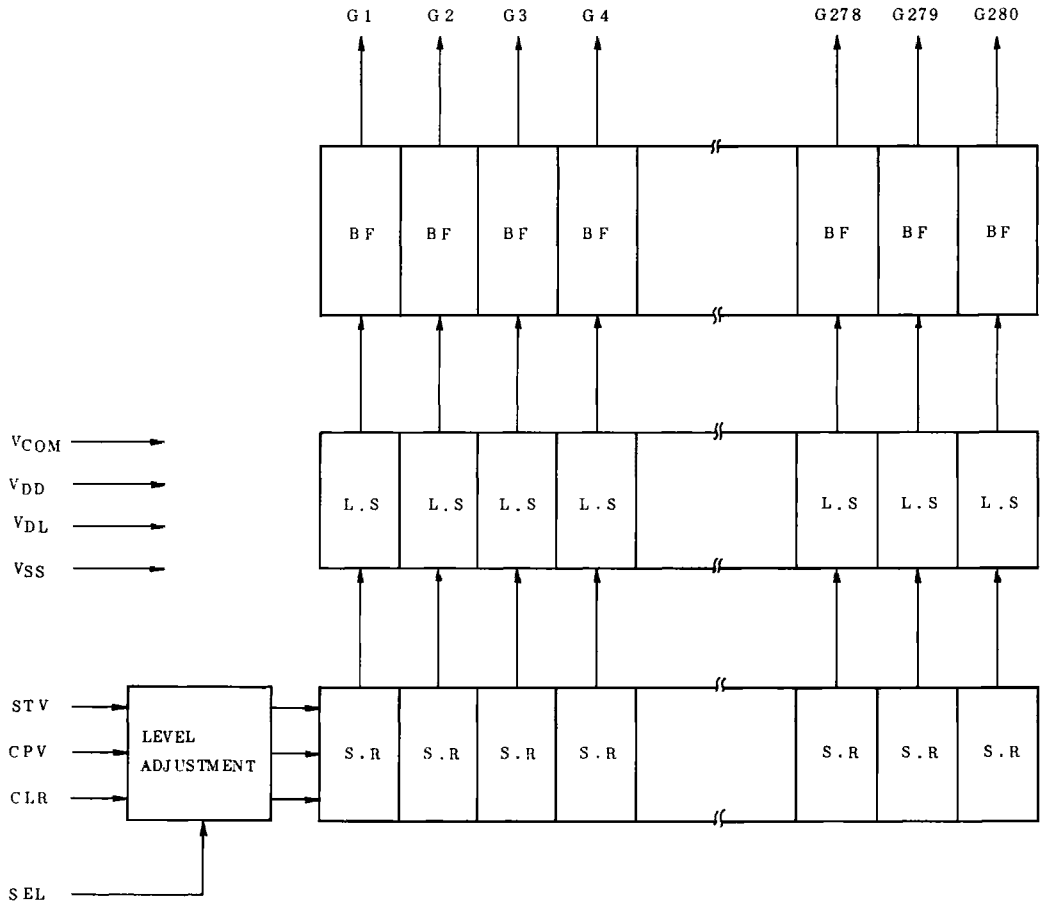
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* Refer to Packaging Outline Dimensions.

- . Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

T6A02/03

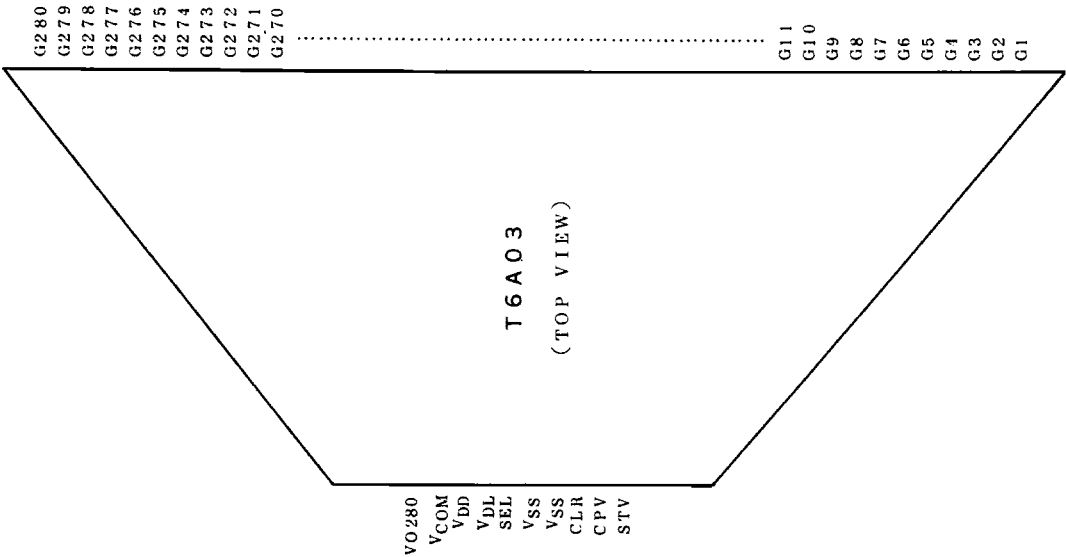
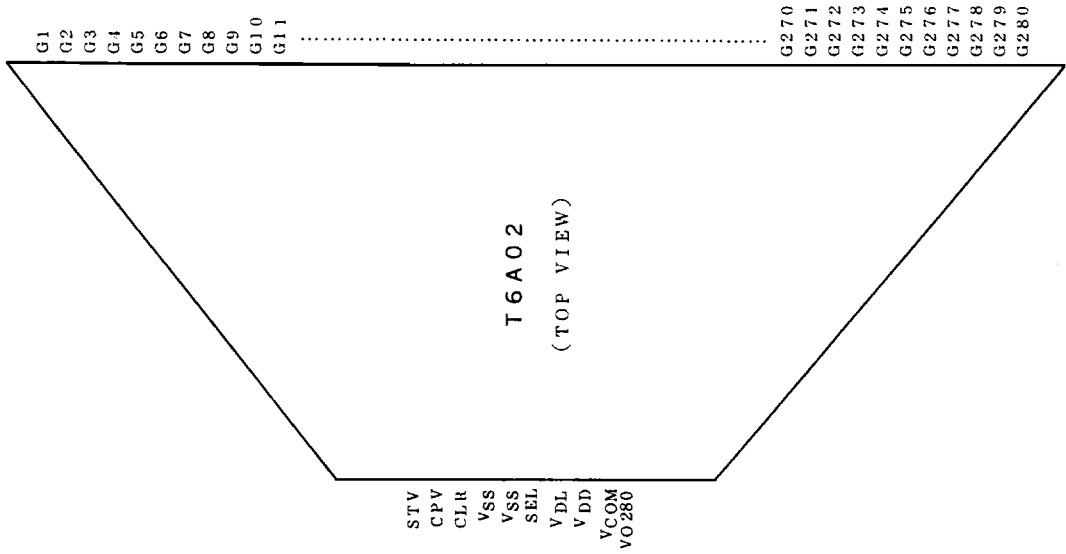
BLOCK DIAGRAM



BF : Output Circuit
 L.S : Level Shifer
 S.R : Shift Resistor

PIN FUNCTION

PIN CONFIGURATION



PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
CPV	I	Vertical Shift Clock It is a shift clock of Shift-Resistor. Data of Shift-Resistor shift synchronously to the rise of CPV.
STV	I	Vertical Shift Data input pin It is a data to input in the first Shift-Resistor and is input into a resistor synchronously to the rise of CPV.
CLR	I	Clear input pin It controls the output Pins (G1-G280) for driving TFT-LCD Panel. <ul style="list-style-type: none"> • CLR="H" : turns to L LEVEL. • CLR="L" : turns to output mode.
SEL	I	Mode Select pin This pin defines either A mode or B mode. When it is A mode, it must connect to VDL. When it is B mode, it must connect to VSS.
V _{O280}	I	Vertical Shift Data output pin In case of cascade connection, it is data to input to the next LSI. The data output synchronously to the fall of CPV.
G1-G280	I	TFT-LCD Panel Controlling Pins These pins are output the data of Shift Resistor which is changed level by Level Shifter.
VCOM	I	Power Source for driving TFT-LCD Panel.
VDD	I	Power Source for Level Shifter Circuit.
VDL	I	Power Source for Internal Logic Circuit.
VSS	I	Power Source for TFT-LCD Panel Controlling and Internal Logic Circuit.

FUNCTIONAL DESCRIPTION

. MODE SELECTION

Mode selection enabled negative voltage output of output pins (G1~G280). This is defined by mode switching pin (SEL) as follows:

A mode

This mode is output a negative voltage when output pin (G1~G280) are "L" level.

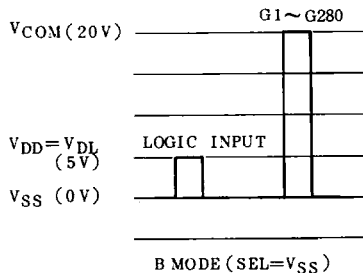
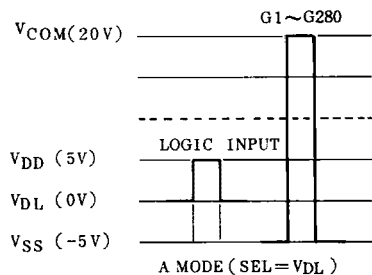
- (1) It must connect SEL to V_{DL} (power supply).
- (2) Input signals (STV, CPV, CLR) must be input a voltage from V_{SS} to V_{DD} .

* $V_{DD} = V_{DL} + 4.5 \sim V_{DL} + 5.5V$

B mode

This mode is output a positive voltage to output pins (G1~G280).

- (1) It must connect SEL to V_{SS} (power supply).
- (2) Input signals (STV, CPV, CLR) must be input a voltage from V_{SS} to $V_{DL}(=V_{DD})$.



The last data (V_{Q280}) which transfers to next LSI outputs a voltage regardless of these mode as follows:

"H" level = V_{DD}

"L" level = V_{SS}

MODE	SEL	V_{IH}/V_{IL}	OUTPUT (H/L)	V_{SS}	V_{DD}	V_{DL}	V_{COM}
A	$H(=V_{DL})$	5V/0V	20V/-5V	-5V	5V	0V	20V
B	$L(=V_{SS})$	5V/0V	20V/0V	0V	5V	5V	20V

FUNCTIONS

TFT-LCD driving pins (G1-G280) output "H" or "L" level by input signal (STV, CPV, CLR).

A data is input to Vertical shift data (STV) and it is written in the first Shift-Resistor synchronously to the rise of CPV.

It outputs as follows.

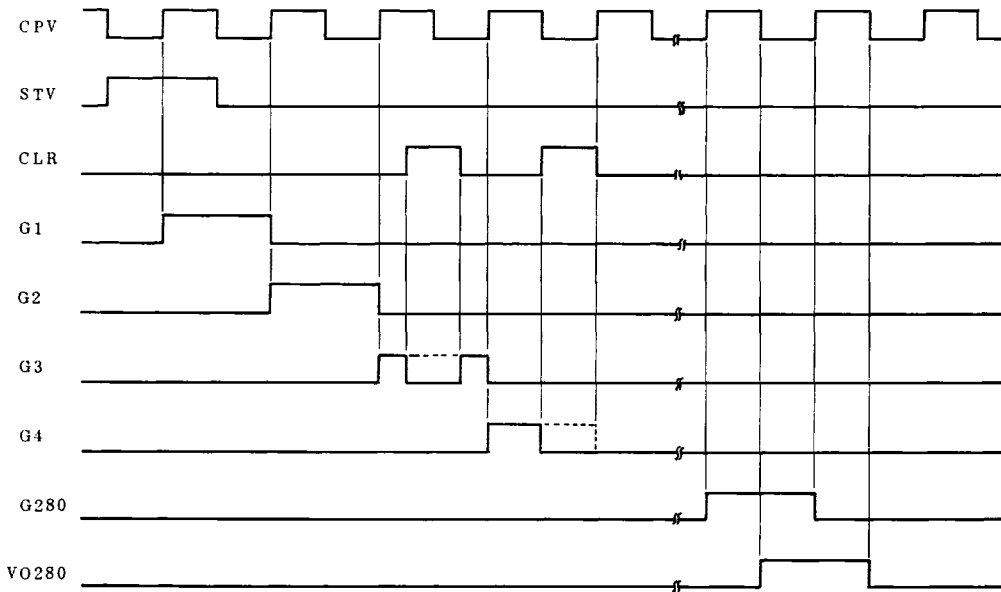
$$STV \rightarrow G1 \rightarrow G2 \rightarrow G3 \dots G278 \rightarrow G279 \rightarrow G280 \rightarrow VO280$$

The data of G280 outputs to vertical shift data (VO280) synchronously to the fall of CPV.

CLR input pin controls the output data as shown:

CLR="H" level: Output pins output "L" level regardless of the data of Shift Resistor

CLR="L" level: Output pins output ordinary data.



MAXIMUM RATINGS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT
Supply Voltage 1	V _{com}		-0.3~30	V
Supply Voltage 2	V _{DD}		-0.3~14.0	V
Supply Voltage 3	V _{DL}		-0.3~7.0	V
Input Voltage	V _{IN}		-0.3~V _{DD} +0.3	V
Storage Temperature	T _{stg}		-55~125	°C

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT	NOTE
Operating Voltage 1	V _{com}		V _{DD} ~27	V	*1
			V _{DD} ~27	V	*2
Operating Voltage 2	V _{DD}		9.0~11.0	V	*1
			4.5~5.5	V	*2
Operating Voltage 3	V _{DL}		4.5~5.5	V	*1
			4.5~5.5	V	*2
Operating Temperature	T _{op}		-20~75	°C	
Operating Frequency	f _{cp}		5~50	kHz	
Output Load Capacitance	C _L		0~300	pF	Each output pins

*1 A mode ... SEL=V_{DL}

*2 B mode ... SEL=V_{SS}

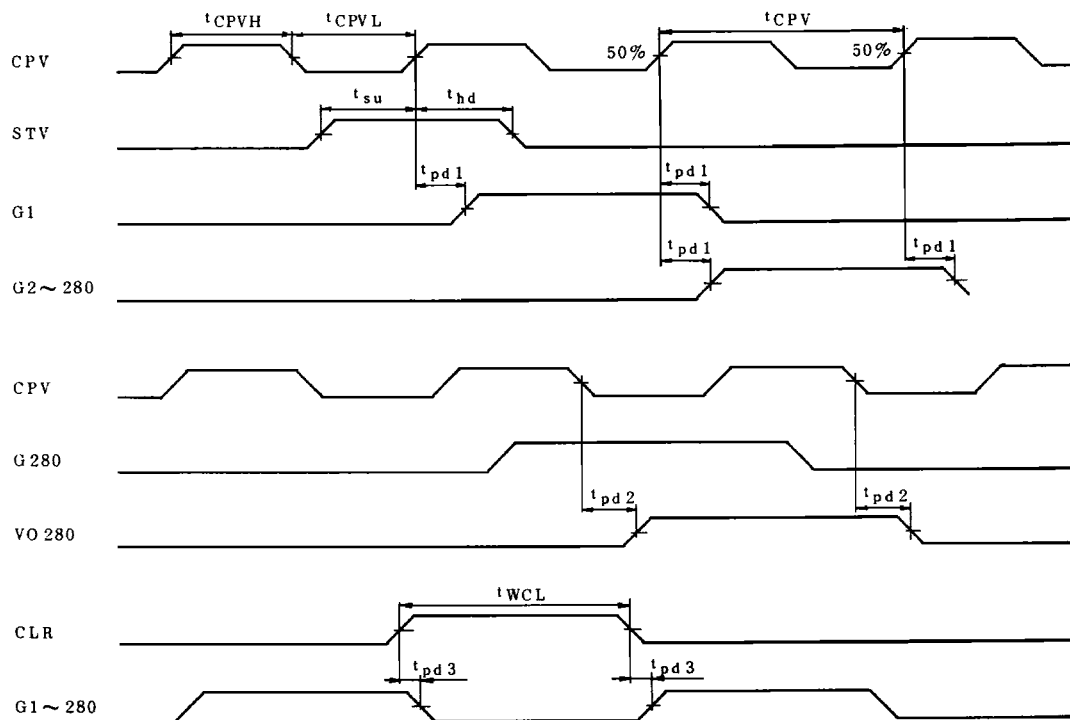
DC CHARACTERISTICS

(Unless otherwise specified, $T_a = -20 \sim 75^\circ\text{C}$, $V_{com} = V_{SS} + 20\text{V}$, $V_{DD} = 9.0 \sim 11.0\text{V}$ (A-mode) / $4.5 \sim 5.5\text{V}$ (B-mode), $V_{DL} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	APPLY PINS
Input "L" Level	V_{IL}	A mode	V_{SS}	-	$V_{DD} - 3.6$	V	*1
Input "H" Level	V_{IH}	A mode	$V_{DD} - 1.2$	-	V_{DD}	V	*1
Input "L" Level	V_{IL}	B mode	V_{SS}	-	$0.2 \times V_{DD}$	V	*1
Input "H" Level	V_{IH}	B mode	$0.8 \times V_{DD}$	-	V_{DD}	V	*1
Output "L" Level	V_{OL}	$I_{OL} = 40\mu\text{A}$	V_{SS}	-	$V_{SS} + 0.3$	V	V_{O280}
Output "H" Level	V_{OH}	$I_{OH} = -40\mu\text{A}$	$V_{DD} - 0.3$	-	V_{DD}	V	V_{O280}
Output "L" Reference	R_{OL}	$V_{OUT} = 0.5\text{V}$	-	-	1500	Ω	G1~G280
Output "H" Reference	R_{OH}	$V_{OUT} = 19.5\text{V}$	-	-	1500	Ω	G1~G280
Input Voltage	I_{in}		-1.0	-	1.0	μA	All Input Pins
Current Consumption 1	I_{DD}		-	-	200	μA	
Current Consumption 2	I_{DL}		-	-	50	μA	
Current Consumption 3	I_{com}		-	-	100	μA	

*1 All Input pins expected of SEL.

AC CHARACTERISTICS



(Unless otherwise specified, $T_a = -20 \sim 75^\circ\text{C}$, $V_{com} = V_{SS} + 20\text{V}$,
 $V_{DD} = 9.0 \sim 11.0\text{V}$ (A-mode) / $4.5 \sim 5.5\text{V}$ (B-mode), $V_{DL} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$
 Rising and falling time = 6ns (all input signals))

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Operating Frequency	tCPV		20	-	μs
CPV Pulse Width (H/L)	tCPVH, tCPVL		10	-	μs
CLR Enable Time	tWCL		1	-	μs
Data Set Up Time	tSU		700	-	ns
Data Hold Time	tHD		700	-	ns
Output Delay Time 1	tPD1	$C_L = 300\text{pF}$	-	800	ns
Output Delay Time 2	tPD2		-	1000	ns
Output Delay Time 3	tPD3	$C_L = 300\text{pF}$	-	800	ns