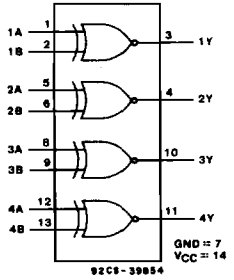
CD54/74HC7266

File Number **1780**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Exclusive-NOR Gate

Type Features:

- *Four independent Exclusive-NOR gates*
- *Buffered inputs and outputs*

Applications

- *Logical comparators*
- *Parity generators and checkers*
- *Adders/Subtracters*

The RCA CD54/74HC7266 contains four independent EXCLUSIVE-NOR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-NOR function.

This device is functionally the same as the TTL226. They differ in that the HC7266 has active high and low outputs whereas the 226 has open collector outputs.

The CD54HC7266 is supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC7266 is supplied in 14-lead plastic dual-in-line package (E suffix), in a 14-lead dual-in-line surface-mount plastic package (M-suffix), and is also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *2 to 6 V Operation*
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CMOS Input Compatibility*
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

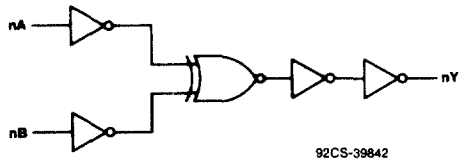


Fig. 1 - Logic diagram each gate.

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level.
L = LOW voltage level.

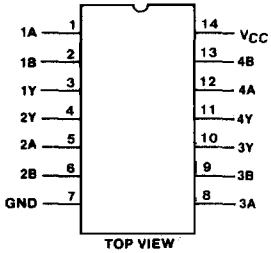
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*	2	6	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: CD74 Types CD54 Types	 -40 -55	 +85 +125	°C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	 0 0 0	 1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC7266

STATIC ELECTRIC CHARACTERISTICS

CHARACTERISTIC		CD54/74HC7266										UNITS
		TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		
					+25°C			-40/ +85°C		-55/ +125°C		
		V_I V	I_O mA	V_{CC} V	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}			2	1.5	—	—	1.5	—	1.5	—	V
				4.5	3.15	—	—	3.15	—	3.15	—	
				6	4.2	—	—	4.2	—	4.2	—	
Low-Level Input Voltage	V_{IL}			2	—	—	0.5	—	0.5	—	0.5	V
				4.5	—	—	1.35	—	1.35	—	1.35	
				6	—	—	1.8	—	1.8	—	1.8	
High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V
				4.5	4.4	—	—	4.4	—	4.4	—	
				6	5.9	—	—	5.9	—	5.9	—	
TTL Loads		V_{IL} or	-4	4.5	3.98	—	—	3.84	—	3.7	—	V
		V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	
Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V
				4.5	—	—	0.1	—	0.1	—	0.1	
				6	—	—	0.1	—	0.1	—	0.1	
TTL Loads		V_{IL} or	4	4.5	—	—	0.26	—	0.33	—	0.4	V
		V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	
Input Leakage Current	I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	μA
				—	—	—	—	—	—	—	—	
Quiescent Device Current	I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL VALUES 54/74HC	UNITS
Propagation Delay, Any Input	t_{PLH} t_{PHL}	15	9	ns
*Power Dissipation Capacitance**	C_{PD}	—	33	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD}+C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C HC		-40°C to +85°C 74HC		-55°C to +125°C 54HC		UNITS
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}, t_{PHL}	2	—	115	—	145	—	150	ns
		4.5	—	23	—	29	—	35	
		6	—	30	—	25	—	30	
Output Transition Time	t_{TLH}, t_{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C_I	—	—	10	—	10	—	10	pF

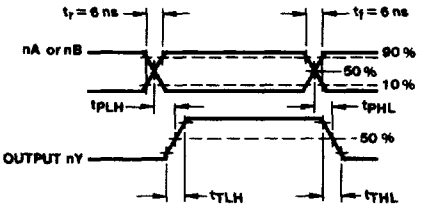


Fig. 2 - Transition times and propagation delay times.