Features

- CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- High-volume replacement for EP1810/EP1800 EPLD designs
- Zero-power operation (typically 10 µA standby)
- Active power of 10 mA at 20 MHz
- High speed (t_{PD} = 25 ns) with 50-MHz clock rates
- TTL and CMOS I/O compatibility
- MAX+PLUS II and A+PLUS development system support, featuring schematic capture, Boolean equation, state machine, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and functional and timing simulation (AHDL, waveform design entry, and timing simulation available only in MAX+PLUS II software)
- Available in a plastic 68-pin J-lead chip carrier (PLCC) package

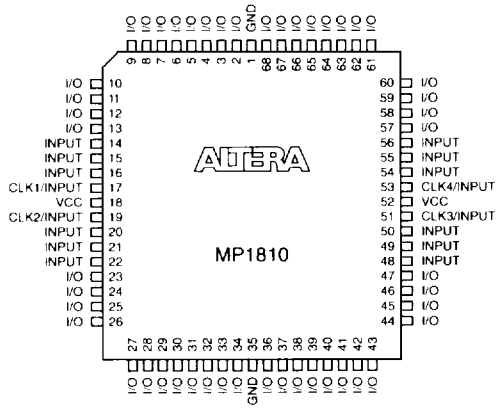
General Description

Altera's MP1810 MPLD provides a high-volume replacement for EP1810/EP1800 designs. It is pin-, function- and timing-compatible with existing EP1810/EP1800 designs. MP1810 designs are created with Altera's MAX+PLUS II or A+PLUS development system and prototyped with EP1810 EPLDs. The source files are then converted to produce the MPLD. The MP1810 MPLD is available in a 68-pin PLCC package. See Figure 3.

This data sheet provides minimum and maximum AC and DC parametric values for the MP1810 MPLD. For additional information, refer to the *EP1810 EPLDs: High-Performance 48-Macrocell Devices Data Sheet* in this data book.

Figure 3. MP1810 Package Pin-Out Diagram

Package outline not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			50	ns
t_F	Input fall time			50	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load		10		µA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *See Note (4)*		0.5		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions *See Note (3)*

External Timing Parameters			MP1810-25		MP1810-35		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		35	ns
t_{PD2}	I/O input to non-registered output			28		40	ns
t_{SU}	Global clock setup time		17		25		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		18		20	ns
t_{CH}	Global clock high time		10		12		ns
t_{CL}	Global clock low time		10		12		ns
t_{ASU}	Array clock setup time		10		10		ns
t_{AH}	Array clock hold time		10		15		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		35	ns
t_{CNT}	Minimum global clock period			25		35	ns
f_{CNT}	Maximum internal frequency	*See Note (4)*	40		28.6		MHz
f_{MAX}	Maximum clock frequency	*See Note (5)*	50		40		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.

(3) Operating conditions: $V_{CC} = 5$ V ± 5%, $T_A = 0°$ C to 70° C for commercial use.

(4) Measured with a device programmed as four 12-bit counters.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 4 shows typical supply current versus frequency for MP1810 MPLDs.

Figure 4. MP1810 I_{CC} vs. Frequency