80C51BH/80C31BH/80C52T2/80C32T2

CMOS Single-Chip Microcontrollers

DISTINCTIVE CHARACTERISTICS

- Industry Standard CMOS Microcontrollers
- Low Power Modes—Idle & Power-Down
- 32 Programmable I/O Lines
- Two 16-bit Counter/Timers
- Programmable Serial Channel
  - Five-source, two-level Interrupt Structure
  - Boolean Processor
- 64K bytes Program Memory Space
- 64K bytes Data Memory Space

	RAM (bytes)	ROM (bytes)
80C31BH	128	—
80C51BH	128	4K
80C32T2	256	—
80C52T2	256	8K

80C51BH = 80C31BH + 4K bytes ROM
80C52T2 = 80C32T2 + 8K bytes ROM

GENERAL DESCRIPTION

The 80C51BH and 80C31BH are CMOS versions of the industry-standard 8051 architecture. The 80C52T2 and 80C32T2 are identical products except they contain double the on-chip memory.

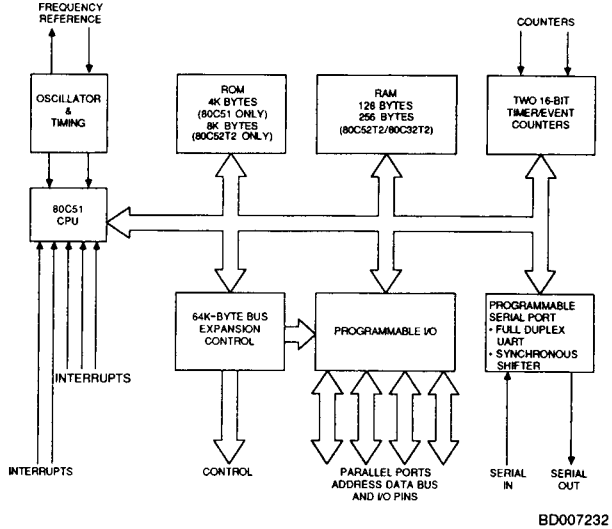
Both the 80C51BH and 80C31BH include 128 bytes of RAM, while the 80C52T2 and 80C32T2 include 256 bytes of RAM. The 80C51BH also includes 4K bytes of custom ROM program memory and the 80C52T2 includes 8K bytes of ROM. The 80C52T2 and 80C32T2 are CMOS equivalents to the 8052AH and 8032AH except they contain two timers (T2) instead of three.

These CMOS products retain all of the features of their NMOS counterparts: 32 I/O lines; two 16-bit counter/timers; a full-duplex serial port; a five-source, two-level interrupt structure; and an on-chip oscillator and clock circuits.

In addition, all CMOS 80C51-based products have two software-selectable modes of reduced activity for further power conservation—Idle and Power-Down. In the Idle mode, the CPU is frozen while the RAM, timers, serial port, and interrupt system continue to function. In the Power-Down mode, the RAM is saved and all other functions are inoperative.

The 80C52T2 and 80C32T2 in PLCC packages offer improved noise tolerance by utilizing previously unused pins for additional V_{CC} and V_{SS} connections.

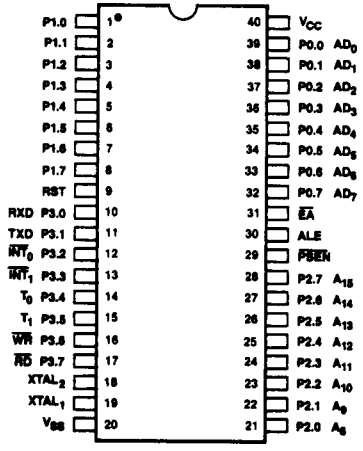
BLOCK DIAGRAM



BD007232

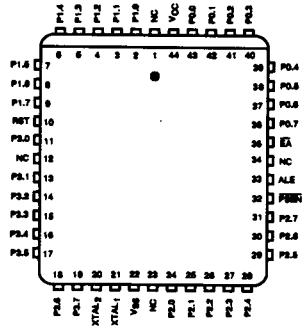
CONNECTION DIAGRAMS
Top View

DIP
80C51BH/80C31BH
80C52T2/80C32T2



CD005554

PLCC
80C51BH/80C31BH



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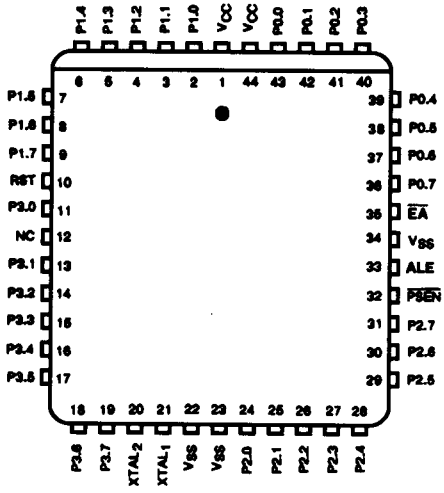
PLCC

80C52T2/80C32T2



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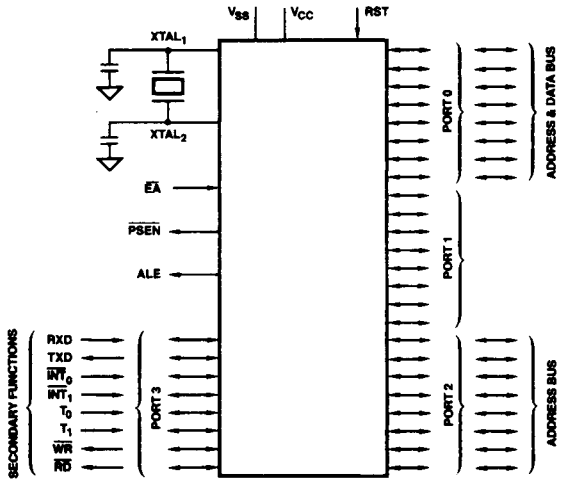
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



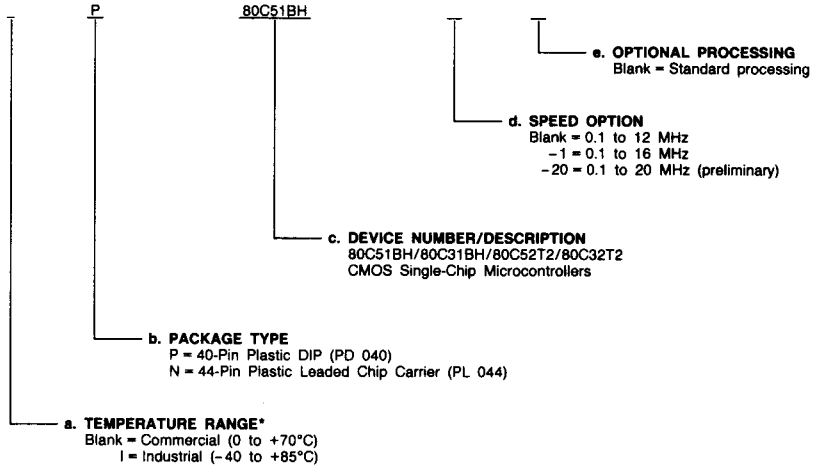
LS001323

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Temperature Range
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
P, N IP, IN	80C51BH
	80C51BH-1
	80C31BH
	80C31BH-1
P	80C31BH-20
P, N IP, IN	80C52T2-1
	80C32T2-1

*This device will also be available in Military temperature range.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Port 0 (Bidirectional, Open Drain)

Port 0 is an open-drain bidirectional I/O port. Port 0 pins that have 1s wriiten to them float, and in that state can allow them to be used as high-impedance inputs.

Port 0 is also the multiplexed Low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 80C51BH. External pullups are required during program verification.

Port 1 (Bidirectional)

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four LS TTL inputs. Port 1 pins that have 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 1 pins that are externally being pulled Low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 1 also receives the Low-order address bytes during program verification.

Port 2 (Bidirectional)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four LS TTL inputs. Port 2 pins having 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 2 pins externally being pulled Low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the High-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function register.

Port 2 also receives the High-order address bits during ROM verification.

Port 3 (Bidirectional)

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four LS TTL inputs. Port 3 pins that have 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 3 pins externally being pulled Low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features as listed below:

Port Pin	Alternate Function
$P_{3.0}$	RxD (serial input port)
$P_{3.1}$	TxD (serial output port)
$P_{3.2}$	$\overline{INT_0}$ (external interrupt 0)
$P_{3.3}$	$\overline{INT_1}$ (external interrupt 1)
$P_{3.4}$	T_0 (Timer 0 external input)
$P_{3.5}$	T_1 (Timer 1 external input)
$P_{3.6}$	$\overline{WR}$ (external Data Memory write strobe)
$P_{3.7}$	$\overline{RD}$ (external Data Memory read strobe)

RST Reset (Input, Active High)

A High on this pin (for two machine cycles while the oscillator is running) resets the device. An internal diffused resistor to V_{SS} permits power-on reset, using only an external capacitor to V_{CC}.

ALE Address Latch Enable (Output, Active High)

Address Latch Enable is the output pulse for latching the Low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, allowing use for external-timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$ Program Store Enable (Output, Active Low)

$\overline{PSEN}$ is the read strobe to external Program Memory. When the 80C51BH is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle—except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal Program Memory.

$\overline{EA}$ External Access Enable (Input, Active Low)

$\overline{EA}$ must be externally held Low to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. If $\overline{EA}$ is held High, the device executes from internal Program Memory unless the program counter contains an address greater than 0FFFH.

$XTAL_1$ Crystal (Input)

Input to the inverting-oscillator amplifier, and input to the internal clock-generator circuits.

$XTAL_2$ Crystal (Output)

Output from the inverting-oscillator amplifier.

V_{CC} Power Supply

Supply voltage during normal, idle, and power-down operations.

V_{SS} Circuit Ground

FUNCTIONAL DESCRIPTION

Oscillator Characteristics

$XTAL_1$ and $XTAL_2$ are the input and output, respectively, of an inverting amplifier which is configured for use as an on-chip oscillator (see Figure 1). Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, $XTAL_1$ should be driven while $XTAL_2$ is left unconnected (see Figure 2). There are no requirements on the duty cycle of the external-clock signal since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum High and Low times specified on the data sheet must be observed.

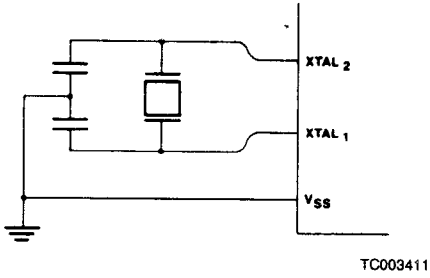


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Figure 1. Crystal Oscillator

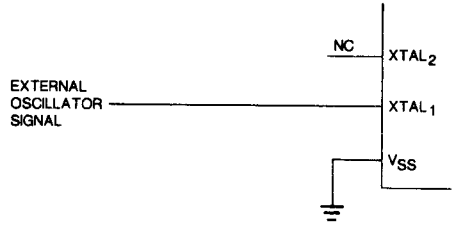

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Figure 2. External Drive Configuration

Note: Different from NMOS configuration.

Idle and Power-Down Operation

Figure 3 shows the internal Idle and Power-Down clock configuration. As illustrated, Power-Down operation freezes the oscillator. Idle mode operation shows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is halted.

These special modes are activated by software via the Special Function Register, PCON (Table 1). Its hardware address is 87H; PCON is not bit-addressable.

If 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is "0XXX0000."

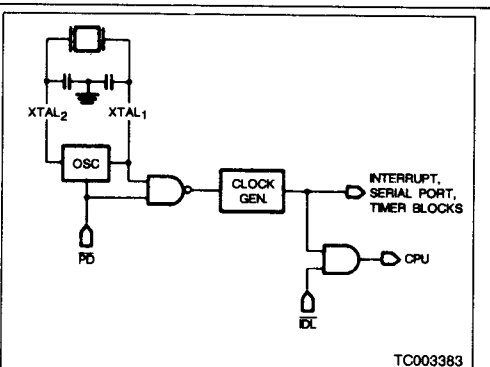

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Figure 3. Idle and Power-Down Hardware

TABLE 1. PCON (Power Control Register)

(MSB)							(LSB)
SMOD	-	-	-	GF1	GF0	PD	IDL

Symbol	Position	Name and Description
SMOD	PCON.7	Double-baud-rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2, or 3.
-	PCON.6	(Reserved)
-	PCON.5	(Reserved)
-	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit
GF0	PCON.2	General-purpose flag bit
PD	PCON.1	Power-Down bit. Setting this bit activates power-down operation.
IDL	PCON.0	Idle-mode bit. Setting this bit activates idle-mode operation.

Idle Mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other registers maintain their data during Idle. Table 2 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote a 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the

hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Power-Down Mode

The instruction that sets PCON.1 is the last executed prior to going into Power-Down. Once in Power-Down, the oscillator is stopped. Only the contents of the on-chip RAM are preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the Power-Down mode.

In the Power-Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the Power-Down mode is entered, and that the voltage is restored before the hardware reset is applied, which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 2 describes the status of the external pins while in the Power-Down mode. It should be noted that if the Power-Down mode is activated while in external program memory, the port data that is held in the Special Function Register P_2 is restored to Port 2. If the data is a 1, the port pin is held High during the Power-Down mode by the strong pullup, P_1, shown in Figure 4.

80C51BH I/O Ports

The I/O port drive of the 80C51BH is similar to the 8051. The I/O buffers for Ports 1, 2, and 3 are implemented as shown in Figure 4.

When the port latch contains a 0, all pFETS in Figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, P_1, turns on for two oscillator periods, pulling the output High very rapidly. As the output line is drawn High, pFET P_3 turns on through the inverter to supply the I_{OH} source current. This inverter and P_3 form a latch which holds the 1 and is supported by P_2.

When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have its strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as I_{TL} under the D.C. Specifications. When the input goes below approximately 2 V, P_3 turns off to save I_{CC} current. Note, when returning to a logical 1, P_2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line High.

TABLE 2. STATUS OF THE EXTERNAL PINS DURING IDLE AND POWER-DOWN MODES

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power-Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power-Down	External	0	0	Floating	Port Data	Port Data	Port Data

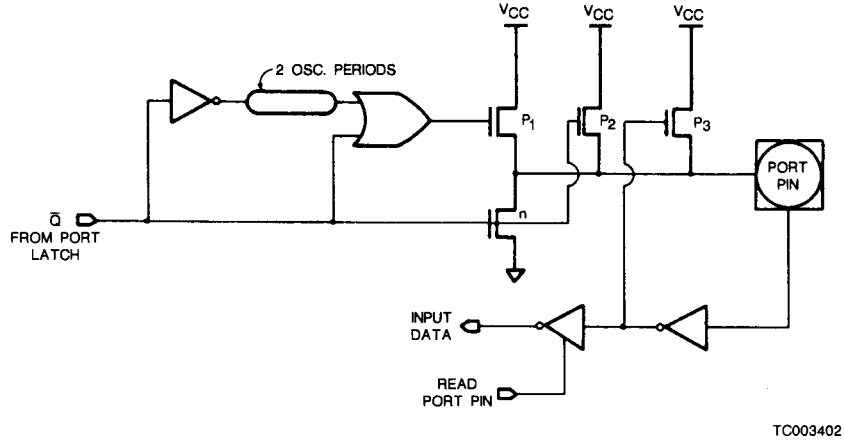


Figure 4. I/O Buffers in the 80C51BH (Ports 1, 2, 3)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Voltage on Any
Pin to V_{SS} ..... −0.5 V to V_{CC} +0.5 V
Voltage on V_{CC} to V_{SS} ..... −0.5 V to 6.5 V
Power Dissipation ..... 200 mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
80C51BH/80C31BH
Supply Voltage (V_{CC}) ..... +4 V to +6 V
80C52T2/80C32T2
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Ground (V_{SS}) ..... 0 V

Industrial (I) Devices
Temperature (T_A) ..... −40 to +85°C
80C51BH/80C31BH
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
80C52T2/80C32T2
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input Low Voltage (Except $\overline{EA}$)		−0.5	.2 V_{CC} − 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		−0.5	.2 V_{CC} − 0.3	V
V_{IH}	Input High Voltage (Except $XTAL_1$, RST)		0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage ($XTAL_1$ RST)		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)	I_{OL} = 1.6 mA (Note 1)		0.45	V
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA (Note 1)		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3)	I_{OH} = −60 μA, V_{CC} = 5 V±10%	2.4		V
		I_{OH} = −25 μA	0.75 V_{CC}		V
		I_{OH} = −10 μA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	I_{OH} = −400 μA, V_{CC} = 5 V±10%	2.4		V
		I_{OH} = −150 μA	0.75 V_{CC}		V
		I_{OH} = −40 μA (Note 2)	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45 V		−50	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2 V		−650	μA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	μA
RRST	Reset Pulldown Resistor		50	150	kΩ
CIO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{PD}	Power Down Current	V_{CC} = 2 to 6 V (Note 3)		50	μA

80C51BH/80C31BH MAXIMUM I_{CC} (mA)

	Operating (Note 4)			Idle (Note 5)		
Freq. V_{CC}	4 V	5 V	6 V	4 V	5 V	6 V
0.1 MHz	1.2	1.5	2.5	0.5	0.7	1.1
3.5 MHz	4.3	5.7	7.5	1.1	1.6	2.2
8.0 MHz	8.3	11	14	1.8	2.7	3.7
12 MHz	12	16	20	2.5	3.7	5
16 MHz	16	20.5	25	3.5	5	6.5

80C52T2/80C32T2 MAXIMUM I_{CC} (mA)

	Operating (Note 4)			Idle (Note 5)		
Freq. V_{CC}	4.5 V	5.0 V	5.5 V	4.5 V	5.0 V	5.5 V
0.1 MHz	2.2	3.1	3.8	0.7	0.9	1.4
3.5 MHz	6	8	10	1.5	2	3
8.0 MHz	11	14	18	2.5	3.5	5
12 MHz	15	20	25	3.5	5	6
16 MHz	19	25	32	4.5	6.5	8.5

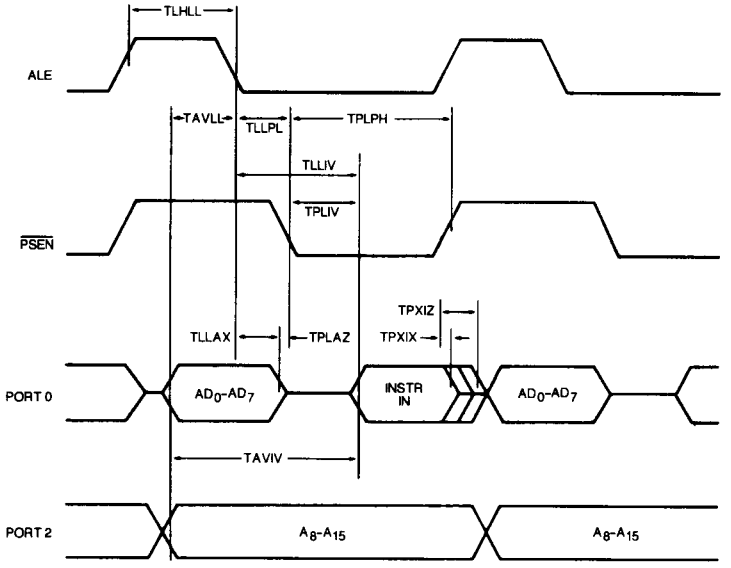
Notes: 1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}S of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt-Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall before the .9 V_{CC} specification when the address bits are stabilizing.
3. Power-Down I_{CC} is measured with all outputs pins disconnected: $\overline{EA}$ = Port 0 = V_{CC}; $XTAL_2$ N.C.; RST = V_{SS}.
4. I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; $XTAL_2$ NC; $\overline{EA}$ = RST = Port 0 = V_{CC}.
I_{CC} would be slightly higher if a crystal oscillator is used.
5. Idle I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; $XTAL_2$ NC; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS}.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

(C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Other Outputs = 80 pF)

Parameter Symbol	Parameter Description	20 MHz		16-MHz Osc.		12-MHz Osc.		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
External Program and Data Memory Characteristics										
1/TCLCL	Oscillator Frequency	0.1	20	0.1	16	0.1	12	0.1	16	MHz
TLHLL	ALE Pulse Width	60		85		127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	20		7		28		TCLCL−55		ns
TLLAX	Address Hold After ALE Low	15		27		48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr. In		120		150		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	25		22		43		TCLCL−40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	115		142		205		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr. In		75		83		145		3TCLCL−105	ns
TPXIX	Input Instr. Hold After $\overline{PSEN}$	0		0		0		0		ns
TPXIZ	Input Instr. Float After $\overline{PSEN}$		35		38		59		TCLCL−25	ns
TAVIV	Address to Valid Instr. In		165		208		312		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		0		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	200		275		400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	200		275		400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		145		148		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		60		55		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		310		350		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		350		398		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	137	238	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to Read or Write Low	110		120		203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	95		2		23		TCLCL−60		ns
TQVWH	Data Valid to Write High	200		287		433		7TCLCL−150		ns
TWHQX	Data Hold After $\overline{WR}$	25		12		33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	20	70	22	103	43	123	TCLCL−40	TCLCL+40	ns

SWITCHING WAVEFORMS



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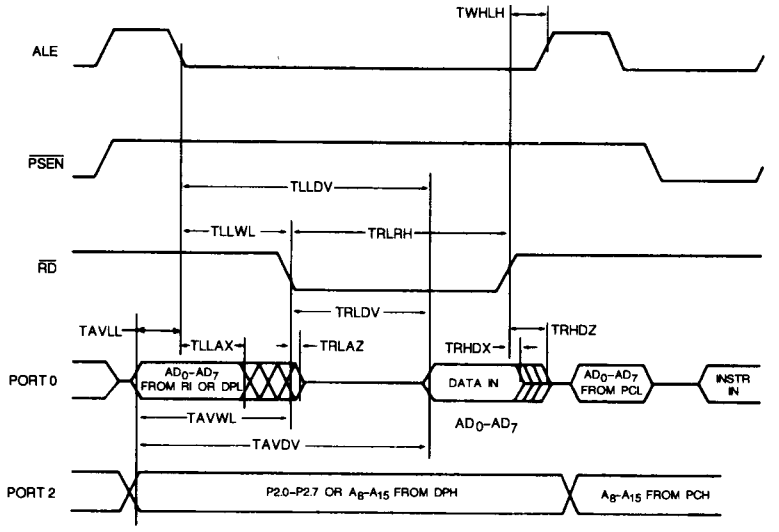
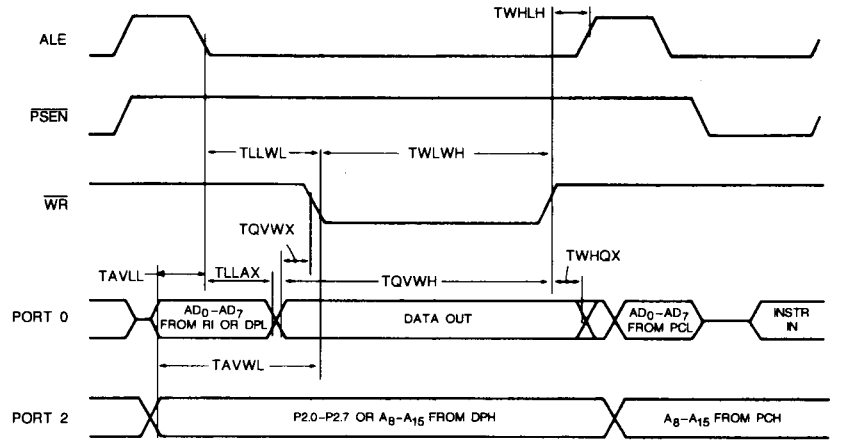
External Program Memory Read Cycle



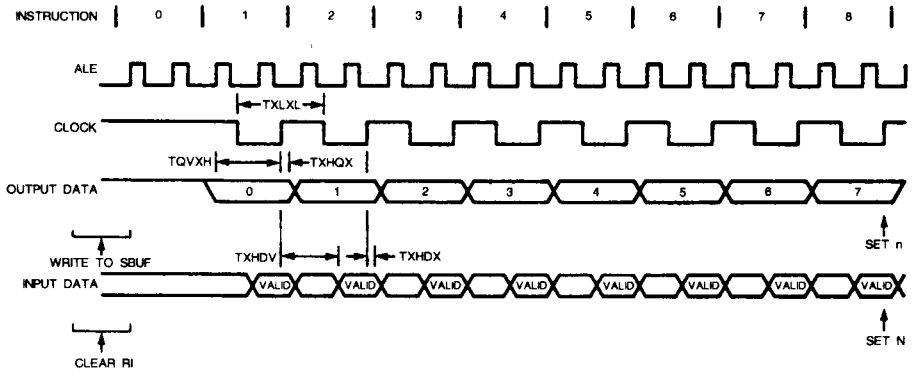
WF020962

External Data Memory Read Cycle



WF020932

External Data Memory Write Cycle

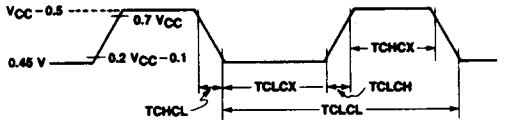


WF020951

Shift Register Timing Waveforms

EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Units
1/TCLCL	Oscillator Frequency	0.1	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



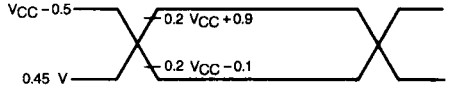
WF020910

External Clock Drive Waveform

SERIAL PORT TIMING — SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to 70°C; V_{CC} = 5 V ±20%; V_{SS} = 0 V; Load Capacitance = 80 pF

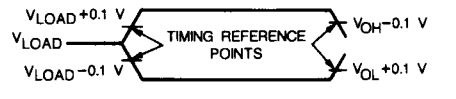
Parameter Symbol	Parameter Description	16 MHz Osc.		Variable Oscillator		Units
		Min.	Max.	Min.	Max.	
TXLXL	Serial Port Clock Cycle Time	750		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	492		10TCLCL - 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	8		2TCLCL - 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		492		10TCLCL - 133	ns



WF020901

AC inputs during testing are driven at V_{CC} - 0.5 for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

AC Testing Input/Output Waveforms



WF020941

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV chance from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Float Waveform