



M.S.KENNEDY CORP.

# HIGH SPEED/VOLTAGE OP AMP

# 1461

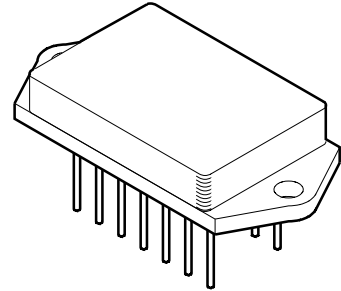
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**FEATURES:**

- Extremely Fast - 500v/ $\mu$ S
- Wide Supply Range  $\pm 15V$  to  $\pm 45V$
- VMOS Output, No Secondary Breakdown
- Large Gain-Bandwidth Product
- FET Input
- Electrically Isolated Case
- 800mA Typical Output Current
- Available as SMD#5962-9050001 HX

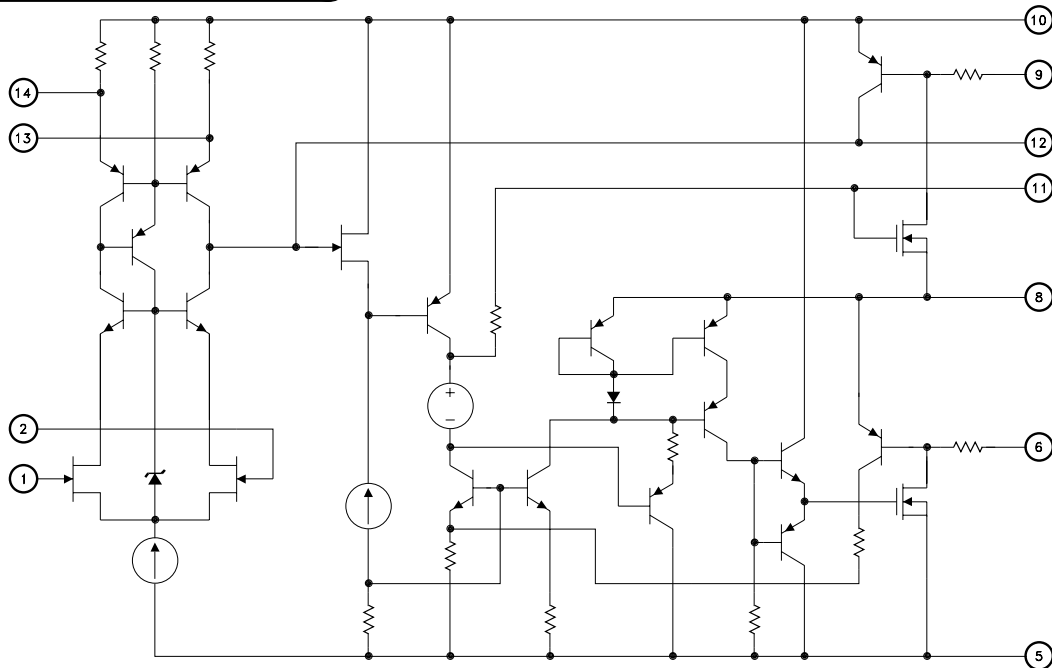
**MIL-PRF-38534 CERTIFIED**



**DESCRIPTION:**

The MSK 1461 is a state of the art high speed FET input operational amplifier. The distinguishing characteristic of the MSK 1461 is its unique VMOS output stage which completely eliminates the safe operating area restrictions associated with secondary breakdown of bipolar transistor output stage op-amps. Freedom from secondary breakdown allows the 1461 to handle large output currents at any voltage level limited only by transistor junction temperature. 115 dB of open loop gain gives the 1461 high closed loop gain accuracy and the typical  $\pm 1.0mV$  of input offset voltage will fit well in any error budget. A 500 V/ $\mu$ S slew rate and 1200 MHz gain bandwidth product make the 1461 an outstanding high-speed op-amp. A single external capacitor is used for compensation and output current limiting is user programmable through the selection of two external resistors.

**EQUIVALENT SCHEMATIC**



**TYPICAL APPLICATIONS**

- Video Yoke Drivers
- Video Distribution Amplifiers
- High Accuracy Audio Amplification
- High Speed ATE Pin Drivers

**PIN-OUT INFORMATION**

- |                          |                          |
|--------------------------|--------------------------|
| 1 Inverting Input        | 14 Offset Adjust         |
| 2 Non-Inverting Input    | 13 Offset Adjust         |
| 3 No Connection          | 12 Compensation          |
| 4 No Connection          | 11 Compensation          |
| 5 Negative Power Supply  | 10 Positive Power Supply |
| 6 Negative Current Limit | 9 Positive Current Limit |
| 7 No Connection          | 8 Output                 |

## ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	Supply Voltage	$\pm 45V$
$I_{OUT}$	Output Current	800mA
$V_{IN}$	Differential Input Voltage	$\pm 25V$
$T_{ST}$	Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

$T_{LD}$	Lead Temperature Range (10 Seconds)	$300^{\circ}C$
$T_C$	Case Operating Temperature (MSK 1461B/E)	$-55^{\circ}C$ to $+125^{\circ}C$
	(MSK 1461)	$-40^{\circ}C$ to $85^{\circ}C$
$T_J$	Junction Temperature	$+175^{\circ}C$

## ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions	Group A Subgroup	MSK 1461B/E			MSK 1461			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>STATIC</b>									
Supply Voltage Range ③		-	$\pm 15$	-	$\pm 45$	$\pm 15$	-	$\pm 45$	V
Quiescent Current	$V_{IN} = 0V$	1	-	$\pm 19$	$\pm 25$	-	$\pm 19$	$\pm 28$	mA
		2,3	-	$\pm 21$	$\pm 35$	-	-	-	mA
Thermal Resistance ③	Junction to Case @ $125^{\circ}C$	-	-	15	16	-	15	18	$^{\circ}C/W$
<b>INPUT</b>									
Input Offset Voltage	$V_{IN} = 0V$ $A_V = -10V/V$	1	-	$\pm 1.0$	$\pm 5.0$	-	$\pm 1.0$	$\pm 8.0$	mV
Input Offset Voltage Drift	Bal. Pins = N/C	2,3	-	$\pm 6.0$	$\pm 50$	-	$\pm 10$	-	$\mu V/^{\circ}C$
Input Offset Adjust ③	$R_{POT} = 10K\Omega$ to $+V_{CC}$	-	-	$\pm 8.0$	-	-	$\pm 8.0$	-	V
Input Bias Current	$V_{CM} = 0V$ Either Input	1	-	$\pm 10$	$\pm 300$	-	$\pm 10$	$\pm 300$	pA
		2,3	-	$\pm 10$	$\pm 100$	-	-	-	nA
Input Offset Current ③	$V_{CM} = 0V$	-	-	$\pm 5.0$	-	-	$\pm 5.0$	-	pA
		-	-	$\pm 5.0$	-	-	-	-	nA
Input Impedance ③	$F = DC$	-	-	$3 \times 10^{12}$	-	-	$3 \times 10^{12}$	-	$\Omega$
Common Mode Range ③		-	$\pm 22$	$\pm 24$	-	$\pm 22$	$\pm 24$	-	V
Common Mode Rejection Ratio ③	$F = 10KHz$ $V_{CM} = \pm 22V$	4	90	100	-	90	100	-	dB
<b>OUTPUT</b>									
Output Voltage Swing	$R_L = 50\Omega$	4	$\pm 27$	$\pm 31$	-	$\pm 27$	$\pm 31$	-	V
	$R_L = 1K\Omega$	4	$\pm 30$	$\pm 33$	-	$\pm 30$	$\pm 33$	-	V
Output Current, Peak	$R_L = 33\Omega$ $T_J < 175^{\circ}C$	4	$\pm 600$	$\pm 800$	-	$\pm 600$	$\pm 800$	-	mA
Settling Time ② ③	0.1% 10V step	4	-	400	800	-	400	800	nS
<b>TRANSFER CHARACTERISTICS</b>									
Slew Rate	$V_{OUT} = \pm 10V$ $R_L = 1K\Omega$	4	200	500	-	200	500	-	$V/\mu S$
Open Loop Voltage Gain ③	$R_L = 10K\Omega$ $F = 100Hz$	4	90	106	-	90	106	-	dB
Gain Bandwidth Product ③	$F = 100KHz$	4	800	1200	-	800	1200	-	MHz

### NOTES:

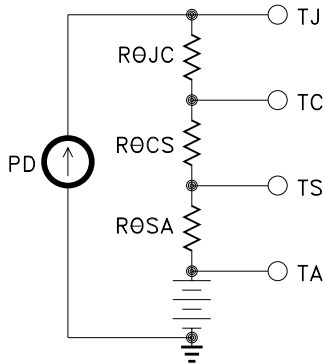
- ①  $R_{SC} = 0\Omega$  and  $\pm V_{CC} = 36VDC$  unless otherwise specified.
- ②  $A_V = -1$ , measured in false summing junction circuit.
- ③ Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
- ④ Industrial grade and "E" suffix devices shall be tested to subgroups 1 and 4 unless otherwise specified.
- ⑤ Military grade devices ("B" suffix) shall be 100% tested to subgroups 1,2,3 and 4.
- ⑥ Subgroups 5 and 6 testing available upon request.
- ⑦ Subgroup 1,4  $T_C = +25^{\circ}C$   
Subgroup 2,5  $T_J = +125^{\circ}C$   
Subgroup 3,6  $T_A = -55^{\circ}C$

## APPLICATION NOTES

### HEAT SINKING

To select the correct heat sink for your application, refer to the thermal model and governing equation below.

#### Thermal Model:



#### Governing Equation:

$$T_J = PD \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$

Where

- T<sub>J</sub> = Junction Temperature
- PD = Total Power Dissipation
- R<sub>θJC</sub> = Junction to Case Thermal Resistance
- R<sub>θCS</sub> = Case to Heat Sink Thermal Resistance
- R<sub>θSA</sub> = Heat Sink to Ambient Thermal Resistance
- T<sub>C</sub> = Case Temperature
- T<sub>A</sub> = Ambient Temperature
- T<sub>S</sub> = Sink Temperature

#### Example:

In our example the amplifier application requires the output to drive a 20 volt peak sine wave across a 400Ω load for 50mA of peak output current. For a worst case analysis we will treat the 50mA peak output current as a D.C. output current. The power supplies shall be set to ±40VDC.

- 1.) Find Driver Power Dissipation
 
$$PD = [(quiescent\ current) \times (+V_s - (-V_s))] + [(+V_s - V_o) \times I_{OUT}]$$

$$= [(50mA) \times (80V)] + [(20V) \times (0.05A)]$$

$$= 4W + 1.0W$$

$$= 5Watts$$
- 2.) For conservative design, set T<sub>J</sub> = +125°C.
- 3.) For this example, T<sub>A</sub> = +25°C
- 4.) R<sub>θJC</sub> = 16°C/W from MSK 1461B Data Sheet
- 5.) R<sub>θCS</sub> = 0.15°C/W for most thermal greases
- 6.) Rearrange governing equation to solve for R<sub>θSA</sub>

$$R_{\theta SA} = ((T_J - T_A)/PD) - (R_{\theta JC}) - (R_{\theta CS})$$

$$= ((125^\circ C - 25^\circ C) / 5W) - (16^\circ C/W) - (0.15^\circ C/W)$$

$$\cong 3.85^\circ C/W$$

The heat sink in this example must have a thermal resistance of no more than 3.85°C/W to maintain a junction temperature of no more than +125°C.

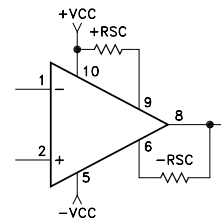
### CURRENT LIMIT

The output current of the MSK 1461 is internally limited to approximately ±750mA by two 0.8Ω internal current limit resistors. Additional current limit can be achieved through the use of two external current limit resistors. One resistor (+R<sub>SC</sub>) limits the positive output current and the other (-R<sub>SC</sub>) limits the negative output current. The value of the current limit resistors can be determined as follows:

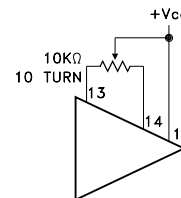
$$\pm R_{SC} = [(0.65V / \pm I_{LIM}) - 0.8\Omega]$$

Since the 0.65V term is obtained from the base to emitter voltage drop of a bipolar transistor, the equation only holds true for +25°C operation. As case temperature increases, the 0.65V term will decrease making the actual current limit set point decrease slightly.

The following schematic illustrates how to connect each current limit resistor:



#### INPUT OFFSET ADJUST CONNECTION



#### POWER SUPPLY BYPASSING

Both the negative and the positive power supplies must be effectively decoupled with a high and low frequency bypass circuit to avoid power supply induced oscillation. An effective decoupling scheme consists of a 0.1μF ceramic capacitor in parallel with a 4.7μF tantalum capacitor from each power supply pin to ground.

#### SAFE OPERATING AREA

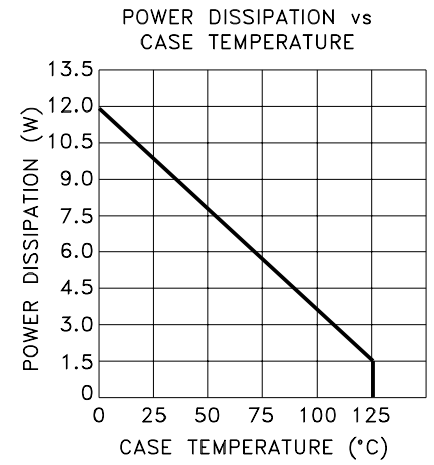
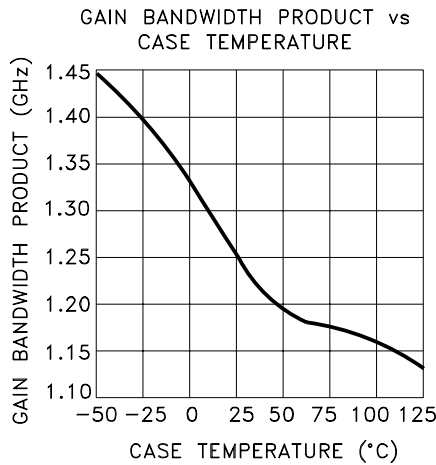
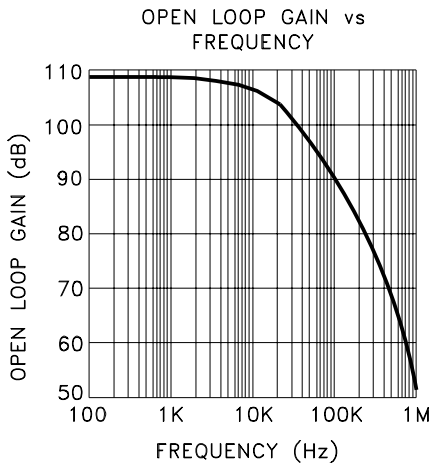
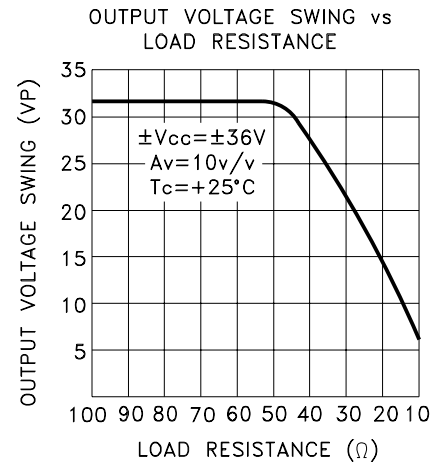
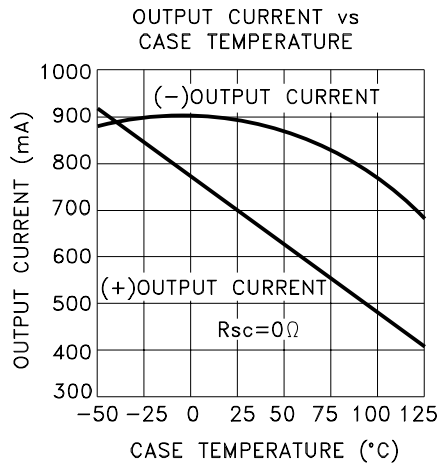
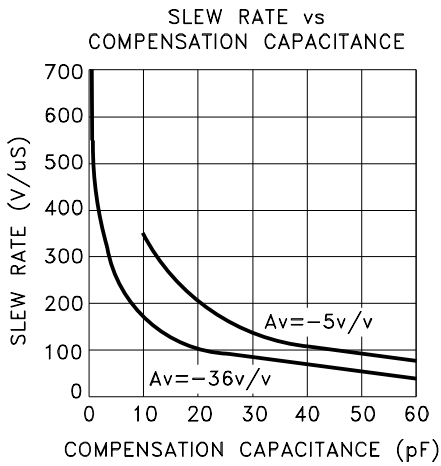
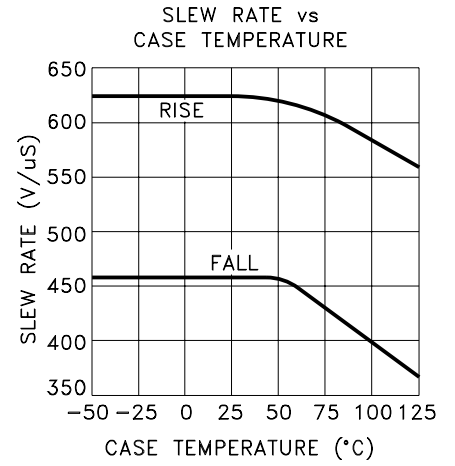
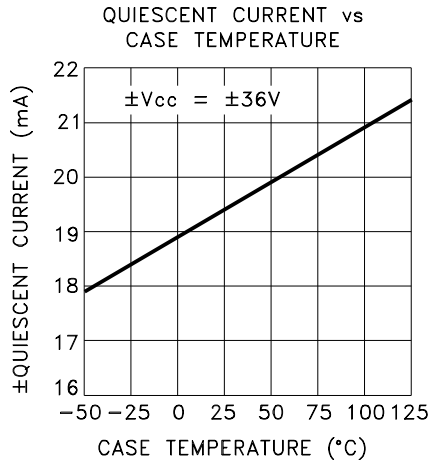
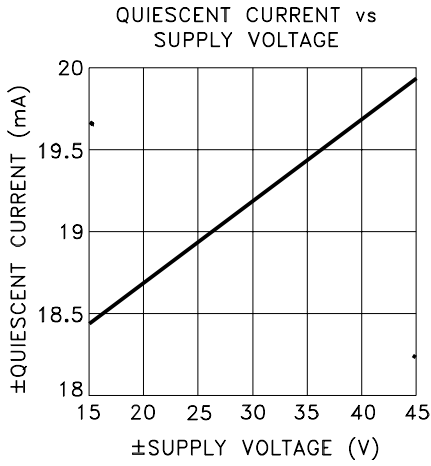
Any designer who has worked with power operational amplifiers is familiar with Safe Operating Area (S.O.A.) curves. S.O.A. curves are a graphical representation of the following three power limiting factors of any bipolar transistor output op-amp.

1. Wire Bond Current Carrying Capability
2. Transistor Junction Temperature
3. Secondary Breakdown Limitations

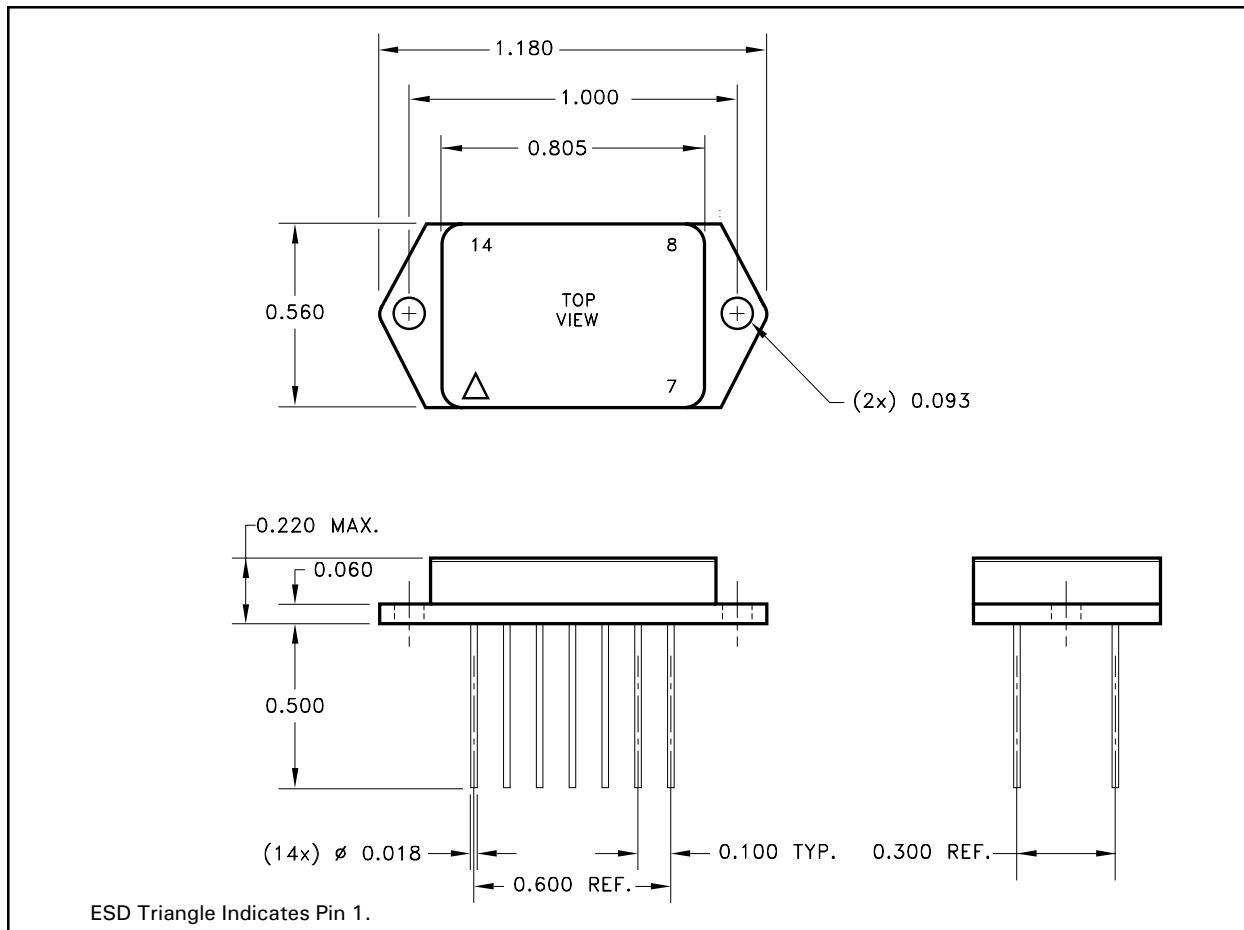
Since the MSK 1461 utilizes a MOSFET output, there are no secondary breakdown limitations and therefore no need for S.O.A. curves. The only limitation on output power is the junction temperature of the output drive transistors.

Whenever possible, junction temperature should be kept below 150°C to ensure high reliability. See "Heat Sinking" for more information involving junction temperature calculations.

# TYPICAL PERFORMANCE CURVES



## MECHANICAL SPECIFICATIONS



NOTE: ALL DIMENSIONS ARE  $\pm 0.010$  UNLESS OTHERWISE LABELED.

## ORDERING INFORMATION

Part Number	Screening Level
MSK1461	Industrial
MSK1461E	Extended Reliability
MSK1461B	Mil-PRF-38534 Class H

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