# SED1210

## CMOS DOT MATRIX LCD CONTROLLER DRIVER

### ■ DESCRIPTION

The SED1210 is a character LCD controller-driver, capable of driving displays as large as 2 lines of 8 character (5 × 8 pixels), with minimum external components.

The SED1210 has an internal CGROM consisting of 160 characters (5 × 7) plus the underline cursor, JIS, ASCII, and four user-programmable characters in RAM.

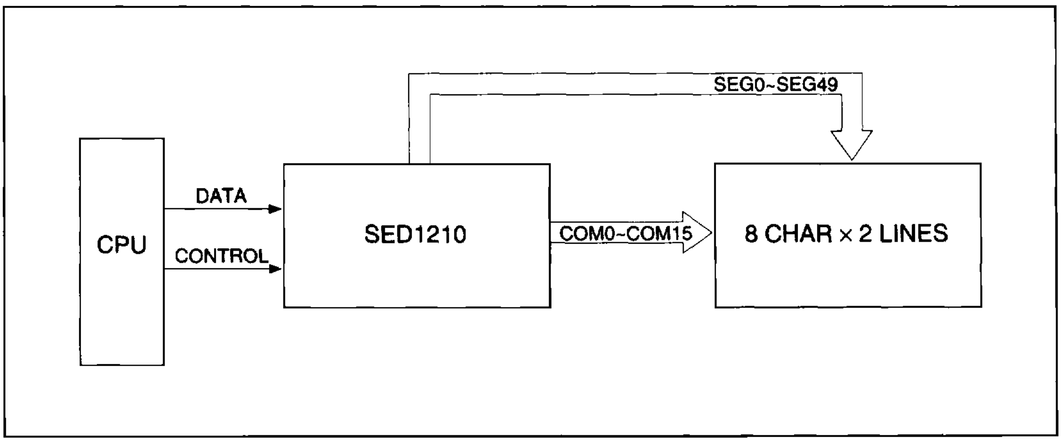
The SED1210 has 40 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 16 characters. The SED1210 can display one line of 40 characters using an SED1181FLA (64 bits) as an expansion segment driver.

The SED1210 is fabricated using a silicon gate CMOS technology process and features very low power dissipation. This makes the device suitable for handheld and portable applications.

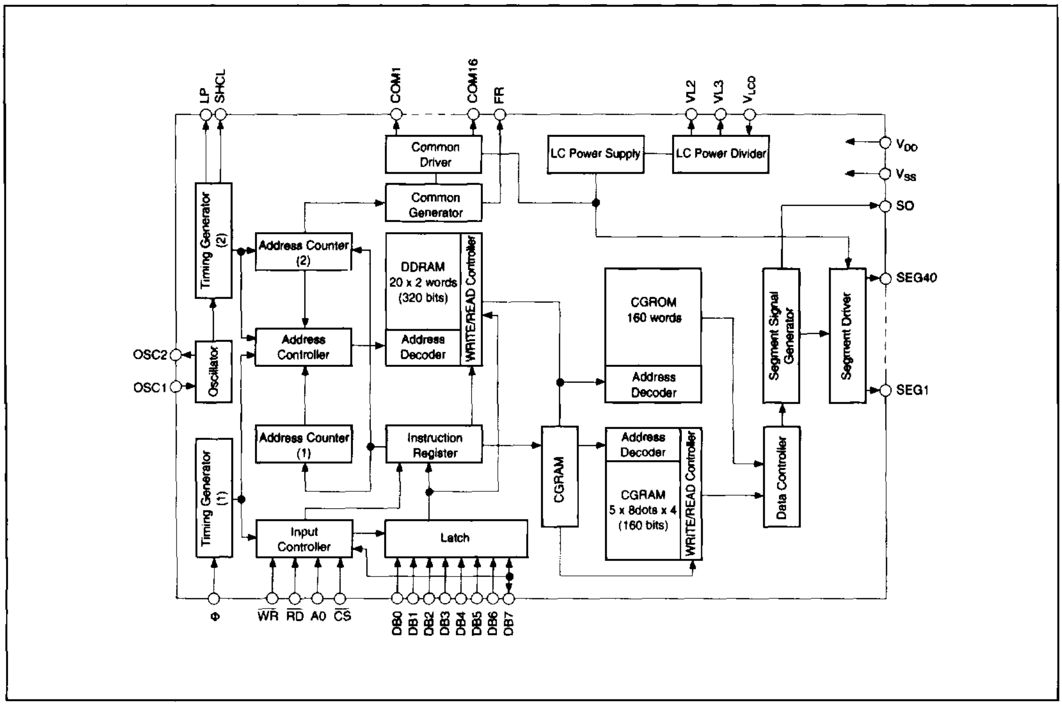
### ■ FEATURES

- Low-power CMOS technology
- 40 segment output
- 16 common output
- Duty: 1/8 or 1/16 (set by command)
- 8-bit CPU data interface, TTL compatible
- 13 display control commands
- CGROM: 160 characters
- CGRAM: 4 characters
- Display data RAM: 40 × 8 bits (40 characters)
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage .............. Logic: 2.5V to 5.5V
  LCD: 3.5V to 5.5V
- Package ........................ QFP5-80 pins (FOB, FOA)
  Al pad (DOA)
  Au bump (DOB)

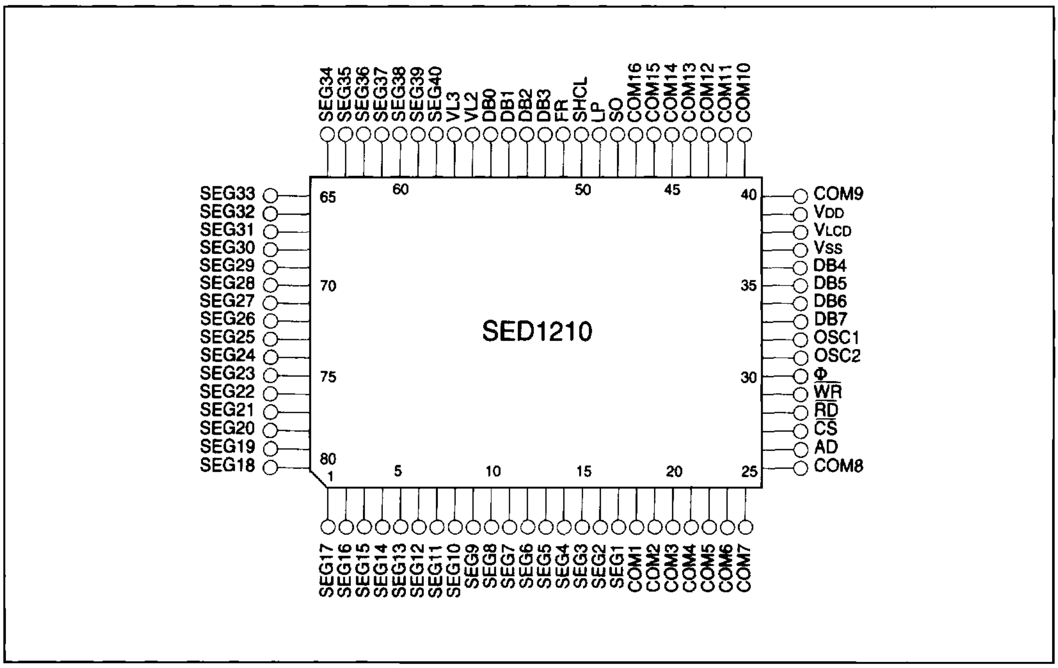
### ■ SYSTEM BLOCK DIAGRAM



## ■ BLOCK DIAGRAM




## ■ PINOUT



## ■ PIN DESCRIPTION

| Pin Name | Functions | No. of Pin |
|---|---|---|
| COM1 to 16 | LCD common output | 16 |
| SEG1 to 40 | LCD segment output | 40 |
| $\overline{CS}$ | Chip select input (active "Low") | 1 |
| $\overline{RD}$ | Read enable input (active "Low") | 1 |
| $\overline{WR}$ | Write enable input (active "Low" to "High") | 1 |
| A0 | "High" ; Display data<br>"Low" ; Command | 1 |
| DB0 to 7 | Data input (except DB7 ; Data input/output) | 8 |
| Φ | Clock for command execution | 1 |

| Pin Name | Functions | No. of Pin |
|---|---|---|
| OSC1, OSC2 | Connect oscillation resistor between OSC1 and OSC2. OSC1 also can be external clock input. | 2 |
| SO | Serial output for Segment driver | 1 |
| LP | Latch output for Segment driver | 1 |
| SHCL | Shift clock for Segment driver | 1 |
| FR | Frame output for Segment driver | 1 |
| VL2, VL3 | Supply voltage for Segment driver | 2 |
| $V_{DD}$ | Supply voltage (2.5V to 5.5V) for logic | 1 |
| $V_{SS}$ | GND (0V) | 1 |
| $V_{LCD}$ | Supply voltage for LCD<br>$3.5V \leq V_{DD}-V_{LCD} \leq 5.5V$ | 1 |

## ■ ELECTRICAL CHARACTERISTICS

### ● Absolute Maximum Ratings

($V_{SS}$ = 0V, $T_a$ = 25°C)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage (1) | $V_{DD}$ | –0.3 to 7.0 | V |
| Supply voltage (2) | $V_{LCD}$ | $V_{DD}$–7.0 to $V_{DD}$+0.3 | V |
| Input voltage | $V_I$ | –0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_O$ | –0.3 to $V_{DD}$+0.3 | V |
| Operating temperature | $T_{opr}$ | –20 to 70 | °C |
| Storage temperature | $T_{stg}$ | –65 to 150 | °C |
| Soldering temperature and time | $T_{sol}$ | 260°C•10s (at lead) | — |

## ■ DC CHARACTERISTICS

● $V_{DD}$ = 5V

$V_{SS}$ = 0V, $T_a$ = –20 to +70°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| Liquid crystal display supply voltage | $V_{LCD}$ | | $V_{DD}$ – 5.5 | — | $V_{DD}$ – 3.5 | V | $V_{LCD}$ |
| Oscillator feedback resistor | $R_f$ | $V_{DD}$ = 5.0V, fosc = 100kHz | 240 | 310 | 380 | kΩ | OSC1, OSC2 |
| Oscillator frequency | fosc | $V_{DD}$ = 5.0V, $R_f$ = 300kΩ | — | 100 | — | kHz | OSC1, OSC2 |
| Operating frequency (1) oscillator or external clock frequency | fosc | $V_{DD}$ = 4.5V | — | — | 300 | kHz | OSC1 |
| Operating frequency (2) | Φ | $V_{DD}$ = 4.5 to 5.5V | — | — | 3.2 | MHz | Φ |
| External clock duty | | $V_{DD}$ = 4.5 to 5.5V | 45 | 50 | 55 | % | OSC1, Φ |
| External clock rise time | $t_r$ | $V_{DD}$ = 4.5 to 5.5V | — | — | 50 | ns | OSC1, Φ |
| External clock fall time | $t_f$ | $V_{DD}$ = 4.5 to 5.5V | — | — | 50 | ns | OSC1, Φ |
| H-level input voltage (1) | $V_{IH1}$ | $V_{DD}$ = 4.5 to 5.5V | 2.0 | — | $V_{DD}$ | V | $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB7, Φ, A0 |
| L-level input voltage (1) | $V_{IL1}$ | $V_{DD}$ = 4.5 to 5.5V | 0 | — | 0.8 | V | |
| H-level input voltage (2) | $V_{IH2}$ | $V_{DD}$ = 4.5 to 5.5V | 0.8 × $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V | OSC1 |
| L-level input voltage (2) | $V_{IL2}$ | $V_{DD}$ = 4.5 to 5.5V | 0 | 0 | 0.2 × $V_{DD}$ | V | OSC1 |
| H-level input leakage current | $I_{LIH}$ | $V_{DD}$ = 5.5V, $V_{IH}$ = 5.5V | — | — | \|–1.0\| | μA | Φ, OSC1, DB0 to DB7 |
| L-level input leakage current | $I_{LIL}$ | $V_{DD}$ = 5.5V, $V_{IL}$ = 0V | — | — | 1.0 | μA | Φ, OSC1, DB0 to DB7 |
| Input pull-up current | $I_{IPU}$ | $V_{DD}$ = 5.0V, $V_{IL}$ = 0V | 3.0 | 10 | 30 | μA | $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0 |
| H-level output current (1) | $I_{OH1}$ | $V_{DD}$ = 4.5 to 5.5V, $V_{OH}$ = 2.4V | \|–1.0\| | — | — | mA | DB7 |
| L-level output current (1) | $I_{OL1}$ | $V_{DD}$ = 4.5 to 5.5V, $V_{OL}$ = 0.4V | 1.6 | — | — | mA | DB7 |
| H-level output current (2) | $I_{OH2}$ | $V_{DD}$ = 4.5V, $V_{OH}$ = 4.0V | 200 | — | — | μA | FR, LP |
| L-level output current (2) | $I_{OL2}$ | $V_{DD}$ = 4.5V, $V_{OL}$ = 0.5V | 200 | — | — | μA | XSCL, SO |
| Common driver output current (1) | $I_{OH}$ | $V_{DD}$ level; $V_{DD}$ – $V_{LCD}$ = 3.5V. Dividing resistor in low impedance state. 1/16 duty. 0.5 voltage drop. Measured on one pin with other pins open circuit. | \|–20\| | — | — | μA | COM1 to COM 16 |
| Common driver output current (2) | $I_{OL}$ | $V_{LCD}$ level | 20 | — | — | μA | |
| Common driver output current (3) | $I_{OL}$ | $V_{L1}$ level | \|±8\| | — | — | μA | |
| Common driver output current (4) | $I_{OL}$ | $V_{L4}$ level | \|±8\| | — | — | μA | |
| Segment driver output current (1) | $I_{OH}$ | $V_{DD}$ level | \|–12\| | — | — | μA | SEG1 to SEG40 |
| Segment driver output current (2) | $I_{OL}$ | $V_{LCD}$ level | 12 | — | — | μA | |
| Segment driver output current (3) | $I_{OL}$ | $V_{L2}$ level | \|±4\| | — | — | μA | |
| Segment driver output current (4) | $I_{OL}$ | $V_{L3}$ level | \|±4\| | — | — | μA | |
| Driver current | $I_{OH}$ | $V_{DD}$ – $V_{LCD}$ = 3.5V 0.5V voltage drop | — | 2 | — | μA | $V_{L2}$, $V_{L3}$ |
| | $I_{OL}$ | | — | 2 | — | μA | |
| Voltage-divider resistor (1) | $R_{d1}$ | Normal conditions | 30 | 130 | 300 | kΩ | |
| Voltage-divider resistor (2) | $R_{d2}$ | Low impedance state | 3.0 | 13 | 30 | kΩ | |
| Voltage-divider resistor low impedance duty | $t_{Rd1}$/$t_{Rd2}$ | 1/8 duty | — | 11/400 | — | — | |
| | | 1/16 duty | — | 11/200 | — | — | |
| Command execution time | tcomd | From $\overline{WR}$ rising edge to the end of internal processing | — | — | 16/Φ | μs | |
| Average operating current | $I_{DD}$ | $V_{DD}$ = 5.0V, $V_{LCD}$ = 0V, fosc = 100 kHz, Φ = 1 MHz, $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0V, output open | — | 80 | 150 | μA | $V_{DD}$ |

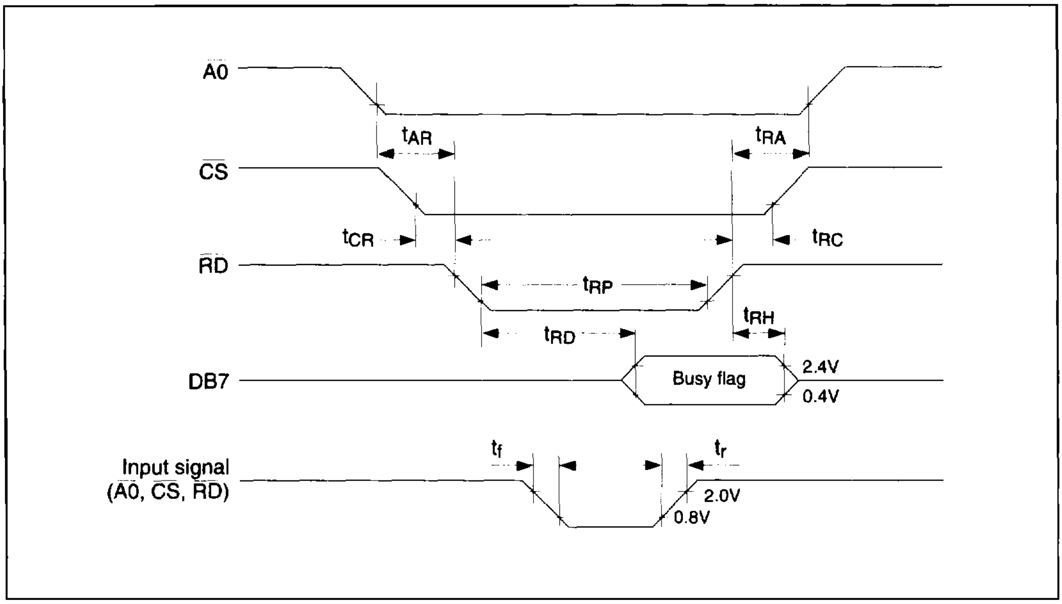
- $V_{DD} = 3V$

$V_{SS} = 0V$, $T_a = -20$ to $+70°C$

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Pin |
|---|---|---|---|---|---|---|---|
| Liquid crystal display supply voltage | $V_{LCD}$ | | 3.5 | — | 5.5 | V | $V_{LCD}$ |
| Oscillator feedback resistor | $R_f$ | $V_{DD} = 3.0V$, $f_{osc} = 100kHz$ | 210 | 290 | 370 | kΩ | OSC1, OSC2 |
| Oscillator frequency | $f_{osc}$ | $V_{DD} = 3.0V$, $R_f = 300kΩ$ | — | 100 | — | kHz | OSC1, OSC2 |
| Operating frequency (1) oscillator or external clock frequency | $f_{osc}$ | $V_{DD} = 2.5V$ | — | — | 300 | kHz | OSC1 |
| Operating frequency (2) | Φ | $V_{DD} = 2.5$ to $4.5V$ | — | — | 1 | MHz | Φ |
| External clock duty | | $V_{DD} = 2.5$ to $4.5V$ | — | 50 | — | % | OSC1, Φ |
| External clock rise time | $t_r$ | $V_{DD} = 2.5$ to $4.5V$ | — | — | 50 | ns | OSC1, Φ |
| External clock fall time | $t_f$ | $V_{DD} = 2.5$ to $4.5V$ | — | — | 50 | ns | OSC1, Φ |
| H-level input voltage (1) | $V_{IH1}$ | $V_{DD} = 2.5$ to $4.5V$ | $0.8 \times V_{DD}$ | — | — | V | $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DB0 to DB7, Φ, A0 |
| L-level input voltage (1) | $V_{IL1}$ | $V_{DD} = 2.5$ to $4.5V$ | — | — | $0.2 \times V_{DD}$ | V | |
| H-level input voltage (2) | $V_{IH2}$ | $V_{DD} = 2.5$ to $4.5V$ | $0.8 \times V_{DD}$ | — | — | V | OSC1 |
| L-level input voltage (2) | $V_{IL2}$ | $V_{DD} = 2.5$ to $4.5V$ | — | — | $0.2 \times V_{DD}$ | V | OSC1 |
| H-level input leakage current | $I_{LIH}$ | $V_{DD} = 4.5V$ | — | — | — | μA | Φ, OSC1, DB0 to DB7 |
| L-level input leakage current | $I_{LIL}$ | $V_{DD} = 4.5V$ | — | — | — | μA | Φ, OSC1, DB0 to DB7 |
| Input pull-up current | $I_{IPU}$ | $V_{DD} = 3.5V$ | — | — | — | μA | $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0 |
| H-level output current (1) | $I_{OH1}$ | $V_{DD} = 2.5V$, $V_{OH} = 2.0V$ | 200 | — | — | μA | DB7 |
| L-level output current (1) | $I_{OL1}$ | $V_{DD} = 2.5V$, $V_{OL} = 0.5V$ | 200 | — | — | μA | DB7 |
| H-level output current (2) | $I_{OH2}$ | $V_{DD} = 2.5V$, $V_{OH} = 2.0V$ | 200 | — | — | μA | FR, LP |
| L-level output current (2) | $I_{OL2}$ | $V_{DD} = 2.5V$, $V_{OL} = 0.5V$ | 200 | — | — | μA | XSCL, SO |
| Common driver output current (1) | $I_{OH}$ | $V_{DD}$ level; $V_{DD} - V_{LCD} = 3.5V$. Dividing resistor in low impedance state. 1/16 duty. 0.5 voltage drop. Measured on one pin with other pins open circuit. | \|−20\| | — | — | μA | COM1 to COM16 |
| Common driver output current (2) | $I_{OL}$ | $V_{LCD}$ level | 20 | — | — | μA | |
| Common driver output current (3) | $I_{OL}$ | $V_{L1}$ level | \|±8\| | — | — | μA | |
| Common driver output current (4) | $I_{OL}$ | $V_{L4}$ level | \|±8\| | — | — | μA | |
| Segment driver output current (1) | $I_{OH}$ | $V_{DD}$ level | \|−12\| | — | — | μA | SEG1 to SEG40 |
| Segment driver output current (2) | $I_{OL}$ | $V_{LCD}$ level | 12 | — | — | μA | |
| Segment driver output current (3) | $I_{OL}$ | $V_{L2}$ level | \|±4\| | — | — | μA | |
| Segment driver output current (4) | $I_{OL}$ | $V_{L3}$ level | \|±4\| | — | — | μA | |
| Driver current (1) | $I_{OH}$ | $V_{DD} - V_{LCD} = 3.5V$ 0.5V voltage drop | — | 2 | — | μA | $V_{L2}$, $V_{L3}$ |
| Driver current (2) | $I_{OL}$ | | — | 2 | — | μA | |
| Voltage-divider resistor (1) | $R_{d1}$ | Normal conditions | — | 130 | — | kΩ | |
| Voltage-divider resistor (2) | $R_{d2}$ | Low impedance state | — | 13 | — | kΩ | |
| Voltage-divider resistor low impedance duty | $t_{Rd1}$/ $t_{Rd2}$ | 1/8 duty | — | 11/400 | — | — | |
| | | 1/16 duty | — | 11/200 | — | — | |
| Command execution time | $t_{comd}$ | From $\overline{WR}$ rise time to the end of internal processing | — | — | 16/Φ | μs | |
| Average operating current | $I_{DD}$ | $V_{DD} - V_{SS} = 3.5V$, $V_{DD} - V_{LCD} = 5V$, Φ = 500kHz, $\overline{CS} = \overline{RD} = \overline{WR} = A0 = V_{DD}$, $R_f = 300kΩ$ | — | 60 | — | μA | $V_{DD}$ |

## ■ AC CHARACTERISTICS

### ● MPU Read Timing




$V_{DD}$ = 5V, $T_a$ = –20 to 70°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Setup time for A0 → $\overline{RD}$ | $t_{AR}$ | — | 0 | — | — | ns |
| Setup time for $\overline{CS}$ → $\overline{RD}$ | $t_{CR}$ | — | 0 | — | — | ns |
| $\overline{RD}$ delay output time* | $t_{RD}$ | — | — | — | 200 | ns |
| Hold time for $\overline{RD}$ → A0 | $t_{RA}$ | — | 20 | — | — | ns |
| Hold time for $\overline{RD}$ → $\overline{CS}$ | $t_{RC}$ | — | 20 | — | — | ns |
| Data hold time | $t_{RH}$ | — | 10 | — | — | ns |
| Read pulsewidth | $t_{RP}$ | — | 300 | — | — | ns |
| Input fall time | $t_f$ | — | — | — | 50 | ns |
| Input rise time | $t_r$ | — | — | — | 50 | ns |

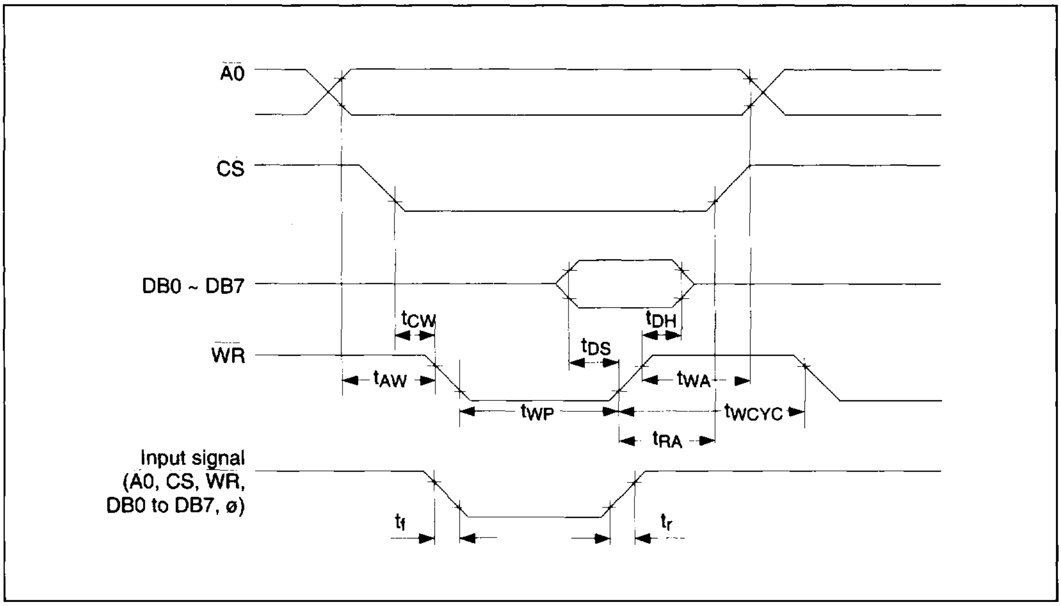
**Note:** Load on pin DB7 is $C_L$ = 100 pF.

$V_{DD}$ = 3V, $T_a$ = –20 to 70°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Setup time for A0 → $\overline{RD}$ | $t_{AR}$ | — | 0 | — | — | ns |
| Setup time for $\overline{CS}$ → $\overline{RD}$ | $t_{CR}$ | — | 0 | — | — | ns |
| $\overline{RD}$ delay output time* | $t_{RD}$ | — | — | — | 350 | ns |
| Hold time for $\overline{RD}$ → A0 | $t_{RA}$ | — | 0 | — | — | ns |
| Hold time for $\overline{RD}$ → $\overline{CS}$ | $t_{RC}$ | — | 0 | — | — | ns |
| Data hold time | $t_{RH}$ | — | 10 | — | — | ns |
| Read pulsewidth | $t_{RP}$ | — | 400 | — | — | ns |
| Input fall time | $t_f$ | — | — | — | 50 | ns |
| Input rise time | $t_r$ | — | — | — | 50 | ns |

**Note:** Load on pin DB7 is $C_L$ = 100 pF.

- **MPU Write Timing**



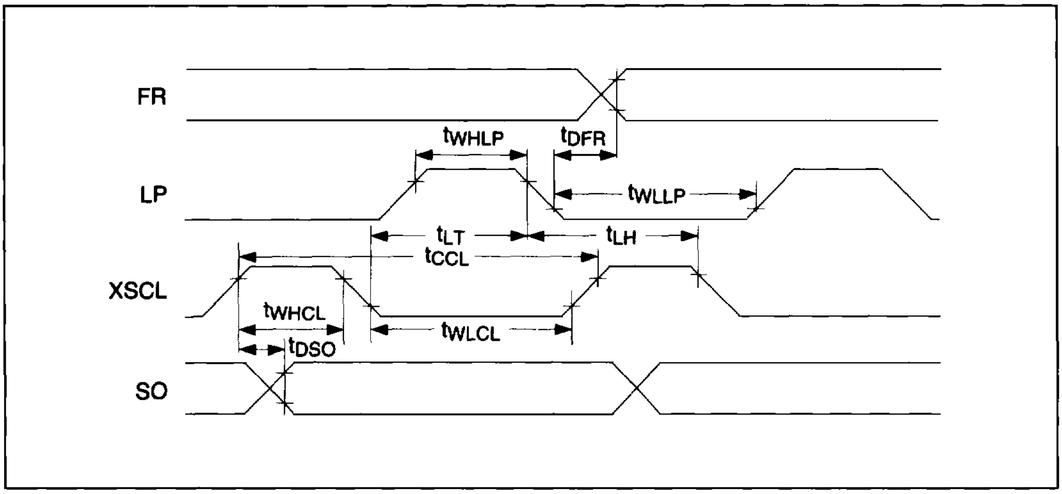

VDD = 5V, Ta = –20 to 70°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| A0 → WR setup time | $t_{AW}$ | — | 0 | — | — | ns |
| CS → WR setup time | $t_{CW}$ | — | 0 | — | — | ns |
| Data setup time | $t_{DS}$ | — | 120 | — | — | ns |
| WR → A0 hold time | $t_{WA}$ | — | 20 | — | — | ns |
| WR → CS hold time | $t_{WC}$ | — | 20 | — | — | ns |
| Data hold time | $t_{DH}$ | — | 20 | — | — | ns |
| Write pulsewidth | $t_{WP}$ | — | 200 | — | — | ns |
| Write cycle | $t_{WCYC}$ | — | 16/Φ | — | — | µs |
| Input fall time | $t_f$ | — | — | — | 50 | ns |
| Input rise time | $t_r$ | — | — | — | 50 | ns |

VDD = 3V, Ta = –20 to 70°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| A0 → WR setup time | $t_{AW}$ | — | 0 | — | — | ns |
| CS → WR setup time | $t_{CW}$ | — | 0 | — | — | ns |
| Data setup time | $t_{DS}$ | — | 120 | — | — | ns |
| WR → A0 hold time | $t_{WA}$ | — | 0 | — | — | ns |
| WR → CS hold time | $t_{WC}$ | — | 0 | — | — | ns |
| Data hold time | $t_{DH}$ | — | 100 | — | — | ns |
| Write pulsewidth | $t_{WP}$ | — | 200 | — | — | ns |
| Write cycle | $t_{WCYC}$ | — | 16/Φ | — | — | µs |
| Input fall time | $t_f$ | — | — | — | 50 | ns |
| Input rise time | $t_r$ | — | — | — | 50 | ns |

- **X-Driver Control Timing**




$V_{DD}$ = 2.5 to 5.5V, $T_a$ = –20 to 70°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Shift clock cycle | $t_{CCL}$ | — | 3.3 | 10 | — | µs |
| Shift clock "H" pulsewidth | $t_{WHCL}$ | — | 1.0 | — | — | µs |
| Shift clock "L" pulsewidth | $t_{WLCL}$ | — | 1.0 | — | — | µs |
| Delay time for XSCL rise → SO output | $t_{DSO}$ | — | — | — | 1 | µs |
| Latch pulse "H" pulsewidth | $t_{WHLP}$ | — | 1.0 | — | — | µs |
| Latch pulse "L" pulsewidth | $t_{WLLP}$ | — | 300 | — | — | ns |
| Latch time | $t_{LT}$ | — | 500 | — | — | ns |
| Latch hold time | $t_{LH}$ | — | 500 | — | — | ns |
| Delay time for frame signal | $t_{DFR}$ | — | — | — | 500 | ns |

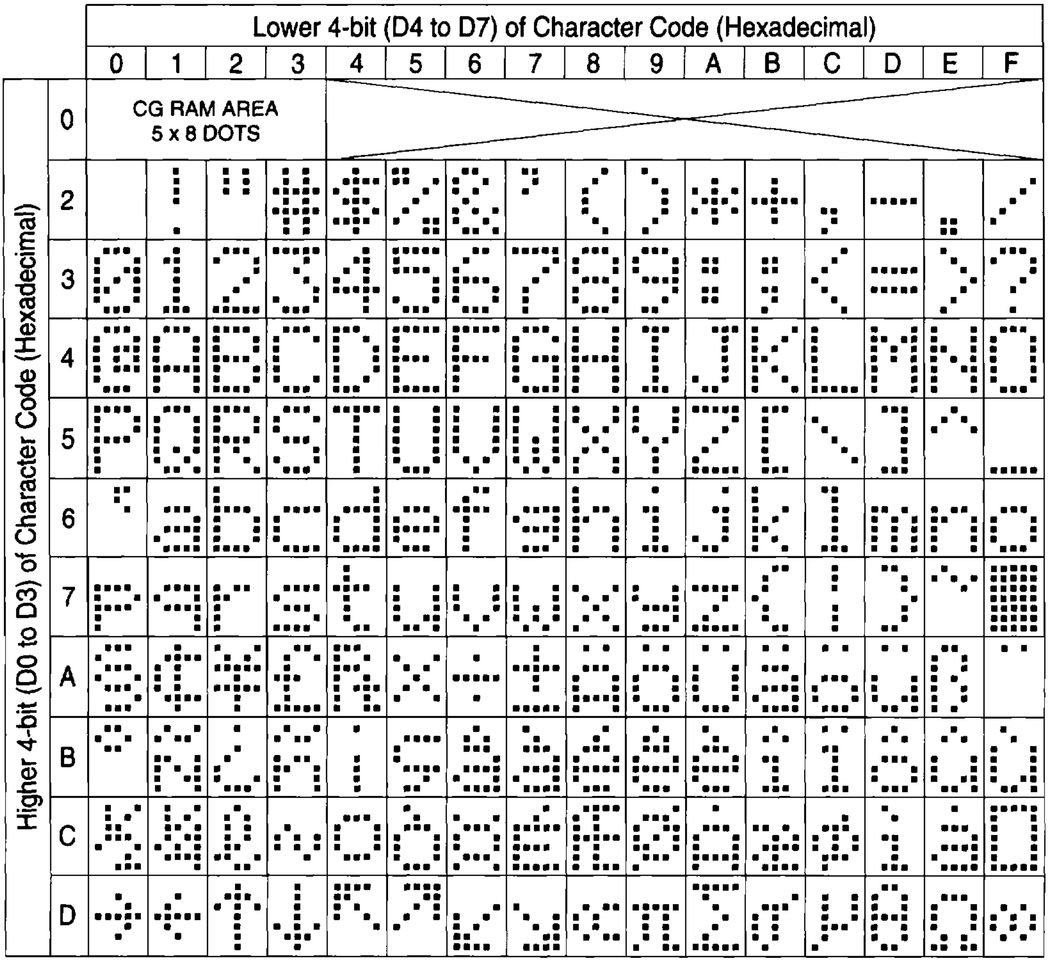
**Note:** Load capacitance $C_L$ = 15 pF

## ■ DISPLAY COMMAND

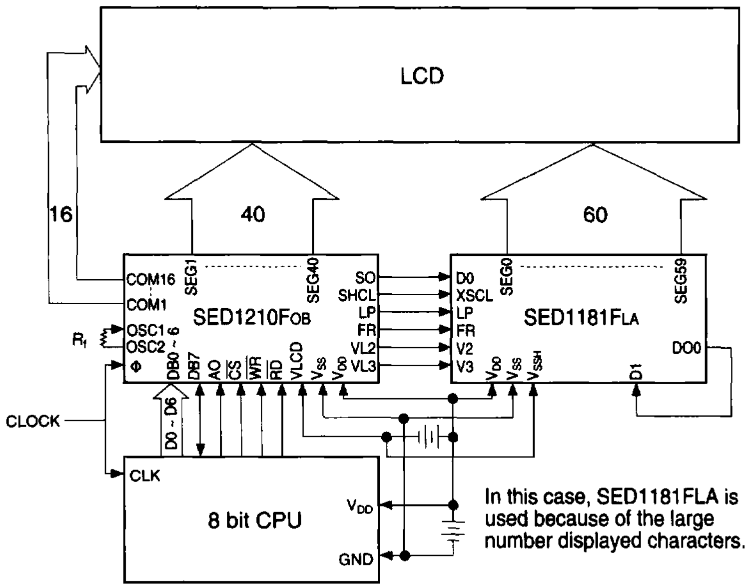
| Command Name | $\overline{CS}$ | $\overline{WR}$ | $\overline{RD}$ | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SET CURSOR DIRECTION | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | D/I | D0=1: Decrement<br>D0=0: Increment |
| CURSOR ADDRESS −1/+1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | −1/+1 | D0=1: −1<br>D0=0: +1 |
| CURSOR FONT SELECT | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | A/U | D0=1: All dots blinking<br>D0=0: Under line |
| CURSOR BLINK ON/OFF | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | ON/OFF | D0=1: ON<br>D0=0: OFF |
| DISPLAY ON/OFF | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | ON/OFF | |
| CURSOR ON/OFF | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | ON/OFF | |
| SYSTEM RESET | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Except data RAM and CGRAM |
| DUTY SELECT | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 2/1 | D0=1: 2 line display (1/16 duty)<br>D0=0: 1 line display (1/8 duty) |
| SET CGRAM ADDRESS | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A3 | A2 | A1 | A0 | UPPER ADDRESS IS FIXED TO 0H |
| SET CGRAM DATA | 0 | 0 | 1 | 0 | 0 | 1 | 0 | D4 | D3 | D2 | D1 | D0 | |
| SET CURSOR ADDRESS | 0 | 0 | 1 | 0 | 1 | 2nd/1st | A5 | A4 | A3 | A2 | A1 | A0 | D6=1: N figure for second line<br>D6=0: N figure for first line |
| SET CHARACTER CODE | 0 | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| BUSY FLAG CHECK | 0 | 1 | 0 | 0 | BF | * | * | * | * | * | * | * | BF=0: Ready *: High impedance<br>BF=1: Busy |

**Note:** Misoperation may be caused when any command other than that listed in the above table is inputted.

## ■ CHARACTER CODE MAP (SED1210FoB)



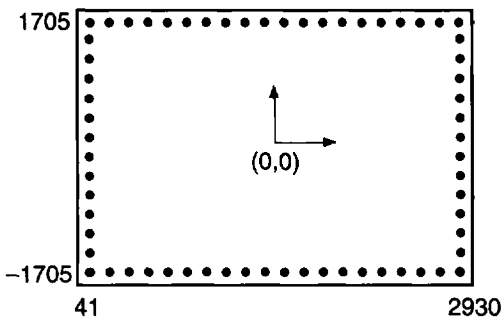
## ■ EXAMPLE OF APPLICATION (20 characters × 2 lines display)




SED1210FOB can be connected directly to the address bus or the data bus of a microprocessor, or to a peripheral interface unit.

## ■ DIE SPECIFICATION

### ● PAD LAYOUT




### ● DIE & PAD SPECIFICATIONS

| | |
|---|---|
| Die Size: | 5.86 mm x 3.41 mm |
| Die Thickness: | 400 µm |
| Pad Size: | 90 µm x 90 µm |
| Pad Pitch: | 190 µm |

## • PAD COORDINATES

unit: µm

| Pad No. | Pad Name | X | Y |
|---|---|---|---|
| 1 | SEG17 | 2123 | 1552 |
| 2 | SEG16 | 1932 | 1552 |
| 3 | SEG15 | 1742 | 1552 |
| 4 | SEG14 | 1551 | 1552 |
| 5 | SEG13 | 1361 | 1552 |
| 6 | SEG12 | 1170 | 1552 |
| 7 | SEG11 | 780 | 1552 |
| 8 | SEG10 | 789 | 1552 |
| 9 | SEG9 | 599 | 1552 |
| 10 | SEG8 | 408 | 1552 |
| 11 | SEG7 | 218 | 1552 |
| 12 | SEG6 | 27 | 1552 |
| 13 | SEG5 | -163 | 1552 |
| 14 | SEG4 | -354 | 1552 |
| 15 | SEG3 | -544 | 1552 |
| 16 | SEG2 | -735 | 1552 |
| 17 | SEG1 | -925 | 1552 |
| 18 | COM1 | -1116 | 1552 |
| 19 | COM2 | -1306 | 1552 |
| 20 | COM3 | -1497 | 1552 |
| 21 | COM4 | -1687 | 1552 |
| 22 | COM5 | -1878 | 1552 |
| 23 | COM6 | -2068 | 1552 |
| 24 | COM7 | -2259 | 1552 |
| 25 | COM8 | -2778 | 1429 |
| 26 | A0 | -2778 | 1238 |
| 27 | $\overline{CS}$ | -2778 | 1048 |
| 28 | $\overline{RD}$ | -2778 | 857 |
| 29 | $\overline{WR}$ | -2778 | 667 |
| 30 | Φ | -2778 | 476 |
| 31 | OSC2 | -2778 | 286 |
| 32 | OSC1 | -2778 | 95 |
| 33 | DB7 | -2778 | -95 |
| 34 | DB6 | -2778 | -286 |
| 35 | DB5 | -2778 | -476 |
| 36 | DB4 | -2778 | -667 |
| 37 | $V_{SS}$ | -2778 | -857 |
| 38 | $V_{LCD}$ | -2778 | -1048 |
| 39 | $V_{DD}$ | -2778 | -1238 |
| 40 | COM9 | -2778 | -1429 |
| 41 | COM10 | -2220 | -1552 |
| 42 | COM11 | -2029 | -1552 |
| 43 | COM12 | -1839 | -1552 |
| 44 | COM13 | -1648 | -1552 |
| 45 | COM14 | -1458 | -1552 |
| 46 | COM15 | -1267 | -1552 |
| 47 | COM16 | -1077 | -1552 |
| 48 | SO | -886 | -1552 |
| 49 | LP | -696 | -1552 |
| 50 | SHCL | -505 | -1552 |
| 51 | FR | -315 | -1552 |
| 52 | DB3 | -124 | -1552 |
| 53 | DB2 | 66 | -1552 |
| 54 | DB1 | 257 | -1552 |
| 55 | DB0 | 447 | -1552 |
| 56 | VL2 | 638 | -1552 |
| 57 | VL3 | 828 | -1552 |
| 58 | SEG40 | 1019 | -1552 |
| 59 | SEG39 | 1209 | -1552 |
| 60 | SEG38 | 1400 | -1552 |
| 61 | SEG37 | 1590 | -1552 |
| 62 | SEG36 | 1781 | -1552 |
| 63 | SEG35 | 1971 | -1552 |
| 64 | SEG34 | 2162 | -1552 |
| 65 | SEG33 | 2777 | -1385 |
| 66 | SEG32 | 2777 | -1195 |
| 67 | SEG31 | 2777 | -1004 |
| 68 | SEG30 | 2777 | -814 |
| 69 | SEG29 | 2777 | -623 |
| 70 | SEG28 | 2777 | -433 |
| 71 | SEG27 | 2777 | -242 |
| 72 | SEG26 | 2777 | -52 |
| 73 | SEG25 | 2777 | 139 |
| 74 | SEG24 | 2777 | 329 |
| 75 | SEG23 | 2777 | 520 |
| 76 | SEG22 | 2777 | 710 |
| 77 | SEG21 | 2777 | 901 |
| 78 | SEG20 | 2777 | 1091 |
| 79 | SEG19 | 2777 | 1282 |
| 80 | SEG18 | 2777 | 1472 |

**Note:** The origin of coordination is the center of the die.