PRELIMINARY

AMD

Élan™SC300

Highly Integrated, Low-Power, 32-Bit Microcontroller

DISTINCTIVE CHARACTERISTICS

- **Highly integrated, single-chip CPU and system logic**
  - Optimized for embedded PC applications
  - Combines 32 bit, x86 compatible, low-voltage CPU with memory controller, PC/AT peripheral controllers, real-time clock, and PLL clock generators
  - 0.7 micron, low-voltage, CMOS process, fully static
- **Enhanced Am386® SXLV CPU core**
  - 25 MHz or 33 MHz operating frequencies
  - 3.3 V core, 3.3 V or 5 V memory and I/O
  - Low-power, fully static design for long battery life
  - System Management Mode (SMM) for power management control
- **Integrated power management functions**
  - Internal clock generators (using multiple Phase-Locked Loops and one external 32-KHz crystal)
  - Supports CPU System Management Mode (SMM)
  - Multiple operating modes: High Speed PLL, Low Speed PLL, Doze, Sleep, Suspend, and Off. Fully static design allows stopped clock.
  - Comprehensive control of system and peripheral clocks
  - Five external power management control pins
  - Suspend refresh of DRAM array
  - Clock switching during ISA cycles
  - Low power consumption: 0.12 mW typical Suspend mode power
  - Simultaneous multiple-voltage I/O pads operate at either 3.3 V or 5 V. Core operates at 3.3 V for minimum power consumption.
- **Integrated memory controller**
  - Controls symmetrically addressable DRAM or asymmetrical 512 Kbyte x 8 bit or 1 Mbyte x 16 bit DRAM or SRAM as main memory
  - Zero wait-state access with 70 ns, Page mode DRAMs
  - Supports up to 16 Mbyte system memory
  - Supports up to 16 Mbyte of application ROM/ Flash, and 320 Kbyte direct ROM BIOS access. Also supports shadow RAM
  - Fully PC/AT compatible
- **Integrated PC/AT-compatible peripheral logic**
  - One programmable interval timer (fully 8254 compatible)
  - Two programmable interrupt controllers (8259A compatible)
  - Two DMA controllers (8237A compatible)
  - Built-in real-time clock (146818A compatible), with an additional 114 bytes of RAM
  - Internal Phase-Locked Loops (PLL) generate all clocks from single 32.768 kHz crystal input
- **Bus configurations**
  - 16-bit data path
  - Optional bus configurations:
    - — Internal LCD controller with subset ISA
    - — 386 Local Bus mode with subset ISA
    - — Maximum ISA Bus mode
  - Four programmable chip selects
  - Built-in 8042 chip select
- **Serial port controller (16450 UART compatible)**
- **Bidirectional parallel port with EPP**
- **Integrates two PCMCIA Version 2.1 slots**
- **Integrated CGA-compatible LCD controller**
  - Fully 6845 compatible
  - 16 gray levels in Text mode; 2 or 4 levels in Graphics mode
  - Supports the following LCD Panel Sizes:
    - — 320 x 240 single scan (2 bpp)
    - — 640 x 200 single/dual scan (1 bpp)
    - — 480 x 320 single scan (1 bpp)

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Issue Date: **October 1997**

GENERAL DESCRIPTION

The ÉlanSC300 microcontroller is a highly integrated, low-voltage, single-chip implementation of the Am386SXLV microprocessor plus most of the additional logic needed for an AT-compatible personal computer. It is ideal for embedded PC applications, such as point-of-sale equipment, web appliances, industrial controls, and communication equipment.

The ÉlanSC300 microcontroller from AMD is part of the growing Élan family of mobile computing products, which leverage existing AMD core modules. The ÉlanSC300 microcontroller demonstrates the feasibility of constructing highly integrated components built from standard cores and getting these products to market quickly.

The ÉlanSC300 microcontroller does this by combining an Am386SXLV low-voltage microprocessor core with a memory control unit, a Power Management Unit (PMU), and the bus control and peripheral control logic of a PC/AT-compatible computer. For more information about the Am386 microprocessors, see the *Am386® SX/SXL/SXLV Data Sheet*, order #21020 and the *Am386® DX/DXL Data Sheet*, order #21017.

For more information about the ÉlanSC310 microcontroller, see the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

The ÉlanSC300 microcontroller includes a memory controller that supports up to 16 Mbyte of DRAM, Flash or ROM; power management functions; a bus controller that supports local or ISA bus; a serial port controller that is 16450 UART compatible; a bidirectional EPP-compliant parallel port; a 146818A-compatible real-time clock; internal phase-locked loops for clock generation; and standard PC logic chips (8259A, 8237A, and 8254).

The ÉlanSC300 microcontroller's true static design and low operating voltage enable battery-powered operation and lower weight for embedded PC applications. The internal core of the ÉlanSC300 microcontroller operates at 3.3 V and the I/O pads allow either 3.3 V or 5 V operation. Lowering typical operating voltage from 5 V to 3.3 V can dramatically reduce power consumption.

Functionally, the ÉlanSC300 microcontroller is a 100% DOS/Windows-compatible, PC/AT-compatible computer on a chip that is designed to furnish the customer with a high-performance, low-power system solution, providing state-of-the-art power management in a small physical footprint.

The ÉlanSC300 microcontroller is available in both 25- and 33-MHz versions, in a 208-lead Plastic Shrink Quad Flat Pack (QFP) (PQR package) and a 208-lead Thin Quad Flat Pack (TQFP) (PQL package).

Note: *Unless specified otherwise, the timings in this data sheet are based on the 33-MHz version of the ÉlanSC300 microcontroller.*

CUSTOMER SERVICE

The AMD customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from the AMD worldwide staff of field application engineers and factory support staff who can answer E86 family hardware and software development questions.

Hotline and World Wide Web Support

For answers to technical questions, AMD provides a toll-free number for direct access to our corporate applications hotline. Also available is the AMD World Wide Web home page and FTP site, which provides the latest E86 family product information.

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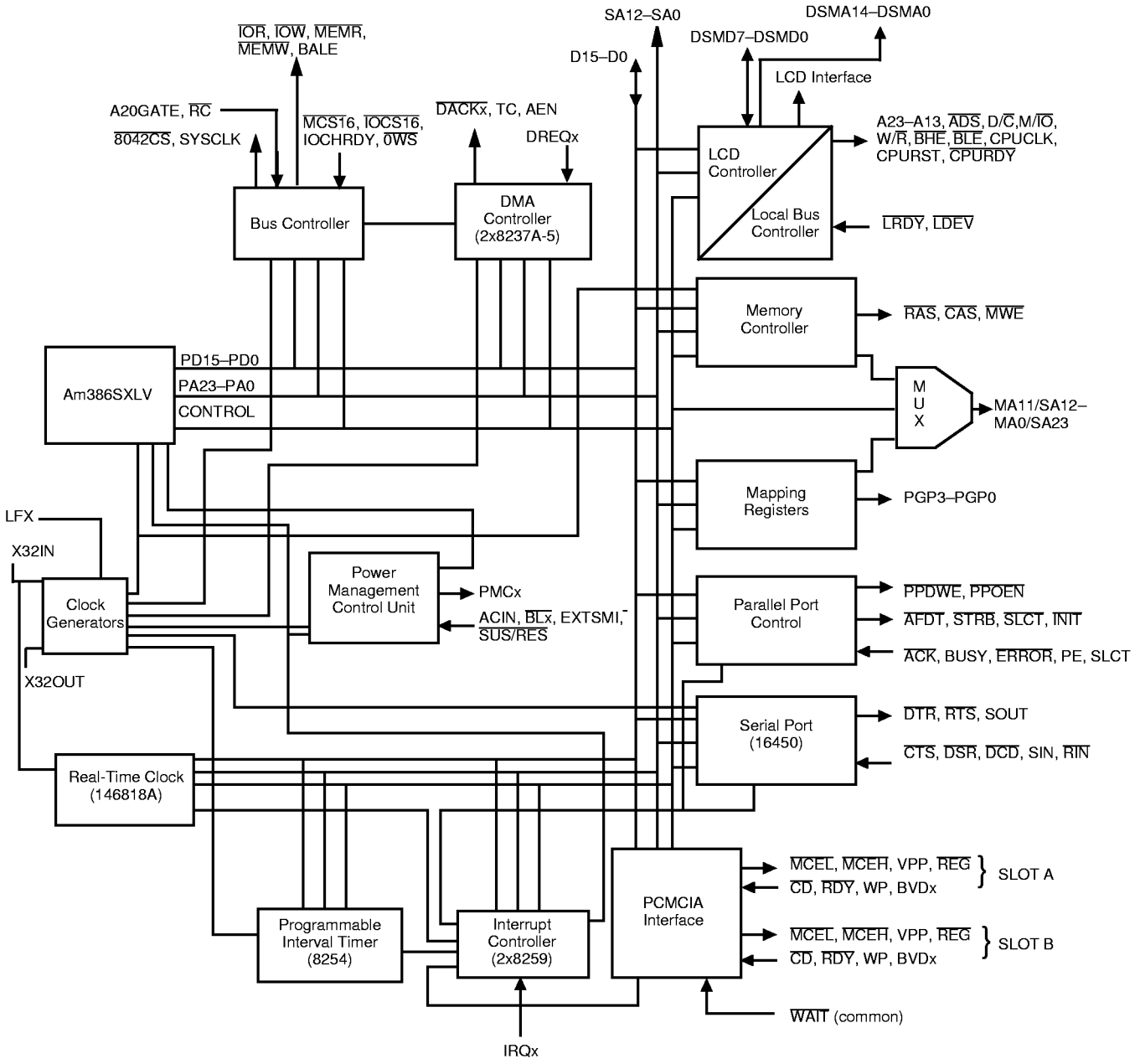
Documentation and Literature

Free E86 family information such as data books, user's manuals, data sheets, application notes, the FusionE86 Partner Solutions Catalog, and other literature is available with a simple phone call. Internationally, contact your local AMD sales office for complete E86 family literature.

Literature Ordering

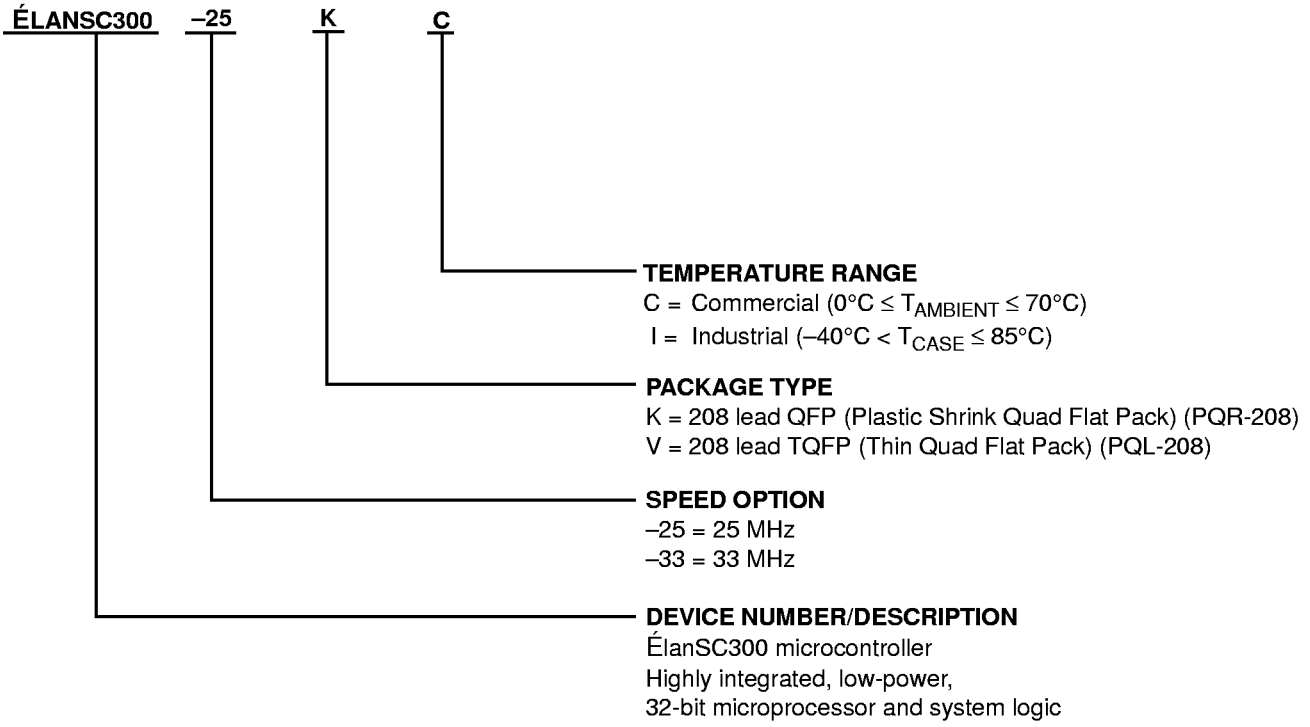
(800) 222-9323	Toll-free for U.S. and Canada
(512) 602-5651	Direct dial worldwide

BLOCK DIAGRAM



ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order numbers (Valid Combinations) are formed by a combination of the elements below.



Valid Combinations	
ELANSC300–25	KC
ELANSC300–33	KC
ELANSC300–25	KI
ELANSC300–33	KI
ELANSC300–25	VC
ELANSC300–33	VC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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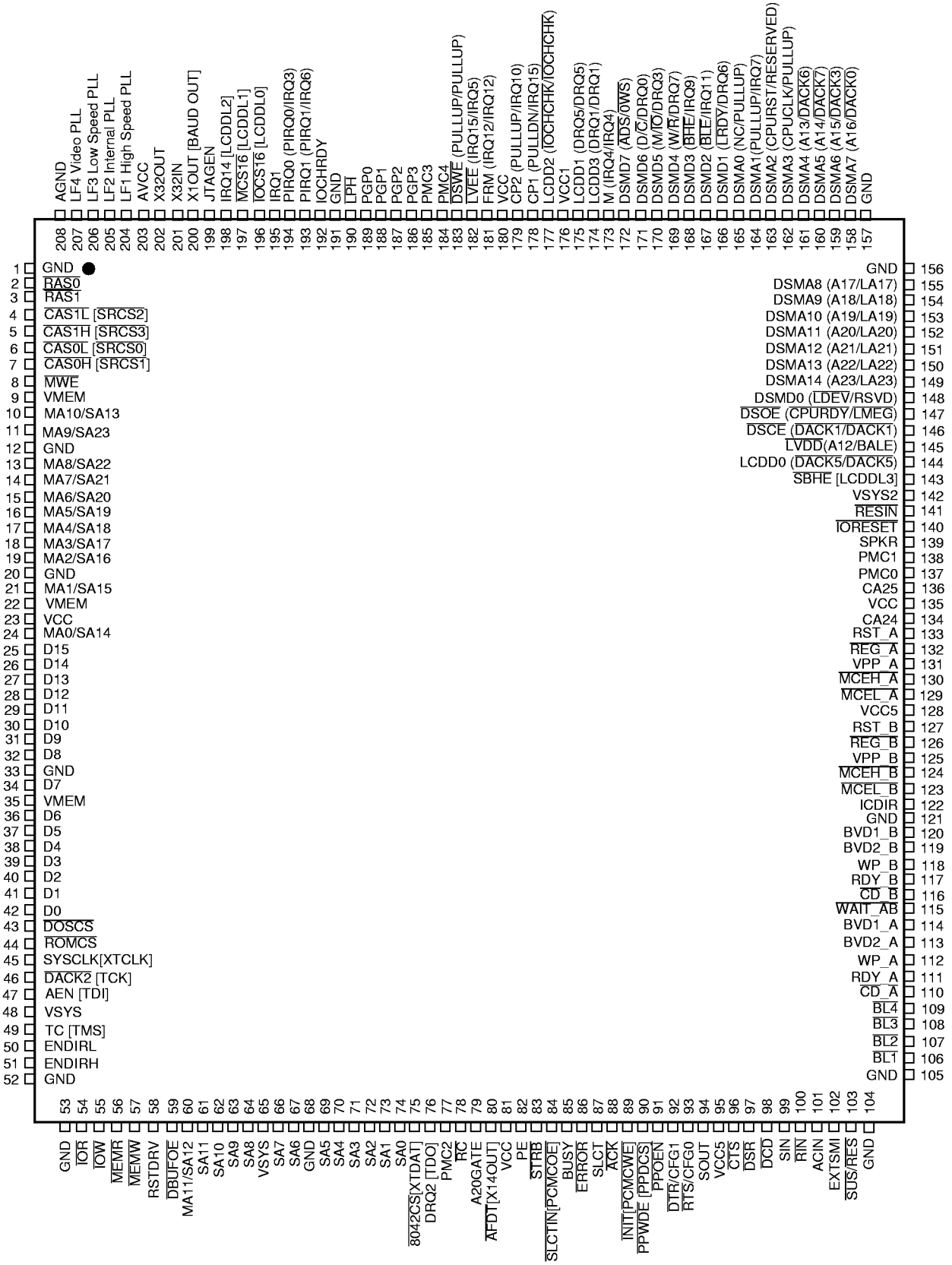
CONNECTION DIAGRAM



ÉLANSC300 MICROCONTROLLER PIN DESIGNATIONS

This section, beginning with the Connection Diagram on the preceding page, identifies the pins of the ÉlanSC300 microcontroller and lists the signals associated with each pin. The table beginning on page 15 lists the pins sorted by pin number; the table beginning on page 17 lists the pins sorted by pin name along with the corresponding pin number, functional grouping, Pin State table number, and the page number where a description of the pin is located. Tables 2–11, beginning on page 25, group these signals according to function.

The Signal Name column in the pin designation table (sorted by pin number), and in Tables 2–11, is decoded as follows:

NAME1 / NAME2 [NAME3] (NAME4 / NAME5)

NAME1 - This is the pin function when the ÉlanSC300 microcontroller has been configured, at reset, for the internal LCD Controller mode of operation. If the pin only has one function regardless of the mode, NAME1 is the only name given.

NAME2 - This is the secondary pin function (by default) when the ÉlanSC300 microcontroller has been configured, at reset, for the internal LCD Controller mode of operation. If the pin always has two functions regardless of the mode, NAME1 followed by NAME2 are the only names given.

NAME3 - This is a tertiary pin function that must be enabled specifically by firmware. As an example, for pins $\overline{\text{DACK2}}$[TCK], DRQ2[TDO], AEN[TDI], and TC[TMS], the NAME3 function is selected by the JTAGEN pin being asserted High (JTAG ENABLE).

NAME4 - Designates the pin function when the ÉlanSC300 microcontroller has been configured, at reset, for the Local Bus mode of operation.

NAME5 - Designates the pin function when the ÉlanSC300 microcontroller has been configured, at reset, for the Maximum ISA mode of operation.

RSVD - Pins marked with this designator are required to remain unconnected.

PULLUP - Needs external pull-up resistor.

PULLDN - Needs external pull-down resistor.

The Signal Name column in the pin designation table (sorted by pin name), beginning on page 17, contains an alphabetical listing of all pin names, followed by their corresponding alternate pin names in the applicable format from those listed here:

NAME1 / NAME2 [NAME3] (NAME4 / NAME5)

NAME2 / NAME1 [NAME3] (NAME4 / NAME5)

[NAME3] (NAME4 / NAME5) NAME1 / NAME2

(NAME4 / NAME5) NAME1 / NAME2 [NAME3]

(NAME5 / NAME4) NAME1 / NAME2 [NAME3]

For more information about how pins are shared and which functions are available in each bus mode, see “Alternate Pin Functions” on page 68.

PIN DESIGNATIONS (SORTED BY PIN NUMBER)

Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)
1	GND	44	ROMCS	87	SLCT
2	RAS0	45	SYSCLK [XTCLK]	88	ACK
3	RAS1	46	DACK2 [TCLK]	89	INIT [PCMCWE]
4	CAS1L [SRCS2]	47	AEN [TDI]	90	PPDWE [PPDCS]
5	CAS1H [SRCS3]	48	VSYS	91	PPOEN
6	CAS0L [SRCS0]	49	TC [TMS]	92	DTR/CFG1
7	CAS0H [SRCS1]	50	ENDIRL	93	RTS/CFG0
8	MWE	51	ENDIRH	94	SOUT
9	VMEM	52	GND	95	VCC5
10	MA10/SA13	53	GND	96	CTS
11	MA9/SA23	54	IOR	97	DSR
12	GND	55	IOW	98	DCD
13	MA8/SA22	56	MEMR	99	SIN
14	MA7/SA21	57	MEMW	100	RIN
15	MA6/SA20	58	RSTDRV	101	ACIN
16	MA5/SA19	59	DBUFOE	102	EXTSMI
17	MA4/SA18	60	MA11/SA12	103	SUS/RES
18	MA3/SA17	61	SA11	104	GND
19	MA2/SA16	62	SA10	105	GND
20	GND	63	SA9	106	BL1
21	MA1/SA15	64	SA8	107	BL2
22	VMEM	65	VSYS	108	BL3
23	VCC	66	SA7	109	BL4
24	MA0/SA14	67	SA6	110	CD_A
25	D15	68	GND	111	RDY_A
26	D14	69	SA5	112	WP_A
27	D13	70	SA4	113	BVD2_A
28	D12	71	SA3	114	BVD1_A
29	D11	72	SA2	115	WAIT_AB
30	D10	73	SA1	116	CD_B
31	D9	74	SA0	117	RDY_B
32	D8	75	8042CS [XTDAT]	118	WP_B
33	GND	76	DRQ2 [TDO]	119	BVD2_B
34	D7	77	PMC2	120	BVD1_B
35	VMEM	78	RC	121	GND
36	D6	79	A20GATE	122	ICDIR
37	D5	80	AFDT [X14OUT]	123	MCEL_B
38	D4	81	VCC	124	MCEH_B
39	D3	82	PE	125	VPP_B
40	D2	83	STRB	126	REG_B
41	D1	84	SLCTIN [PCMCOE]	127	RST_B
42	D0	85	BUSY	128	VCC5
43	DOSCS	86	ERROR	129	MCEL_A

PIN DESIGNATIONS (SORTED BY PIN NUMBER) (CONTINUED)

Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)
130	MCEH_A	157	GND	184	PMC4
131	VPP_A	158	DSMA7 (A16/DACK0)	185	PMC3
132	REG_A	159	DSMA6 (A15/DACK3)	186	PGP3
133	RST_A	160	DSMA5 (A14/DACK7)	187	PGP2
134	CA24	161	DSMA4 (A13/DACK6)	188	PGP1
135	VCC	162	DSMA3 (CPUCLK/PULLUP)	189	PGP0
136	CA25	163	DSMA2 (CPURST/RSVD)	190	LPH
137	PMC0	164	DSMA1 (PULLUP/IRQ7)	191	GND
138	PMC1	165	DSMA0 (NC/PULLUP)	192	IOCHRDY
139	SPKR	166	DSMD1 (LRDY/DRQ6)	193	PIRQ1 (PIRQ1/IRQ6)
140	IORESET	167	DSMD2 (BLE/IRQ11)	194	PIRQ0 (PIRQ0/IRQ3)
141	RESIN	168	DSMD3 (BHE/IRQ9)	195	IRQ1
142	VSYS2	169	DSMD4 (W/R/DRQ7)	196	IOCS16 [LCDDL0]
143	SBHE [LCDDL3]	170	DSMD5 (M/IO/DRQ3)	197	MCS16 [LCDDL1]
144	LCDD0 (DACK5/DACK5)	171	DSMD6 (D/C/DRQ0)	198	IRQ14 [LCDDL2]
145	LVDD (A12/BALE)	172	DSMD7 (ADS/0WS)	199	JTAGEN
146	DSCE (DACK1/ DACK1)	173	M (IRQ4/IRQ4)	200	X1OUT [BAUD_OUT]
147	DSOE (CPURDY/LMEG)	174	LCDD3 (DRQ1/DRQ1)	201	X32IN
148	DSMD0 (LDEV/RSVD)	175	LCDD1 (DRQ5/DRQ5)	202	X32OUT
149	DSMA14 (A23/LA23)	176	VCC1	203	AVCC
150	DSMA13 (A22/LA22)	177	LCDD2 (IOCHCHK/ IOCHCHK)	204	LF1
151	DSMA12 (A21/LA21)	178	CP1 (PULLDN/IRQ5)	205	LF2
152	DSMA11 (A20/LA20)	179	CP2 (PULLUP/IRQ10)	206	LF3
153	DSMA10 (A19/LA19)	180	VCC	207	LF4
154	DSMA9 (A18/LA18)	181	FRM (IRQ12/IRQ12)	208	AGND
155	DSMA8 (A17/LA17)	182	LVEE (IRQ15/IRQ15)	-	-
156	GND	183	DSWE (PULLUP/PULLUP)	-	-

PIN DESIGNATIONS (SORTED BY PIN NAME)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
(0WS/ADS) DSMD7	172	Maximum ISA bus interface	8	43
8042CS [XTDAT]	75	Keyboard interface	3	37
(A12/BALE) LVDD	173	Local bus interface	8	42
(A13/DACK6) DSMA4	161	Local bus interface	8	42
(A14/DACK7) DSMA5	160	Local bus interface	8	42
(A15/DACK3) DSMA6	159	Local bus interface	8	42
(A16/DACK0) DSMA7	158	Local bus interface	8	42
(A17/LA17) DSMA8	155	Local bus interface	8	42
(A18/LA18) DSMA9	154	Local bus interface	8	42
(A19/LA19) DSMA10	153	Local bus interface	8	42
(A20/LA20) DSMA11	152	Local bus interface	8	42
A20GATE	79	Keyboard interface	3	37
(A21/LA21) DSMA12	151	Local bus interface	8	42
(A22/LA22) DSMA13	150	Local bus interface	8	42
(A23/LA23) DSMA14	149	Local bus interface	8	42
ACIN	101	Power management interface	6	40
ACK	88	Parallel port interface	4	37
(ADS/0WS) DSMD7	172	Local bus interface	8	42
AEN [TDI]	47	System interface	2	35
AFDT [X14OUT]	80	Parallel port interface	4	37
AGND	208	Power	10	44
AVCC	203	Power	10	44
(BALE/A12) LVDD	173	Maximum ISA bus interface	8	43
[BAUD_OUT] X1OUT	200	Miscellaneous interface	9	42
(BHE/IRQ9) DSMD3	168	Local bus interface	8	42
BL1	106	Power management interface	6	40
BL2	107	Power management interface	6	40
BL3	108	Power management interface	6	40
BL4	109	Power management interface	6	40
(BLE/IRQ11) DSMD2	167	Local bus interface	8	42
BUSY	85	Parallel port interface	4	37
BVD1_A (STSCHG_A)	114	PCMCIA interface	7	38
BVD1_B (STSCHG_B)	120	PCMCIA interface	7	38
BVD2_A (SPKR_A)	113	PCMCIA interface	7	38
BVD2_B (SPKR_B)	119	PCMCIA interface	7	38
CA24	134	PCMCIA interface	7	38
CA25	136	PCMCIA interface	7	38
CAS0H [SRCS1]	7	Memory bus interface	1	34
CAS0L [SRCS0]	6	Memory bus interface	1	34
CAS1H [SRCS3]	5	Memory bus interface	1	34
CAS1L [SRCS2]	4	Memory bus interface	1	34
CD_A	110	PCMCIA interface	7	38

PIN DESIGNATIONS (SORTED BY PIN NAME) (CONTINUED)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
$\overline{CD\_B}$	116	PCMCIA interface	7	38
CFG0/$\overline{RTS}$	93	Serial port interface	5	38
CFG1/$\overline{DTR}$	92	Serial port interface	5	38
CP1 (PULLDN/IRQ5)	178	Display interface	8	41
CP2 (PULLUP/IRQ10)	179	Display interface	8	41
(CPUCLK/PULLUP) DSMA3	162	Local bus interface	8	43
($\overline{CPURDY}$/$\overline{LMEG}$) $\overline{DSOE}$	147	Local bus interface	8	43
(CPURST/RSVD) DSMA2	163	Local bus interface	8	43
$\overline{CTS}$	96	Serial port interface	5	38
D0	42	System interface	2	35
D1	41	System interface	2	35
D10	30	System interface	2	35
D11	29	System interface	2	35
D12	28	System interface	2	35
D13	27	System interface	2	35
D14	26	System interface	2	35
D15	25	System interface	2	35
D2	40	System interface	2	35
D3	39	System interface	2	35
D4	38	System interface	2	35
D5	37	System interface	2	35
D6	36	System interface	2	35
D7	34	System interface	2	35
D8	32	System interface	2	35
D9	31	System interface	2	35
($\overline{DACK0}$/A16) DSMA7	158	Maximum ISA bus interface	8	43
($\overline{DACK1}$/$\overline{DACK1}$) $\overline{DSCE}$	146	Local and maximum ISA bus interface	8	43
$\overline{DACK2}$ [TCK]	46	System and maximum ISA bus interface	2	35, 44
($\overline{DACK3}$/A15) DSMA6	159	Maximum ISA bus interface	8	43
($\overline{DACK5}$/$\overline{DACK5}$) LCDD0	144	Local and maximum ISA bus interface	8	43
($\overline{DACK6}$/A13) DSMA4	161	Maximum ISA bus interface	8	43
($\overline{DACK7}$/A14) DSMA5	160	Maximum ISA bus interface	8	43
$\overline{DBUFOE}$	59	System interface	2	35
(D/$\overline{C}$/DRQ0) DSMD6	171	Local bus interface	8	43
$\overline{DCD}$	98	Serial port interface	5	38
$\overline{DOSCS}$	43	Memory bus interface	1	34
(DRQ0/D/C) DSMD6	171	Maximum ISA bus interface	8	43
(DRQ1/DRQ1) LCDD3	174	Local and maximum ISA bus interface	8	43
DRQ2 [TDO]	76	System and maximum ISA bus interface	2	35, 44
(DRQ3/M/$\overline{IO}$) DSMD5	170	Maximum ISA bus interface	8	43
(DRQ5/DRQ5) LCCD1	175	Local and maximum ISA bus interface	8	43
(DRQ6/$\overline{LRDY}$) DSMD1	166	Maximum ISA bus interface	8	43
(DRQ7/W/$\overline{R}$) DSMD4	169	Maximum ISA bus interface	8	43

PIN DESIGNATIONS (SORTED BY PIN NAME) (CONTINUED)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
DSCE (DACK1/DACK1)	146	Display interface	8	41
DSMA0 (NC/PULLUP)	165	Display interface	8	41
DSMA1 (PULLUP/IRQ7)	164	Display interface	8	41
DSMA10 (A19/LA19)	153	Display interface	8	41
DSMA11 (A20/LA20)	152	Display interface	8	41
DSMA12 (A21/LA21)	151	Display interface	8	41
DSMA13 (A22/LA22)	150	Display interface	8	41
DSMA14 (A23/LA23)	149	Display interface	8	41
DSMA2 (CPURST/RSVD)	163	Display interface	8	41
DSMA3 (CPUCLK/PULLUP)	162	Display interface	8	41
DSMA4 (A13/DACK6)	161	Display interface	8	41
DSMA5 (A14/DACK7)	160	Display interface	8	41
DSMA6 (A15/DACK3)	159	Display interface	8	41
DSMA7 (A16/DACK0)	158	Display interface	8	41
DSMA8 (A17/LA17)	155	Display interface	8	41
DSMA9 (A18/LA18)	154	Display interface	8	41
DSMD0 (LDEV/RSVD)	148	Display interface	8	41
DSMD1 (LRDY/DRQ6)	166	Display interface	8	41
DSMD2 (BLE/IRQ11)	167	Display interface	8	41
DSMD3 (BHE/IRQ9)	168	Display interface	8	41
DSMD4 (W/R/DRQ7)	169	Display interface	8	41
DSMD5 (M/IO/DRQ3)	170	Display interface	8	41
DSMD6 (D/C/DRQ0)	171	Display interface	8	41
DSMD7 (ADS/0WS)	172	Display interface	8	41
DSOE (CPURDY/LMEG)	147	Display interface	8	41
DSR	97	Serial port interface	5	38
DSWE (PULLUP/PULLUP)	183	Display interface	8	41
DTR/CFG1	92	Serial port interface	5	38
ENDIRH	51	System interface	2	35
ENDIRL	50	System interface	2	35
ERROR	86	Parallel port interface	4	37
EXTSMI	102	Power management interface	6	40
FRM (IRQ12/IRQ12)	181	Display Interface	8	41
GND	1, 12, 20, 33, 52, 53, 68, 104, 105, 121, 156, 157, 191	Power	10	45
ICDIR	122	PCMCIA interface	7	39
INIT [PCMCWE]	89	Parallel port interface	4	37
(IOCHCHK/IOCHCHK)	177	Maximum ISA bus interface	8	43
IOCHRDY	192	System interface	2	35
IOCS16 [LCDDL0]	196	System interface	8	35

PIN DESIGNATIONS (SORTED BY PIN NAME) (CONTINUED)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
(IOIS16A) WP_A	112	PCMCIA interface	7	39
(IOIS16B) WP_B	118	PCMCIA interface	7	39
IOR	54	System interface	2	35
IORESET	140	Reset and power	9	45
IOW	55	System interface	2	36
(IREQ_A) RDY_A	111	PCMCIA interface	7	39
(IREQ_B) RDY_B	117	PCMCIA interface	7	39
IRQ1	195	System and maximum ISA bus interface	2	36, 44
(IRQ10/PULLUP) CP2	179	Maximum ISA bus interface	8	44
(IRQ11/BLE) DSMD2	167	Maximum ISA bus interface	8	44
(IRQ12/IRQ12) FRM	181	Local and maximum ISA bus Interface	8	44
IRQ14 [LCDDL2]	198	System and maximum ISA bus interface	8	36, 44
(IRQ15/IRQ15) LVEE	182	Local and maximum ISA bus interface	8	44
(IRQ3/PIRQ0) PIRQ0	194	Maximum ISA bus interface	2	44
(IRQ4/IRQ4) M	173	Local and maximum ISA bus interface	8	44
(IRQ5/PULLDN) CP1	178	Maximum ISA bus interface	8	44
(IRQ6/PIRQ1) PIRQ1	193	Maximum ISA bus interface	2	44
(IRQ7/PULLUP) DSMA1	164	Maximum ISA bus interface	8	44
(IRQ9/BHE) DSMD3	168	Maximum ISA bus interface	8	44
JTAGEN	199	JTAG boundary scan interface	9	44
(LA17/A17) DSMA8	155	Maximum ISA bus interface	8	44
(LA18/A18) DSMA9	154	Maximum ISA bus interface	8	44
(LA19/A18) DSMA10	153	Maximum ISA bus interface	8	44
(LA20/A20) DSMA11	152	Maximum ISA bus interface	8	44
(LA21/A21) DSMA12	151	Maximum ISA bus interface	8	44
(LA22/A22) DSMA13	150	Maximum ISA bus interface	8	44
(LA23/A23) DSMA14	149	Maximum ISA bus interface	8	44
LCDD0 (DACK5/DACK5)	144	Display interface	8	41
LCDD1 (DRQ5/DRQ5)	175	Display interface	8	41
LCDD2 (IOCHCHK/IOCHCHK)	177	Display interface	8	41
LCDD3 (DRQ1/DRQ1)	174	Display interface	8	41
[LCDDL0] IOCS16	196	Display interface	8	35
[LCDDL1] MCS16	197	Display interface	8	36
[LCDDL2] IRQ14	198	Display interface	8	36
[LCDDL3] SBHE	143	Display interface	8	36
(LDEV/RSVD) DSMD0	148	Local bus interface	8	43
LF1	204	Miscellaneous interface	9	42
LF2	205	Miscellaneous interface	9	42
LF3	206	Miscellaneous interface	9	42
LF4	207	Miscellaneous interface	9	42
(LMEG/CPURDY) DSOE	147	Maximum ISA bus interface	8	44
LPH	190	Power management interface	6	40
(LRDY/DRQ6) DSMD1	166	Local bus interface	8	43

PIN DESIGNATIONS (SORTED BY PIN NAME) (CONTINUED)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
LVDD (A12/BALE)	173	Display interface	8	41
LVEE (IRQ15/IRQ15)	182	Display interface	8	41
M (IRQ4/IRQ4)	173	Display interface	8	42
MA0/SA14	24	Memory bus interface	1	34
MA1/SA15	21	Memory bus interface	1	34
MA10/SA13	10	Memory bus interface	1	34
MA11/SA12	60	Memory bus interface	1	34
MA2/SA16	19	Memory bus interface	1	34
MA3/SA17	18	Memory bus interface	1	34
MA4/SA18	17	Memory bus interface	1	34
MA5/SA19	16	Memory bus interface	1	34
MA6/SA20	15	Memory bus interface	1	34
MA7/SA21	14	Memory bus interface	1	34
MA8/SA22	13	Memory bus interface	1	34
MA9/SA23	11	Memory bus interface	1	34
MCEH_A	130	PCMCIA interface	7	39
MCEH_B	124	PCMCIA interface	7	39
MCEL_A	129	PCMCIA interface	7	39
MCEL_B	123	PCMCIA interface	7	39
MCS16 [LCDDL1]	197	System interface	8	36
MEMR	56	System interface	2	36
MEMW	57	System interface	2	36
(M/IO/DRQ3) DSMD5	170	Display interface	8	41
MWE	8	Memory bus interface	1	34
[PCMCOE] SLCTIN	84	PCMCIA interface	4	38
[PCMCWE] INIT	89	PCMCIA interface	4	39
PE	82	Parallel port interface	4	37
PGP0	189	Power management interface	6	40
PGP1	188	Power management interface	6	40
PGP2	187	Power management interface	6	40
PGP3	186	Power management interface	6	40
PIRQ0 (PIRQ0/IRQ3)	194	System and maximum ISA bus interface	2	36, 44
(PIRQ0/IRQ3) PIRQ0	194	System and maximum ISA bus interface	2	36, 44
PIRQ1 (PIRQ1/IRQ6)	193	System and maximum ISA bus interface	2	36, 44
(PIRQ1/IRQ6) PIRQ1	193	System and maximum ISA bus interface	2	36, 44
PMC0	137	Power management interface	6	40
PMC1	138	Power management interface	6	40
PMC2	77	Power management interface	6	40
PMC3	185	Power management interface	6	40
PMC4	184	Power management interface	6	40
[PPDCS] PPDWE	90	Parallel port interface	4	37
PPDWE [PPDCS]	90	Parallel port interface	4	37
PPOEN	91	Parallel port interface	4	37

PIN DESIGNATIONS (SORTED BY PIN NAME) (CONTINUED)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
$\overline{RAS0}$	2	Memory bus interface	1	34
$\overline{RAST}$	3	Memory bus interface	1	34
$\overline{RC}$	78	Keyboard interface	3	37
RDY_A ($\overline{IREQ\_A}$)	111	PCMCIA interface	7	39
RDY_B ($\overline{IREQ\_B}$)	117	PCMCIA interface	7	39
$\overline{REG\_A}$	132	PCMCIA interface	7	39
$\overline{REG\_B}$	126	PCMCIA interface	7	39
$\overline{RESIN}$	141	Reset and power	9	45
$\overline{RIN}$	100	Serial port interface	5	38
$\overline{ROMCS}$	44	Memory bus interface	1	34
RST_A	133	PCMCIA interface	7	39
RST_B	127	PCMCIA interface	7	39
RSTDRV	58	System interface	2	36
$\overline{RTS}$/CFG0	93	Serial port interface	5	38
SA0	74	System interface	2	36
SA1	73	System interface	2	36
SA10	62	System interface	2	36
SA11	61	System interface	2	36
SA12	60	System interface	2	34
SA13/MA10	10	System interface	1	34
SA14/MA0	24	System interface	1	34
SA15/MA1	21	System interface	1	34
SA16/MA2	19	System interface	1	34
SA17/MA3	18	System interface	1	34
SA18/MA4	17	System interface	1	34
SA19/MA5	16	System interface	1	34
SA2	72	System interface	2	36
SA20/MA6	15	System interface	1	34
SA21/MA7	14	System interface	1	34
SA22/MA8	13	System interface	1	34
SA23/MA9	11	System interface	1	34
SA3	71	System interface	2	36
SA4	70	System interface	2	36
SA5	69	System interface	2	36
SA6	67	System interface	2	36
SA7	66	System interface	2	36
SA8	64	System interface	2	36
SA9	63	System interface	2	36
$\overline{SBHE}$ [LCDDL3]	143	System interface	8	36
SIN	99	Serial port interface	5	38
SLCT	87	Parallel port interface	4	37
$\overline{SLCTIN}$ [$\overline{PCMCOE}$]	84	Parallel port interface	4	38
SOUT	94	Serial port interface	5	38

PIN DESIGNATIONS (SORTED BY PIN NAME) (CONTINUED)

Signal Name (Alternate Functions)	Pin No.	Functional Group	Pin State Table Number	Description Page Number
SPKR	139	Miscellaneous interface	9	36
($\overline{\text{SPKR\_A}}$) BVD2_A	113	PCMCIA interface	7	38
($\overline{\text{SPKR\_B}}$) BVD2_B	119	PCMCIA interface	7	38
[$\overline{\text{SRCS0}}$] $\overline{\text{CAS0L}}$	6	Memory bus interface	1	34
[$\overline{\text{SRCS1}}$] $\overline{\text{CAS0H}}$	7	Memory bus interface	1	34
[$\overline{\text{SRCS2}}$] $\overline{\text{CAS1L}}$	4	Memory bus interface	1	34
[$\overline{\text{SRCS3}}$] $\overline{\text{CAS1H}}$	5	Memory bus interface	1	34
$\overline{\text{STRB}}$	83	Parallel port interface	4	38
($\overline{\text{STSCHG\_A}}$) BVD1_A	114	PCMCIA interface	7	38
($\overline{\text{STSCHG\_B}}$) BVD1_B	120	PCMCIA interface	7	38
$\overline{\text{SUS/RES}}$	103	Power management interface	6	40
SYSCLK [XTCLK]	45	System interface	2	37
TC [TMS]	49	System interface	2	37
[TCK] $\overline{\text{DACK2}}$	46	JTAG boundary scan interface	2	44
[TDI] AEN	47	JTAG boundary scan interface	2	44
[TDO] DRQ2	76	JTAG boundary scan interface	2	44
[TMS] TC	49	JTAG boundary scan interface	2	44
VCC	23, 81, 135, 180	Power	10	45
VCC1	176	Power	10	45
VCC5	95, 128	Power	10	45
VMEM	9, 22, 35	Power	10	45
VPP_A	131	PCMCIA interface	7	39
VPP_B	125	PCMCIA interface	7	39
VSYS	48, 65	Power	10	45
VSYS2	142	Power	10	45
(W/$\overline{\text{R}}$/DRQ7) DSMD4	169	Local bus interface	8	43
$\overline{\text{WAIT\_AB}}$	115	PCMCIA interface	7	39
WP_A ($\overline{\text{IOIS16A}}$)	112	PCMCIA interface	7	39
WP_B ($\overline{\text{IOIS16B}}$)	118	PCMCIA interface	7	39
X1OUT [BAUD_OUT]	200	Miscellaneous interface	9	42
[X14OUT] $\overline{\text{AFDT}}$	80	Miscellaneous and parallel port interface	4	37, 42
X32IN	201	Miscellaneous interface	9	42
X32OUT	202	Miscellaneous interface	9	42
[XTCLK] SYSCLK	45	System and keyboard interface	2	37
[XTDAT] $\overline{\text{8042CS}}$	75	Keyboard interface	3	37

PIN STATE TABLES

The Pin State tables beginning on page 25 are grouped by function based on their primary function when the ÉlanSC300 microcontroller is configured at reset for the internal LCD Controller mode (NAME1). See page 14 for a description of NAME1. The Pin State tables also show the I/O type and reset state for those pins that have been configured at reset for either Local Bus mode or Maximum ISA Bus mode.

Pin Characteristics

The following information clarifies the meaning of the Pin State tables beginning on page 25:

The letters in the **I/O Type** column of Tables 1–10 mean the following:

I – Input

O – Output

STI – Schmitt Trigger Input

B – Bidirectional

A – Analog

The **Term** column refers to internal termination. The letters in this column of Tables 1–10 mean the following:

PD – Pull-down resistor

PU – Pull-up resistor

The symbols (letters) in the **Drive Type** column specify the drive capability of output pins. These specifications can be found in the DC Characteristics section beginning on page 80 of this document. For a more complete description of I/O Drive Types, see “Derating Curves” on page 84 and Table 48 on page 84.

The **Clock Off** column describes the logic level of the I/O pins while the ÉlanSC300 microcontroller is in any of the power management modes where the CPU clock is stopped, and power is still applied to both the VCCIO and VCC clamp supply pins associated with that I/O pin. For Doze mode, the data reflects a situation in which the internal CGA controller video refresh is disabled.

The **Reset State** column lists the I/O pin voltage level when all of the VCC pins are stable and the $\overline{\text{RESIN}}$ input is active. The level of the VCC pins correlating to this data is shown in Table 1.

Table 1. I/O Pin Voltage Level

	Internal CGA (V)	Local Bus (V)	Maximum ISA (V)
VCC	3.3	3.3	3.3
AVCC	3.3	3.3	3.3
VCC5	5.0	5.0	5.0
VSYS2	3.3	3.3	5.0
VSYS	5.0	5.0	5.0
VMEM	3.3	3.3	3.3
VCC1	3.3	3.3	3.3

The **VCCIO** column refers to the voltage supply pin on the ÉlanSC300 microcontroller that is directly connected to the output driver for the specified signal pin.

The **VCC Clamp** column refers to the voltage supply pin on the ÉlanSC300 microcontroller that is directly connected to the ESD protection diode (cathode) for the specified signal pin. Any pin with a 5-V VCC Clamp is a “5-V safe” input.

The **Spec. Load** (specification load) column is used to determine derated AC timing. See “Derating Curves” on page 84 of this data sheet.

Table 2. Memory Bus Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Reset State (volts)				VCC Clamp	Spec. Load (pF)
					Clock Off	Internal CGA	Local Bus	Max ISA	VCCIO		
$\overline{\text{RAS0}}$ [1,3]	2	O		E,D,C	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	50
$\overline{\text{RAS1}}$ [1,3]	3	O		E,D,C	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	50
$\overline{\text{CAS1L}}$ [$\overline{\text{SRCS2}}$] [1,2]	4	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
$\overline{\text{CAS1H}}$ [$\overline{\text{SRCS3}}$] [1,2]	5	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
$\overline{\text{CAS0L}}$ [$\overline{\text{SRCS0}}$] [1,2]	6	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
$\overline{\text{CAS0H}}$ [$\overline{\text{SRCS1}}$] [1,2]	7	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
MA10/SA13 [3]	10	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA9/SA23 [3]	11	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA8/SA22 [3]	13	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA7/SA21 [3]	14	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA6/SA20 [3]	15	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA5/SA19 [3]	16	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA4/SA18 [3]	17	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA3/SA17 [3]	18	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA2/SA16 [3]	19	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA1/SA15 [3]	21	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA0/SA14 [3]	24	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
$\overline{\text{MWE}}$ [3]	8	O		E,D,C	1	3.3	3.3	3.3	VMEM	VMEM	70
$\overline{\text{ROMCS}}$	44	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{DOSCS}}$	43	O		B	1	5.0	5.0	5.0	VSYS	VCC5	50

Notes:

1. *These signals are active during reset.*
2. *These pins always default to their DRAM interface function.*
3. *The drive strength for these pins is programmable. E is the default.*

All inputs that have VCC Clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 3. System Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
MA11/SA12	60	O		E	0	5.0	5.0	5.0	VSYS	VCC5	70
SA11	61	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA10	62	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA9	63	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA8	64	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA7	66	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA6	67	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA5	69	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA4	70	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA3	71	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA2	72	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA1	73	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA0	74	O		D	0	0.0	0.0	0.0	VSYS	VCC5	70
D15 [2]	25	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D14[2]	26	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D13[2]	27	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D12[2]	28	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D11[2]	29	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D10[2]	30	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D9[2]	31	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D8[2]	32	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D7[2]	34	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D6[2]	36	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D5[2]	37	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D4[2]	38	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D3[2]	39	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D2[2]	40	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D1[2]	41	B	PD	E,D,C	0	0.0	3.3	0.0	VMEM	VMEM	70
D0[2]	42	B	PD	E,D,C	0	0.0	3.3	0.0	VMEM	VMEM	70
SYSCLK [XTCLK][1]	45	O(STI)		B	0(–)	5.0/0	5.0/0	5.0/0	VSYS	VCC5	30
IRQ1	195	I	PU	–	–	4.4	4.4	4.4	VCC1	VCC5	
PIRQ1 (PIRQ1/IRQ6)	193	I	PU	–(–/–)	–(–/–)	3.3	3.3	3.3	VCC1	VCC5	
PIRQ0(PIRQ0/IRQ3)	194	I	PU	–(–/–)	–(–/–)	3.3	3.3	3.3	VCC1	VCC5	
$\overline{\text{DACK2}}$ [TCK]	46	O(I)		B	1	5.0	5.0	5.0	VSYS	VCC5	30
DRQ2 [TDO]	76	I(O)	PD	A	–	0.0	0.0	0.0	VSYS	VCC5	30

Table 3. System Interface (Continued)

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
AEN [TDI]	47	O(I)		B	1	0.0	0.0	0.0	VSYS	VCC5	30
TC [TMS]	49	O(I)		B	0	0.0	0.0	0.0	VSYS	VCC5	30
ENDIRL	50	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
ENDIRH	51	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{DBUFOE}}$	59	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{IOR}}$	54	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
$\overline{\text{IOW}}$	55	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
$\overline{\text{MEMR}}$	56	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
$\overline{\text{MEMW}}$	57	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
RSTDRV	58	O		A	0	5.0	5.0	5.0	VSYS	VCC5	30
IOCHRDY	192	STI	PU	–	–	3.3	3.3	3.3	VCC1	VCC5	
$\overline{\text{IOCS16}}$ [LCDDL0]	196	I [B]		C	– [0]	3.3	3.3	3.3	VCC1	VCC5	70
$\overline{\text{MCS16}}$ [LCDDL1]	197	I [B]		C	– [0]	3.3	3.3	3.3	VCC1	VCC5	70
IRQ14 [LCDDL2]	198	I [B]		C	– [0]	0.0	0.0	0.0	VCC1	VCC5	70
$\overline{\text{SBHE}}$ [LCDDL3]	143	O [B]		C	0[0]	0.0	0.0	0.0	VSYS2	VCC5	70

Notes:

1. *Reset State SYSCLK frequency is 4.6 MHz.*
2. *The drive strength for these pins is programmable. E is the default.*

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 4. Keyboard Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{8042CS}$ [XTDAT]	75	O(STI)		B	1(–)	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{RC}$	78	I	PU	–	–	5.0	5.0	5.0	VSYS	VCC5	
A20GATE	79	I	PU	–	–	5.0	5.0	5.0	VSYS	VCC5	

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 5. Parallel Port Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{AFDT}$ [X14OUT][1]	80	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
$\overline{INIT}$ [$\overline{PCMCWE}$][1]	89	O		D	Last state	0.0	0.0	0.0	VCC5	VCC5	100
$\overline{STRB}$[1]	83	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
$\overline{SLCTIN}$ [$\overline{PCMCOE}$][1]	84	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
$\overline{ACK}$	88	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
BUSY[2]	85	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{ERROR}$	86	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
PE	82	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
SLCT	87	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{PPDWE}$ [$\overline{PPDCS}$]	90	O		B	1(1)	5.0	5.0	5.0	VCC5	VCC5	30
$\overline{PPOEN}$	91	O		B	1(1)	0.0	0.0	0.0	VCC5	VCC5	30

Notes:

1. *These outputs function as open-drain outputs in Normal Parallel Port mode, and function as CMOS drivers when the EPP-MODE configuration bit is set.*
2. *The parallel port interface BUSY input must have an external pullup if the parallel port is to be used in EPP mode. If this pullup is not present, accesses to the parallel port in EPP mode will lock up the system.*

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 6. Serial Port Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{DTR}}$/CFG [1]	92	O		A	Last state	0.0	5.0	0	VCC5	VCC5	50
$\overline{\text{RTS}}$/CFG0 [1]	93	O		A	Last state	0.0	0.0	5.0	VCC5	VCC5	50
SOUT	94	O		A	Last state	0.0	0.0	5.0	VCC5	VCC5	50
$\overline{\text{CTS}}$	96	I	PU		–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{DCD}}$	98	I	PU		–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{DSR}}$	97	I	PU		–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{RIN}}$	100	I	PU		–	5.0	5.0	5.0	VCC5	VCC5	
SIN	99	I	PU		–	5.0	5.0	5.0	VCC5	VCC5	

Notes:

1. These pins are terminated externally per bus option selection.

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 7. Power Management Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
ACIN	101	STI	PD	–	–	0.0	0.0	0.0	VCC5	VCC5	
EXTSMI	102	STI	PD	–	–	0.0	0.0	0.0	VCC5	VCC5	
$\overline{\text{SUS}}$/$\overline{\text{RES}}$	103	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
PMC4[1]	184	O		B	Active	0.0	0.0	0.0	VCC1	VCC5	50
PMC3[1]	185	O		B	Active	3.3	3.3	3.3	VCC1	VCC5	50
PMC2[1]	77	O		B	Active	0.0	0.0	0.0	VSYS	VCC5	50
PMC1[1]	138	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
PMC0[1]	137	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
PGP3	186	O		B	Active	3.3	3.3	3.3	VCC1	VCC5	50
PGP2	187	O		B	Active	3.3	3.3	3.3	VCC1	VCC5	50
PGP1	188	B		B	Active	3.3	3.3	3.3	VCC1	VCC5	50
PGP0	189	B		B	Active	0.0	0.0	0.0	VCC1	VCC5	50
$\overline{\text{BL1}}$	106	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{BL2}}$	107	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{BL3}}$	108	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{BL4}}$	109	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{LPH}}$	190	O		B	Active	0.0	0.0	0.0	VCC1	VCC5	50

Notes:

1. PMC outputs: four Low (PMC0, PMC1, PMC2, PMC4), one High (PMC3), default state after reset. All five are programmable as either active High or Low after reset.

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 8. PCMCIA Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{MCEL\_A}}$	129	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
$\overline{\text{MCEH\_A}}$	130	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
VPP_A	131	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
$\overline{\text{REG\_A}}$	132	O		B	0	5.0	5.0	5.0	VCC5	VCC5	50
RST_A[1]	133	O		B	3 state	0.0	0.0	0.0	VCC5	VCC5	50
$\overline{\text{CD\_A}}$	110	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
RDY_A[2]	111	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
WP_A[2]	112	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD2_A[2]	113	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD1_A[2]	114	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
$\overline{\text{WAIT\_AB}}$[2]	115	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
ICDIR	122	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
$\overline{\text{MCEL\_B}}$	123	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
$\overline{\text{MCEH\_B}}$	124	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
VPP_B	125	O		A	Active	0.0	0.0	0.0	VCC5	VCC5	50
$\overline{\text{REG\_B}}$	126	O		A	0	5.0	5.0	5.0	VCC5	VCC5	50
RST_B[1]	127	O		B	3 state	0.0	0.0	0.0	VCC5	VCC5	50
$\overline{\text{CD\_B}}$	116	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
RDY_B[2]	117	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
WP_B[2]	118	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD2_B[2]	119	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD1_B[2]	120	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
CA24	134	O		B	0	0.0	0.0	0.0	VCC5	VCC5	50
CA25	136	O		B	0	0.0	0.0	0.0	VCC5	VCC5	50

Notes:

1. *External weak pull-down resistor is required.*
2. *The reset state of these signals will be zero only if the reset state of the PCMCIA power source is zero. All of these pins are required to be pulled up to the PCMCIA power source externally.*

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 9. Display Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
DSMD7 (ADS/0WS)	172	B (O/I)		C	0 (1/–)	0.0	3.3	3.3	VCC1	VCC5	50
DSMD6 (D/C/ DRQ0)[1]	171	B (O/I)		C	0 (LS/–)	0.0	3.3	0.0	VCC1	VCC5	50
DSMD5 (M/IO/ DRQ3)[1]	170	B (O/I)		C	0 (LS/–)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD4 (W/R/ DRQ7)[1]	169	B (O/I)		C	0 (LS/–)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD3 (BHE/ IRQ9)[1]	168	B (O/I)		C	0 (LS/–)	0.0	0.0	3.3	VCC1	VCC5	50
DSMD2 (BLE/ IRQ11)[1]	167	B (O/I)		C	0 (LS/–)	0.0	0.0	3.3	VCC1	VCC5	50
DSMD1 (LRDY/ DRQ6)	166	B (I/I)		C	0 (–/–)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD0 (LDEV/ RSVD)	148	B (I/O)		C	0 (–/3 state)	0.0	3.3	0.0	VSYS2	VCC5	50
DSMA14 (A23/ LA23)	149	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA13 (A22/ LA22)	150	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA12 (A21/ LA21)	151	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA11 (A20/ LA20)	152	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA10 (A19/ LA19)	153	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA9 (A18/LA18)	154	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA8 (A17/LA17)	155	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA7 (A16/ DACK0)	158	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA6 (A15/ DACK3)	159	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA5 (A14/ DACK7)	160	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA4 (A13/ DACK6)	161	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA3 (CPUCLK/ PULLUP)[2]	162	O		E	0	3.3	3.3/0	3.3	VCC1	VCC5	50 (30)
DSMA2 (CPURST/ RSVD)	163	O		C	0	3.3	3.3	0.0	VCC1	VCC5	50
DSMA1 (PULLUP/ IRQ7)	164	O (I/I)		C	0 (–/–)	3.3	3.3	3.3	VCC1	VCC5	50
DSMA0 (NC/ PULLUP)	165	O (0/I)		C	0 (0/–)	0.0	3.3	3.3	VCC1	VCC5	50
DSWE (PULLUP/ PULLUP)	183	O (I/I)		B	1 (–/–)	3.3	3.3	3.3	VCC1	VCC5	30
DSOE (CPURDY/ LMEG)	147	O		B	1	5.0	0.0	0.0	VSYS2	VCC5	50
DSCE (DACK1/ DACK1)	146	O		B	1	0.0	3.3	5.0	VSYS2	VCC5	30

Table 9. Display Interface (Continued)

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
LCDD3 (DRQ1 / DRQ1)	174	O (I/I)		C	0 (–/–)	0.0	0.0	0.0	VCC1	VCC5	100
LCDD0 ($\overline{\text{DACK5}}$/ $\overline{\text{DACK5}}$)	144	O		C	0 (1/1)	3.3	3.3	5.0	VSYS2	VCC5	100
LCDD1 (DRQ5/ DRQ5)	175	O (I/I)		C	0 (–/–)	0.0	3.3	0.0	VCC1	VCC5	100
LCDD2 ($\overline{\text{IOCHCHK}}$/ $\overline{\text{IOCHCHK}}$)	177	O (I/I)		C	0 (–/–)	0.0	3.3	3.3	VCC1	VCC5	100
M (IRQ4/IRQ4)	173	O (I/I)		C	0 (–/–)	0.0	3.3	3.3	VCC1	VCC5	100
CP1 (PULLDN/IRQ5)	178	O (I/I)		C	0 (–/–)	0.0	0.0	3.3	VCC1	VCC5	100
CP2 (PULLUP/ IRQ10)	179	O (I/I)		C	0 (–/–)	0.0	0.0	3.3	VCC1	VCC5	100
FRM (IRQ12/IRQ12)	181	O (I/I)		C	0 (–/–)	0.0	3.3	3.3	VCC1	VCC5	100
$\overline{\text{LVEE}}$ (IRQ15/ IRQ15)	182	O (I/I)		B	1 (–/–)	3.3	3.3	3.3	VCC1	VCC5	50
$\overline{\text{LVDD}}$ (A12/ BALE)	145	O		E	1(0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
$\overline{\text{IOCS16}}$ [LCDDL0]	196	I [B]		C	– [0]	3.3	3.3	3.3	VCC1	VCC5	70
$\overline{\text{MCS16}}$ [LCDDL1]	197	I [B]		C	– [0]	3.3	3.3	3.3	VCC1	VCC5	70
IRQ14 [LCDDL2]	198	I [B]		C	– [0]	0.0	0.0	0.0	VCC1	VCC5	70
$\overline{\text{SBHE}}$ [LCDDL3]	143	O [B]		C	0[0]	0.0	0.0	0.0	VSYS2	VCC5	70

Notes:

*1. LS in the **Clock Off** column stands for Last State.*

2. Reset State Local Bus signal loading 920 mV–0 V. For 33-MHz operation, CPUCLK loading = 30 pF.

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 10. Miscellaneous Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{IORESET}}$ [1]	140	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
X32IN[2]	201	I		–	–	640 mV	920/0	920/0	AVCC	AVCC	
X32OUT [3]	202	O		osc.	Active	1.68/0	1.68/0	1.68/0	AVCC	AVCC	
LF1	204	A		–	–	1.52	1.52	1.52	AVCC	AVCC	
LF2	205	A		–	–	1.48	1.48	1.48	AVCC	AVCC	
LF3	206	A		–	–	1.52	1.52	1.52	AVCC	AVCC	
LF4	207	A		–	–	1.68	1.68	1.68	AVCC	AVCC	
X1OUT [BAUD_OUT]	200	O		B	(LS) [4]	0.0	1.24	1.24	VCC1	VCC5	50
$\overline{\text{RESIN}}$	141	STI		–	–	0.0	0.0	0.0	VCC	VCC	
SPKR[4]	139	O		B	(LS) [4]	5.0	5.0	5.0	VCC5	VCC5	50
JTAGEN	199	I	PD	–	–	0.0	0.0	0.0	VCC1	VCC5	

Notes:

1. $\overline{\text{IORESET}}$ *(pin #140) requires an external pull-down resistor (~10K).*
2. *Reset State Local Bus signal and Reset State ISA Max signal: 920 mV–0 V frequency = 32 kHz.*
3. *Reset State signal: 1.68 V–0 V frequency = 32 kHz.*
4. *LS in the* ***Clock Off*** *column stands for Last State.*

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 11. Power Pins

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
AVCC[1]	203					3.3	3.3	3.3			
VCC[1]	23, 81, 135,180					3.3	3.3	3.3			
VCC5[1]	95, 128					5.0	5.0	5.0			
VSYS2[1]	142					3.3	3.3	5.0			
VSYS[1]	48, 65					5.0	5.0	5.0			
VMEM[1]	9, 22, 35					3.3	3.3	3.3			
VCC1[1]	176					3.3	3.3	3.3			
GND	1,12, 20, 33, 52, 53, 68, 104, 105, 121, 156, 157, 191										
AGND	208										

Notes:

1. *These reset state entries identify the VCCIO levels that are present on the ÉlanSC300 microcontroller for the three bus mode options. Note that the device is not limited to these VCC levels.*

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

PIN DESCRIPTIONS

Descriptions of the ÉlanSC300 microcontroller pins are organized into the following functional groupings:

- Memory bus interface
- System interface
- Keyboard interface
- Parallel port interface
- Serial port interface
- PCMCIA interface
- Power management interface
- Display interface
- Miscellaneous interface
- Local bus interface
- Maximum ISA bus interface
- JTAG boundary scan interface
- Reset and power

MEMORY BUS INTERFACE

$\overline{\text{CAS1H}}$ [$\overline{\text{SRCS3}}$], $\overline{\text{CAS1L}}$ [$\overline{\text{SRCS2}}$], $\overline{\text{CAS0H}}$ [$\overline{\text{SRCS1}}$], $\overline{\text{CAS0L}}$ [$\overline{\text{SRCS0}}$]

Column Address Strobe (Outputs; Active Low)

Column Address Strobe indicates to DRAM that a valid column address is present on the MA10–MA0 lines. Two $\overline{\text{CAS}}$ signals are allocated to each 16-bit bank, one per byte.

When SRAM, instead of DRAM, is configured as main memory, $\overline{\text{SRCS3}}$, $\overline{\text{SRCS2}}$, $\overline{\text{SRCS1}}$, and $\overline{\text{SRCS0}}$ are the alternate pin functions corresponding to $\overline{\text{CAS1H}}$, $\overline{\text{CAS1L}}$, $\overline{\text{CAS0H}}$, and $\overline{\text{CAS0L}}$ respectively. Each pin selects a byte in one of two possible 16-bit-wide SRAM banks. The SRAM functionality is selected via firmware. In this mode, all four of these outputs are active Low. For more information about $\overline{\text{SRCS3}}$–$\overline{\text{SRCS0}}$, see page 49.

$\overline{\text{DOSCS}}$

DOS ROM Chip Select (Output; Active Low)

The DOS ROM Chip Select is an active Low output that provides the chip select function for the Flash/ROM array banks that are used to hold the operating system or application code. $\overline{\text{DOSCS}}$ is used to select the DOS ROMs and can be configured to respond to direct addressing or Memory Management System (MMS) addressing.

MA11–MA0/SA23–SA12

Memory Address (Outputs; Active High)

Memory address lines for multiplexed and nonmultiplexed memory devices; their effect depends on the system configuration and the type of bus cycle.

- When system memory is configured as DRAM, the MA10–MA0 signals are multiplexed outputs and convey the row address during $\overline{\text{RAS}}$ assertion and column address during $\overline{\text{CAS}}$ assertion.
- When system memory is configured as SRAM, MA11–MA0 output the system addresses, SA12–SA23, and are used in conjunction with SA1–SA11.
- For cycles that are not targeted to system memory or internal I/O, MA11–MA0 are used to provide nonmultiplexed ISA-type address signals SA23–SA12, as shown in Table 12. See also SA11–SA0 on page 36.

Table 12. Non-Multiplexed Address Signals Provided by MA11–MA0

MA	11	10	9	8	7	6	5	4	3	2	1	0
SA	12	13	23	22	21	20	19	18	17	16	15	14

$\overline{\text{MWE}}$

Write Enable (Output; Active Low)

Write Enable is the write command strobe for the DRAM and SRAM devices.

$\overline{\text{RAS1}}$–$\overline{\text{RAS0}}$

Row Address Strobe (Output; Active Low)

Row Address Strobe indicates to DRAM that a valid row address is present on the MA11–MA0 lines. One $\overline{\text{RAS}}$ signal is allocated for each 16-bit DRAM bank, one per word.

$\overline{\text{ROMCS}}$

BIOS ROM Chip Select (Output; Active Low)

BIOS ROM Chip Select is an active Low output that provides the chip select function for the Flash/ROM array. $\overline{\text{ROMCS}}$ is used to select the BIOS ROM, and can be configured to respond to direct addressing or MMS addressing. When configured for direct addressing, the BIOS ROM can reside at one or all of the following address ranges:

0F0000h–0FFFFFh
0E0000h–0EFFFFh
0D0000h–0DFFFFh
0C0000h–0CFFFFh
0A0000h–0AFFFFh

The BIOS ROM chip select is also active for accesses into the 64-Kbyte segment that contains the boot vector, at address FF0000h to FFFFFFh.

For more information about the ROMCS pin, see the *Using 16-Bit ROMCS Designs in Élan™SC300 and ÉlanSC310 Microcontrollers Application Note*, order #21825.

SYSTEM INTERFACE

AEN [TDI]

DMA Address Enable (Output; Active High)

AEN is used to indicate that the current address active on the SA23–SA0 address bus is a memory address and that the current cycle is a DMA cycle. All I/O devices should use this signal in decoding their I/O addresses and should not respond when this signal is asserted. When AEN is asserted, the DACKx signals are used to select the appropriate I/O device for the DMA transfer.

This is a dual-function pin. When the JTAGEN signal is asserted, it functions as the TDI, JTAG Test Data Input pin.

D15–D0

System Data Bus (Bidirectional; Active High)

The System Data Bus inputs data during memory and I/O read cycles, and outputs data during memory and I/O write cycles. During Local Bus and DRAM/SRAM cycles, this bus represents the CPU data bus.

DACK2 [TCK]

DMA Channel 2 Acknowledge (Output; Active Low)

This output indicates that the current transfer is a DMA transfer to the I/O device connected to this DMA channel. In PC-compatible system designs, this signal can be connected to the floppy disk controller DMA acknowledge input.

This is a dual-function pin. When the JTAGEN signal is asserted, it functions as the TCK (JTAG Test Clock) pin. See "JTAG Boundary Scan Interface" on page 44 for more information on the function of this pin during Test mode.

DBUFOE

Data Buffer Output Enable (Output; Active Low)

This output is used to control the output enable on the system data bus buffer. When Low, the outputs of the Data Bus Buffer are enabled.

DRQ2 [TDO]

DMA Channel 2 Request (Input; Active High with Internal Pulldown)

This input is used to request a DMA transfer. It can be connected to the floppy disk controller DMA request output in PC-compatible system designs.

This is a dual-function pin. When the JTAGEN signal is asserted, it will function as the TDO, JTAG Test Data Out pin. See "JTAG Boundary Scan Interface" on page 44 for more information on the function of this pin during Test mode.

ENDIRH

High Byte Data Buffer Direction Control (Output; Active High)

This output controls the transceiver on the high byte of the data bus, bits 15–8. When asserted, this signal is used to enable the data from the ÉlanSC300 microcontroller data bus to the buffered data bus.

ENDIRL

Low Byte Data Buffer Direction Control (Output; Active High)

This output controls the transceiver on the low byte of the data bus, bits 7–0. When asserted, this signal is used to enable the data from the ÉlanSC300 microcontroller data bus to the buffered data bus.

IOCHRDY

I/O Channel Ready (Input; Active High)

This signal is used by ISA slave devices to add wait states to the current transfer. When this signal is deasserted, wait states are added.

IOCS16 [LCDDL0]

(Input; Active Low)

This input is used to signal to the ISA control logic that the targeted I/O device is a 16-bit device.

(IOCS16 is available unless the internal LCD Controller Bus mode is selected and a dual-scan LCD panel interface is selected via firmware.)

IOCS16 is generated by a 16-bit ISA I/O expansion board when the board recognizes it is being addressed. IOCS16 provides the same function for 16-bit I/O expansion devices as the MCS16 signal provides for the 16-bit memory devices.

Note: *IOCS16 is internally OR'd with MCS16. Do not tie IOCS16 Low.*

For more information about the IOCS16 pin, see the *Using 16-Bit ROMCS Designs in Élan™SC300 and ÉlanSC310 Microcontrollers Application Note*, order #21825.

IOR

I/O Read Command (Output; Active Low)

The IOR signal indicates that the current cycle is a read of the currently selected I/O device. When this signal is asserted, the selected I/O device can drive data onto the data bus.

$\overline{\text{IOW}}$

I/O Write Command (Output; Active Low)

The $\overline{\text{IOW}}$ signal indicates that the current cycle is a write of the currently selected I/O device. When this signal is asserted, the selected I/O device can latch data from the data bus.

IRQ1, IRQ14 [LCDDL2]

Interrupt Request Channels 1 and 14 (Input; Rising Edge/Active High, with Internal Pullup)

This input is connected to the internal 8259A-compatible Interrupt Controller Channels 1 and 14. In PC-compatible systems, IRQ1 may be connected to the 8042 keyboard controller.

(IRQ14 is available unless the internal LCD Controller Bus mode is selected and a dual-scan panel interface is selected via firmware.)

$\overline{\text{MCS16}}$ [LCDDL1]

(Input; Active Low)

This input is used to signal to the ISA control logic that the targeted memory device is a 16-bit device.

($\overline{\text{MCS16}}$ is available unless the internal LCD Controller Bus mode is selected and a dual-scan LCD panel interface is selected via firmware.)

$\overline{\text{MCS16}}$ is generated by a 16-bit memory expansion card when the card recognizes it is being addressed. This signal tells the data bus steering logic that the addressed memory device is capable of communicating over both data paths. When accessing an 8-bit memory device, the $\overline{\text{MCS16}}$ line remains deasserted, indicating to the data bus steering logic that the currently addressed device is an 8-bit memory device capable of communicating only over the lower data path.

Note: *$\overline{\text{MCS16}}$ is internally ORed with $\overline{\text{IOCS16}}$. Do not tie $\overline{\text{MCS16}}$ Low.*

For more information about the $\overline{\text{MCS16}}$ pin, see the *Using 16-Bit $\overline{\text{ROMCS}}$ Designs in Élan™SC300 and ÉlanSC310 Microcontrollers Application Note*, order #21825.

$\overline{\text{MEMR}}$

Memory Read Command (Output; Active Low)

The $\overline{\text{MEMR}}$ signal indicates that the current cycle is a read of the currently selected memory device. When this signal is asserted, the selected memory device can drive data onto the data bus.

$\overline{\text{MEMW}}$

Memory Write Command (Output; Active Low)

The $\overline{\text{MEMW}}$ signal indicates that the current cycle is a write of the currently selected memory device. When this signal is asserted, the selected memory device can latch data from the data bus.

PIRQ0 (PIRQ0/IRQ3),
PIRQ1 (PIRQ1/IRQ6)

Programmable Interrupt Requests (Inputs; Rising Edge/Active High, with Internal Pullup)

These two inputs can be programmed to drive any of the available interrupt controller interrupt request inputs. For more information, see the PIRQ Configuration Register, Index B2h, in the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

RSTDRV

System Reset (Output; Active High)

This signal is the ISA-compatible reset signal. When this signal is asserted, all connected devices reinitialize to their reset state. The pulse width of RSTDRV is adjustable, based on PLL startup timing. For more information, see "Loop Filters" on page 97 and the power-up sequence timings beginning on page 99.

SA11–SA0

System Address Bus (Output; Active High)

The system address bus outputs the physical memory or I/O port, least-significant, latched addresses. They are used by all external I/O devices and all memory devices other than main system DRAM. During main system SRAM and local bus cycles, this bus represents the CPU address bus (A11–A1). SA0 is equivalent to A0 during local bus cycles. See MA11–MA0 on page 34 for SA23–SA12.

$\overline{\text{SBHE}}$ [LCDDL3]

(Output; Active Low)

Active when the high byte is to be transferred on the upper 8 bits of the data bus.

($\overline{\text{SBHE}}$ is available unless the internal LCD Controller Bus mode is selected and a dual-scan LCD panel interface is selected via firmware.)

SPKR

Speaker, Digital Audio Output (Output)

This signal controls an external speaker driver. It is generated from the internal 8254-compatible Timer Channel 2 output ANDed with I/O port 061h, bit 1 (speaker data enable).

TC [TMS]

Terminal Count (Output; Active High)

This signal is used to indicate that the transfer count for the currently active DMA channel has reached zero, and that the current DMA cycle is the last transfer.

This is a dual-function pin. When the JTAGEN signal is asserted, it will function as the TMS, JTAG Test Mode Select pin. See the "JTAG Boundary Scan Interface" on page 44 for more information on the function of this pin during Test mode.

KEYBOARD INTERFACE

$\overline{\text{8042CS}}$ [XTDAT]

Keyboard Controller Chip Select (Output; Active Low)

This signal is a decode of A9–A0 = 060h to 06Eh, all even addresses. In PC-compatible systems, it connects to the external keyboard controller chip select. XTDAT is the PC/XT keyboard data line.

A20GATE

Address Bit-20 Gate (Input; Active High)

When deasserted, this signal is used to force CPU address bit 20 Low, a function required for PC compatibility. In PC-compatible systems, this signal can be driven by an 8042 keyboard controller, port 2, bit 1.

For detailed information about the A20GATE signal, see the *Élan™SC300 and ÉlanSC310 Microcontrollers GATEA20 Function Clarification Application Note,* order #21811.

$\overline{\text{RC}}$

Reset CPU (Input; Active Low)

This signal resets the internal CPU. In PC-compatible systems, this signal can be driven by a keyboard controller, port 2, bit 0.

SYSCLK [XTCLK]

System Clock (Output)

This clock can be used to provide a clock to a keyboard controller. It is not synchronous to ISA bus cycles. XTCLK is the PC/XT keyboard clock. For information about internal clock states, see Table 23 on page 54. For information about the maximum ISA bus option, see page 65.

PARALLEL PORT INTERFACE

$\overline{\text{ACK}}$

Printer Acknowledge (Input; Active Low)

The printer asserts ACK to confirm that the transfer from the ÉlanSC300 microcontroller to the parallel port was successful.

$\overline{\text{AFDT}}$ [X14OUT]

Auto Line Feed Detect (Output; Active Low)

This pin signals the printer to autofeed continuous form paper. It can be programmed to become a 14.336-MHz output.

BUSY

Printer Busy (Input; Active High)

The printer asserts BUSY when it is performing an operation.

$\overline{\text{ERROR}}$

(Input; Active Low)

The printer asserts the $\overline{\text{ERROR}}$ signal to inform the parallel port of a deselect condition, PE, or other error condition.

$\overline{\text{INIT}}$ [$\overline{\text{PCMCWE}}$]

Initialize Printer (Output; Active Low)

This pin signals the printer to begin an initialization routine. It can be programmed to become the PCMCIA write enable signal ($\overline{\text{PCMCWE}}$).

PE

Paper End (Input; Active High)

The printer asserts this signal when it is out of paper.

$\overline{\text{PPDWE}}$ [$\overline{\text{PPDCS}}$]

Parallel Port Write Enable (Output; Active Low)

The $\overline{\text{PPDWE}}$ signal is used to control the 374 type latch in a unidirectional parallel port design. To support a bidirectional parallel port design, this pin can be reconfigured ($\overline{\text{PPDCS}}$) to act as an address decode for the parallel port data port. It can then be externally gated with $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ to provide the Parallel Port Data Read and Write Strobes, respectively. For more information, see "Parallel Port" on page 61.

$\overline{\text{PPOEN}}$

Parallel Port Output Buffer Enable (Output; Active Low)

This signal supports a bidirectional parallel port design. It is used to control the output enable of the Parallel Port Output Buffer.

SLCT

Printer Select Return (Input; Active High)

The printer asserts SLCT when it has been selected.

SLCTIN [PCMCOE]

Printer Selected (Output; Active Low)

Asserting SLCTIN selects the line printer. This pin can be programmed to become the PCMCIA output enable signal (PCMCOE). For more information, see "Parallel Port" on page 61.

STRB

Strobe (Output; Active Low)

Asserting STRB signals the line printer to latch data currently on the parallel port.

SERIAL PORT INTERFACE

CTS

Clear To Send (Input; Active Low)

This signal indicates that the external serial device is ready to accept data.

DCD

Data Carrier Detect (Input; Active Low)

This signal indicates to the internal serial port controller that the attached serial device has detected a data carrier.

DSR

Data Set Ready (Input; Active Low)

This signal is used to indicate that the external serial device is ready to establish a communication link with the internal serial port controller.

DTR/CFG1

Data Terminal Ready (Output; Active Low)

This signal indicates to the external serial device that the internal serial port controller is ready to communicate.

The state of this signal is used to determine the pin configuration at power-up. For more information, see "Alternate Pin Functions" on page 68.

RIN

Ring Indicate (Input; Active Low)

This signal is used as a modem control function. A change in state on this signal by the external serial device causes a modem status interrupt. This signal can be used to cause the ÉlanSC300 microcontroller to resume from a suspended state.

RTS/CFG0

Request To Send (Output; Active Low)

This signal indicates to the external serial device that the internal serial port controller is ready to send data.

The state of this signal is used to determine the pin configuration at power-up. For more information, see "Alternate Pin Functions" on page 68.

SIN

Serial Data In (Input; Active High)

This signal is used to receive the serial data from the external serial device into the internal serial port controller.

SOUT

Serial Data Out (Output; Active High)

This signal is used to transmit the serial data from the internal serial port controller to the external serial device.

PCMCIA INTERFACE

BVD1_A (STSCHG_A), BVD1_B (STSCHG_B)

Battery Voltage Detect (Inputs)

These signals are generated by the memory card as an indication of the condition of its battery for a memory card interface. For an I/O card interface, these inputs are the card's Status Change Interrupt (active Low).

BVD2_A (SPKR_A), BVD2_B (SPKR_B)

Battery Voltage Detect (Inputs)

These signals are generated by the memory card as an indication of the condition of its battery for a memory card interface. For an I/O card interface, these pins become the speaker inputs from the cards.

CA24

Card Address Bit 24 (Output)

This card address bit is controlled by accessing the ÉlanSC300 microcontroller configuration registers and should be connected to the card interface signal A24. This address signal is common to slot A and slot B interfaces.

CA25

Card Address Bit 25 (Output)

This card address bit is controlled by accessing the ÉlanSC300 microcontroller configuration registers, and should be connected to the card interface signal A25. This address signal is common to slot A and slot B interfaces.

CD_A, CD_B

Card Detect (Inputs; Active Low)

The card detect signals indicate that the card is properly inserted into a socket. These signals should be driven from an "ANDing" of the CD1 and CD2 pins of a single socket. Therefore, two external AND gates are required, one for each slot.

ICDIR

Card Data Direction (Output)

This signal controls the direction of the card data buffers or translators, working in conjunction with the MCEL_x and MCEH_x card enable signals to control the data buffers on the card interface. When this signal is High, the data flow is from the ÉlanSC300 microcontroller to the card socket, indicating a data write cycle. When this signal is Low, the data flow is from the card socket into the ÉlanSC300 microcontroller, indicating a read cycle. Note that PCMCIA bus buffering may or may not be implemented in a system design.

MCEH_A, MCEH_B

Card Enables, High Byte (Output; Active Low)

These signals enable odd address bytes for their respective card interfaces.

MCEL_A, MCEL_B

Card Enables, Low Byte (Output; Active Low)

These signals enable even address bytes for their respective card interfaces.

PCMCOE

Card Memory Output Enable (Output, Active Low)

The Parallel Port SLCTIN signal can be programmed to become PCMCOE. PCMCOE indicates that a memory read cycle from the card interface is being performed.

PCMCWE

Card Memory Write Enable (Output, Active Low)

The Parallel Port INIT signal can be programmed to become PCMCWE. PCMCWE indicates that a memory write cycle to the card interface is being performed.

RDY_A (IREQ_A), RDY_B (IREQ_B)

Card Ready (Inputs; Active High)

This signal indicates that the respective card is ready to accept a new data transfer command if a memory interface is selected. If the card interface is configured as an I/O interface, the Socket A I/O card's IREQ_A signal uses RDY_A as a general purpose input pin that may be used as the card interrupt request input into the ÉlanSC300 microcontroller (active High). For more information about socket A card's IREQ_A signal, see Chapter 5 in the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

REG_A, REG_B

Attribute Memory Select (Output; Active Low)

This signal selects either the Attribute Memory or the Common Memory. This signal will be inactive (High) for accesses to Common Memory, and asserted (Low) for accesses to Attribute Memory. This signal is also asserted (Low) for all I/O accesses.

RST_A, RST_B

Card Reset (Outputs; Active High)

These signals reset their respective cards. When active, this signal clears the Card Configuration Option register, thus placing a card in a memory-only mode.

VPP_A, VPP_B

Program and Peripheral Voltage Control (Output; Active High)

These signals can be used to enable the programming voltages to their respective card interfaces.

WAIT_AB

Extend Bus Cycle (Input; Active Low)

This signal delays the completion of the memory access or I/O access that is currently in progress. When this signal is asserted (Low), wait states will be inserted into the cycle in progress. A two-card solution needs each slot's WAIT_AB signal "ANDed" before being input to the ÉlanSC300 microcontroller.

WP_A (IOIS16A), WP_B (IOIS16B)

Write Protect (Inputs; Active High)

When a memory interface is selected, this signal indicates the status of the targeted device's Write Protect Switch. When the targeted device is configured for an I/O interface, the WP_A signal is used to indicate that the currently accessed port is a 16-bit port (IOIS16x active Low).

Both WP_A and WP_B signals indicate that the targeted device is a 16-bit device during I/O access to the targeted device. When the targeted device is configured as an I/O access, the two signals are OR'd together to generate the IOIS16x signal. When the targeted device is configured as an I/O access, there is basically no difference between the WP_A and WP_B signals.

POWER MANAGEMENT INTERFACE

ACIN

AC Input Status (Input; Active High)

When asserted, this signal disables all power management functions (if so enabled). It can be used to indicate when the system is being supplied power from an AC source.

$\overline{BL4}$–$\overline{BL1}$

Battery Low Detects
(Inputs; Negative Edge Sensitive)

These signals are used to indicate to the ÉlanSC300 microcontroller the current status of the battery. $\overline{BL4}$–$\overline{BL1}$ can indicate various conditions of the battery as status changes. A High indicates normal operating conditions, while a Low indicates a low voltage warning condition. These inputs can be used to force the system into one of the power saving modes when activated, as follows:

- $\overline{BL1}$ can be programmed to force the system to go to Low Speed PLL mode or to generate an SMI.
- $\overline{BL2}$ can be programmed to force the system to enter Sleep mode if not already in Sleep mode, or to generate an SMI.
- $\overline{BL3}$ can only be programmed to generate an SMI.
- $\overline{BL4}$ can be programmed to force the system to enter Suspend mode.

EXTSMI

External System Management Interrupt
(Input; Edge Sensitive)

This input is provided to allow external logic to generate an SMI request to the CPU. It is edge triggered, with the polarity programmable.

$\overline{LPH}$

Latched Power Control (Output; Active Low)

This signal is the inverse of $\overline{BL4}$ if ACIN is not true and $\overline{BL4}$ is enabled.

PGP3–PGP0

Programmable Chip Select Generation
(Input/Output)

PGP0 and PGP1 can be programmed as input or output. The default is input. PGP2 and PGP3 are output only.

These general purpose pins can be individually programmed as decoder outputs or chip selects for other external peripheral devices.

PGP0 and PGP2 can be gated with I/O write or act as an address decode only. PGP1 and PGP3 can be gated with I/O Read or act as an address decode only. PGP0 and PGP1 can be directly controlled via a single register bit if configured to do so. PGP2 and PGP3 can also be configured for a specific state when the PMU is in the off state.

PGP2 and PGP3 can be programmed to be set to a pre-defined state for Micro Power Off mode.

For more information about PGP3–PGP0, see the *ÉlanTMSC300 Microcontroller Programmer's Reference Manual*, order #18470B and *Using 10-Bit ROMCS Designs in ÉlanTMSC300 and ÉlanSC310 Microcontrollers Application Note*, order #21825.

PMC4–PMC0

Power Management Controls
(Output; Programmable)

Power Management Control outputs control the power to various external devices and system components. The PMC0, PMC1, PMC2, and PMC4 signals are asserted Low immediately after reset, and the PMC3 signal is asserted High immediately after reset. Each of the PMC pins can then be programmed to be High or Low for each of the ÉlanSC300 microcontroller power management modes.

$\overline{SUS}$/$\overline{RES}$

Suspend/Resume Operation (Input; Rising Edge)

When the ÉlanSC300 microcontroller is in High Speed PLL, Low Speed PLL, or Doze mode, a positive edge on this pin causes the internal logic to step down through the Power Management modes (one per refresh cycle) until Sleep mode is entered. If in Sleep, Suspend, or Off mode, a positive edge on this pin causes the ÉlanSC300 microcontroller to enter the High Speed PLL mode.

DISPLAY INTERFACE

The signals listed as part of the display interface are only available when the ÉlanSC300 microcontroller is configured with the internal LCD controller enabled. If the internal LCD controller is disabled, the functions of these pins change to support either a CPU local bus interface or maximum ISA bus interface. The pins required for physical connection to the microcontroller are listed at the end of this section on page 42. For more information about the LCD controller, see the *Configuring the ÉlanTMSC300 Device's Internal CGA Controller for a Specific LCD Panel Application Note*, order #20749.

CP1

LCD Panel Line Clock (Output)

This is the Line Clock when in internal LCD mode and an LCD configuration is selected. It is activated at the start of every pixel line refresh cycle. CP1 should be connected to the equivalent line on the LCD panel.

CP2

LCD Panel Shift Clock (Output)

This is the nibble/byte strobe when in internal LCD mode and an LCD configuration is selected. CP2 is also known as the shift clock or data shift. It is used by the LCD to latch data. CP2 should be connected to the equivalent line on the LCD panel.

$\overline{\text{DSCE}}$

Display SRAM Chip Enable (Output; Active Low)

This signal generates the external video SRAM Chip Enable.

DSMA14–DSMA0

Display SRAM Address Bus (Output)

These signals generate the address to the SRAM. Up to 32 Kbyte can be supported for the display interface.

DSMD7–DSMD0

Display SRAM Data Bus (Bidirectional)

These signals provide the data bus used for the video SRAM.

$\overline{\text{DSOE}}$

Display SRAM Output Enable (Output; Active Low)

This signal controls the video SRAM Output Enable pin.

$\overline{\text{DSWE}}$

Display SRAM Write Enable (Output; Active Low)

When asserted, this signal indicates a Write to the video SRAM.

FRM

LCD Panel Line Frame Start (Output)

This signal is asserted at the start of every frame (panel scan) when in LCD mode and an LCD configuration is selected. FRM is also known as FLM or frame. It should be connected to the equivalent line on the LCD panel.

LCDD0

LCD Data Bit (Output)

When in internal LCD mode and an LCD configuration is selected, this signal is data bit 0. LCDD0 is the LSB and should be connected to the corresponding LSB pin on the LCD panel.

LCDD1

LCD Data Bit (Output)

When in internal LCD mode and an LCD configuration is selected, this signal is data bit 1. LCDD1 should be connected to the corresponding pin on the LCD panel.

LCDD2

LCD Data Bit (Output)

When in internal LCD mode and an LCD configuration is selected, this signal is data bit 2. LCDD2 should be connected to the corresponding pin on the LCD panel.

LCDD3

LCD Data Bit (Output)

When in internal LCD mode and an LCD configuration is selected, this signal is data bit 3. LCDD3 is the MSB and should be connected to the corresponding MSB pin on the LCD panel.

[LCDDL3–LCDDL0]

LCD Panel Data Bits for Dual-Scan Panels (Outputs)

When the ÉlanSC300 microcontroller is programmed to support LCD Dual-Scan Panel mode (separate data bits for the top and bottom half of the panel), these bits (LCDDL3–LCDDL0) are for the bottom half of the screen. LCDD3–LCDD0 are the data bits for the top half of the screen. LCD Dual-Scan Panel mode is selected via firmware. LCDDL0 is the LSB for the lower panel and LCDDL3 is the MSB for the lower panel.

These pins are shared with $\overline{\text{IOCS16}}$, $\overline{\text{MCS16}}$, IRQ14, and $\overline{\text{SBHE}}$ (described in “System Interface”, beginning on page 35.) LCDDL3–LCDDL0 should be connected to their corresponding pins on the dual-screen LCD lower panel.

$\overline{\text{LVDD}}$

LCD Panel VDD Voltage Control (Output; Active Low)

This signal is used to control the assertion of the LCD’s VDD driver. $\overline{\text{LVDD}}$ is provided to be part of the solution in sequencing the panel’s VDD, DATA, and VEE signals in the proper order.

$\overline{\text{LVEE}}$

LCD Panel VEE Voltage Control (Output; Active Low)

This signal is used to control the assertion of the LCD’s VEE driver. $\overline{\text{LVEE}}$ is provided to be part of the solution in sequencing the panel’s VDD, DATA, and VEE signals in the proper order.

M

LCD Panel AC Modulation (Output)

In internal LCD mode, this is the AC modulation signal for the LCD. AC modulation causes the LCD to change polarity on its crystal material to keep the LCD from forming a DC bias. Some LCD panels do not require this signal. Connect M to the equivalent line on the LCD panel if appropriate.

LCD Physical Pin Connections

To connect an LCD panel to the ÉlanSC300 microcontroller, the following pins need to be connected:

- CP1
- CP2
- FRM
- LCDD3–LCDD0
- LCDDL3–LCDDL0 (dual-scan panel only)
- M

The other connections that are required vary. For example:

- Contrast voltage can be positive or negative, typically about -22 V.
- +5 V
- GND
- Display enable usually requires a simple 5-V enable signal that some panels require. This can easily be connected to one of the ÉlanSC300 microcontroller's PMC pins.
- V_{EE} is typically a voltage in the same range as the contrast voltage. Refer to the panel specifications for more information.

MISCELLANEOUS INTERFACE

LF1, LF2, LF3, LF4 (Analog inputs)

Loop Filters

These pins are used to connect external components that make up the loop filters for the internal PLLs. For more information, see "Loop Filters" on page 97.

X1OUT [BAUD_OUT]

14-MHz/UART Output

This can be programmed to be either the 14.336-MHz clock or the serial baud rate clock for serial infrared devices. The 14.336-MHz output can be used by external video controllers. As BAUD_OUT, it is 16 x the bit data rate of the serial port and is used by serial infrared devices.

[X14OUT]

14-MHz Output

The Parallel Port $\overline{\text{AFDT}}$ output can be programmed to become X14OUT, a 14.336-MHz clock.

X32IN, X32OUT

32.768-kHz Crystal Interface

These pins are used for the 32.768-kHz crystal. This is the main clock source for the ÉlanSC300 microcontroller and is used to drive the internal Phase-Locked Loops that generate all other clock frequencies needed in the system. For more information, see "Crystal Specifications" on page 95.

LOCAL BUS INTERFACE

The local bus interface pins are only available when the ÉlanSC300 microcontroller's internal LCD controller is disabled and the ÉlanSC300 microcontroller pin configuration is set to support a CPU local bus and a partial ISA bus.

The following list of pins is specific to local bus functionality. In Local Bus mode, additional ISA pins are also available. These pins are described in the next section "Maximum ISA Bus Interface" because these pins are available in both Local Bus and Maximum ISA Bus modes. For more information, see "CPU Local Bus Interface versus Internal LCD Interface" on page 69 and Tables 37– on page 73.

A23–A12

Local Bus Upper Address Lines (Output)

These signals are the local bus CPU address lines when in Local Bus mode. These signals are combined with the SA11–SA0 signals to form the complete CPU address bus during local bus cycles.

$\overline{\text{ADS}}$

Local Bus Address Strobe (Output; Active Low)

Local Bus Address Strobe is an active Low address strobe signal for 386 local bus devices.

$\overline{\text{BHE}}$

Local Bus Byte High Enable (Output; Active Low)

This signal indicates to the local bus devices that data is being transferred on the high byte of the data bus.

$\overline{\text{BLE}}$

Local Bus Byte Low Enable (Output; Active Low)

This signal indicates to the local bus devices that data is being transferred on the low byte of the data bus.

CPUCLK

CPU 2X Clock (Output)

This is the timing reference for the local bus device. The high-speed PLL can be programmed to provide one of the clock frequencies shown on page 53.

$\overline{\text{CPURDY}}$

386 CPU Ready Signal (Output; Active Low)

This signal shows the current state of the 386 core CPU's $\overline{\text{CPURDY}}$ signal.

CPURST

CPU Reset (Output; Active High)

This signal is used to force the local bus device to an initial condition. It is also used to allow the local bus device to synchronize to the CPUCLK. This signal is taken directly from the internal CPU reset.

D/$\overline{\text{C}}$

Local Bus Data/Control (Output; Active Low)

This signal indicates to the local bus devices that the current cycle is either a Data cycle or a Control cycle. A Low on this signal indicates that the current cycle is a Control cycle.

$\overline{\text{LDEV}}$

Local Bus Device Select (Input; Active Low)

This signal is used by the local bus devices to signal that they will respond to the current cycle. If $\overline{\text{LDEV}}$ is not driven active by the time specified in Table 57 on page 108, then the cycle defaults to an ISA bus cycle.

$\overline{\text{LRDY}}$

Local Bus Device Ready (Input; Active Low)

This signal is used by the local bus devices to terminate the current bus cycle.

M/$\overline{\text{IO}}$

Local Bus Memory/I/O (Output; Active Low)

This signal indicates to the local bus devices that the current cycle is either a memory or an I/O cycle. A Low on this signal indicates that the current cycle is an I/O cycle.

W/$\overline{\text{R}}$

Local Bus Write/Read (Output; Active Low)

This signal indicates to the local bus devices that the current cycle is either a Read or a Write cycle. A Low on this signal indicates that the current cycle is a Read cycle.

MAXIMUM ISA BUS INTERFACE

The pins listed below as part of the "ISA Bus Interface" are only available when the ÉlanSC300 microcontroller pin configuration is configured to enable the maximum ISA Bus. When the maximum ISA bus interface is enabled, the internal LCD controller and the CPU local bus interface are disabled. (This mode does not support master and ISA refresh cycles.)

For more information, see "Maximum ISA Interface versus Internal LCD Interface" on page 70, Table 37–Table on page 73, and the *Élan™SC300 and Élan™SC310 Devices' ISA Bus Anomalies Application Note*, order #20747.

$\overline{\text{0WS}}$

Zero Wait State (Input; Active Low)

This input can be driven active by an ISA memory device to indicate that it can accept a Zero Wait State memory cycle.

BALE

Bus Address Latch Enable (Output; Active High)

This PC/AT-compatible signal is used by external devices to latch the LA signals for the current cycle.

$\overline{\text{DACK7}}$, $\overline{\text{DACK6}}$, $\overline{\text{DACK5}}$, $\overline{\text{DACK3}}$, $\overline{\text{DACK2}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$

DMA Acknowledge (Output; Active Low)

DMA acknowledge signals are active Low output pins that acknowledge their corresponding DMA requests.

Note: *The $\overline{\text{DACK2}}$ signal is available regardless of the ÉlanSC300 microcontroller's bus mode. $\overline{\text{DACK1}}$ and $\overline{\text{DACK5}}$ are also available in the local bus pin configuration.*

DRQ7, DRQ6, DRQ5, DRQ3, DRQ2, DRQ1, DRQ0

DMA Request (Input; Active High)

DMA Request signals are asynchronous DMA channel request inputs used by peripheral devices to gain access to a DMA service.

Note: *The DRQ2 signal is available regardless of the ÉlanSC300 microcontroller's bus mode. DRQ1 and DRQ5 are also available in the local bus pin configuration.*

$\overline{\text{IOCHCHK}}$

I/O Channel Check (Input; Active Low)

This is a PC/AT-compatible signal used to generate an NMI or SMI.

Note: *$\overline{\text{IOCHCHK}}$ is also available in the Local Bus pin configuration.*

IRQ15, IRQ14, IRQ12–IRQ9, IRQ7–IRQ3, IRQ1

Interrupt Request
(Inputs; Rising Edge/Active High Trigger)

Interrupt Request input pins signal the internal 8259 compatible interrupt controller that an I/O device needs servicing.

IRQ3 and IRQ6 are shared with PIRQ0 and PIRQ1.

IRQ0 is internally connected to the counter/timer, and IRQ8 is internally connected to the real-time clock. IRQ2 is used for cascading, and IRQ13 is reserved. IRQ0, IRQ2, IRQ8, and IRQ13 are not available externally.

Note: *IRQ4, IRQ12, and IRQ15 are also available in the Local Bus pin configuration.*

LA23–LA17

Latchable ISA Address Bus (Outputs)

These are the ISA latchable address signals. These signals are valid early in the bus cycle so that external peripherals may have time to decode the address and return certain control feedback signals such as $\overline{\text{MCS16}}$.

$\overline{\text{LMEG}}$

Address is in Low Meg (Output; Active Low)

This signal is active (Low) whenever the address for the current cycle is in the first Mbyte of memory address space (SA23 = SA22 = SA21 = SA20 = 0).

Note: *$\overline{\text{LMEG}}$ should not be used to generate $\overline{\text{SMEMR}}$ or $\overline{\text{SMEMW}}$. Instead, address lines SA23–SA20 should be decoded. For more information about $\overline{\text{LMEG}}$, see the* ÉlanTMSC300 and ÉlanTMSC310 Devices' ISA Bus Anomalies Application Note*, order #20747.*

JTAG BOUNDARY SCAN INTERFACE

The ÉlanSC300 microcontroller provides an IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port (TAP) and Boundary-Scan Architecture.

The boundary-scan test logic consists of a boundary scan register and support logic that are accessed through the TAP. The TAP provides a simple serial interface that makes it possible to test the microcontroller and system hardware in a production environment.

The TAP contains extensions that allow a hardware-development system to control and observe the microcontroller without interposing hardware between the microcontroller and the system.

The TAP can be controlled via a bus master. The bus master can be either automatic test equipment or a component (PLD) that interfaces to the four-pin test bus.

The JTAG pins described here are shared pin functions. They are enabled by the JTAGEN signal.

JTAGEN

JTAG Enable (Input; Active High)

This pin enables the JTAG pin functions. When it is High, the JTAG interface is enabled. When it is Low, the JTAG pin functions are disabled and the pins are configured to their default functions. See the Pin Designations, System Interface, and Miscellaneous Interface tables for the JTAG pin default function descriptions. For more information, see "System Test and Debug" on page 74.

[TCK]

Test Clock (Input)

Test clock is a JTAG input clock that is used to access the test access port when JTAGEN is active.

[TDI]

Test Data Input (Input)

Test data Input is the serial input stream for JTAG scan input data when JTAGEN is active.

[TDO]

Test Data Output (3-State Output)

Test data Output is the serial output stream for JTAG scan result data when JTAGEN is active.

[TMS]

Test Mode Select (Input)

Test Mode Select is an input for controlling the Test Access Port when JTAGEN is active.

RESET AND POWER

See the Voltage Partitioning section on page 95 for more information about power.

AGND

Analog Ground pin

This pin is the ground for the analog circuitry and is broken out separately from the other GND pins making it possible to filter AGND in a system that has a lot of noise on the ground plane. In most applications, AGND is tied directly to the ground plane with the other ground pins on the microcontroller.

AVCC

3.3 V (only) Supply Pin

This supply pin provides power to the analog section of the ÉlanSC300 microcontroller's internal PLLs. Extreme care should be taken that this supply voltage is isolated properly to provide a clean, noise-free voltage to the PLLs

AVCC is required for battery backup. For more information about battery backup, see the *ÉlanTMSC300 and ÉlanTMSC310 Microcontrollers Solution For Systems Using a Back-Up Battery Application Note*, order #20746.

GND

System Ground Pins

These pins provide electric grounding to all non-analog sections of the ÉlanSC300 microcontroller's internal CPU and peripherals.

$\overline{\text{IORESET}}$

Reset Input (Input; Active Low)

$\overline{\text{IORESET}}$ is an asynchronous hardware reset input equivalent to POWERGOOD in the PC/AT system architecture. Asserting this signal does not reset the RTC RAM invalid bit.

Asserting $\overline{\text{IORESET}}$ without asserting $\overline{\text{RESIN}}$ causes the ÉlanSC300 microcontroller to go into Micro Power Off mode. For more information, see "Micro Power Off Mode" on page 55.

$\overline{\text{RESIN}}$

Master Reset (Input; Active Low)

$\overline{\text{RESIN}}$ indicates that main power is being applied to the ÉlanSC300 microcontroller for the first time. When this signal is asserted, the RTC and internal registers are reset.

The $\overline{\text{RESIN}}$ signal supersedes the $\overline{\text{IORESET}}$ signal.

VCC

3.3 V (only) DC Supply Pins

These supply pins provide power to the ÉlanSC300 microcontroller core. Refer to AC Characteristics for VCC power up timing restrictions.

The VCC pins are required for battery backup. For more information about battery backup, see the *ÉlanTMSC300 and ÉlanTMSC310 Microcontrollers Solution For Systems Using a Back-Up Battery Application Note*, order #20746.

VCC1

3.3 V or 5 V Supply Pin

This supply pin provides power to a subset of the LCD/ alternate, power management, and ISA interface pins.

VCC5

5 V DC Supply Pins

These supply pins provide power to the 5 V only interface pins. These pins could be 3.3 V in a pure 3.3-V system.

VMEM

3.3-V or 5-V Supply Pins

These supply pins provide power to the Memory Interface and Data Bus pins (D15–D0). These pins must be connected to the same DC supply as the system DRAMs.

VSYS

3.3 V or 5 V Supply Pins

These supply pins provide power to a subset of the ISA address and command signal pins, in addition to external memory chip selects, buffer direction controls, and other miscellaneous functions.

VSYS2

3.3 V or 5 V Supply Pins

These supply pins provide power to some of the ÉlanSC300 microcontroller alternate system interface pins.

FUNCTIONAL DESCRIPTION

The ÉlanSC300 microcontroller architecture consists of several components, as shown in the device block diagram. These components can be grouped into eight main functional modules:

1. The Am386SXLV microprocessor core itself, including System Management Mode (SMM) power management hardware
2. A memory controller and associated mapping hardware
3. Two PCMCIA Revision 2.1 slots
4. An additional power management controller that interfaces to the CPU's System Management Mode (SMM) and is integrated tightly with internal clock generator hardware
5. Core peripheral controllers (DMA, interrupt controller, and timer)
6. Additional peripheral controllers (UART, parallel port, and real-time clock)
7. PC/AT support features
8. An integrated LCD controller, optional local bus controller, or optional maximum ISA bus

The remainder of this section describes these modules.

Am386SXLV CPU Core

The CPU core component is a full implementation of the AMD Am386SXLV 32-bit, low-voltage microprocessor (with I/O pads removed). For more information about the Am386 microprocessors, see the

Am386® SX/SXL/SXLV Data Sheet, order #21020 and the *Am386® DX/DXL Data Sheet*, order #21017.

Along with standard 386 architectural features, the CPU core includes SMM. SMM and the other features of the CPU are described in the *Am386DXLV and Am386SXLV Microprocessors Technical Reference Manual,* order #16944.

Memory Controller

The ÉlanSC300 microcontroller memory controller is a unified control unit that supports a high-performance, 16-bit data path to DRAM or SRAM. No external memory bus buffers are required and up to 16 Mbyte in two 16-bit banks can be supported. System memory must always be configured as 16-bits wide. For more information about the memory controller, see Chapter 2 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470. The System Block Diagram, Figure 7 on page 64 of this manual, shows a typical palm-top memory configuration.

The ÉlanSC300 microcontroller's memory controller supports an EMS-compatible Memory Mapping System (MMS) with 12 page registers. This facility can be used to provide access to ROM-based software. MMS is also used in the PCMCIA slot support. Shadow RAM is also supported.

The Memory Controller supports one of three different memory operating modes: SRAM, Page mode DRAM, or Enhanced Page mode DRAM. Enhanced Page mode increases DRAM access performance by effectively doubling the DRAM page size in a two-bank DRAM system by arranging the address lines such that one page is spread across both DRAM banks. Both DRAM modes use standard Fast Page mode DRAMs.

The memory controller operation is synchronous with respect to the CPU. This ensures maximum performance for all transfers to local memory. The clock stretching implemented by the clock generation circuitry works to reduce synchronous logic power consumption.

As shown in Table 13, the two DRAM operating modes are defined by the MOD field in the Memory Configuration Register, Index 66h, bit 0.

Table 13. DRAM Mode Selection

MOD0 (Index 66h, bit 0)	Function
0	Page mode
1	Enhanced Page mode

The ÉlanSC300 microcontroller defaults to a DRAM interface. The SRAM mode is selected via bit 0 of the Miscellaneous 6 Register Index 70h. The memory controller provides for a direct connection of two 16-bit banks supporting up to 16 Mbyte of DRAM, utilizing industry standard modules. The ÉlanSC300 microcontroller shares the DRAM address lines MA0–MA11 with the upper system address lines SA12–SA23 to reduce pin count. This signal sharing is shown in Table 14.

Table 14. MA and SA Signal Pin Sharing

System Address	DRAM Memory Address
SA23–SA14	MA9–MA0
SA13	MA10
SA12	MA11

The ÉlanSC300 microcontroller also shares the DRAM data bus with the system data bus on the D15–D0 pins. In a typical system, an SD bus is created with an external x 16 bit buffer or level translator to isolate the DRAM data bus from the rest of the system. Refer to the Typical System Block Diagram, Figure 7 on page 64 of this data sheet. The DRAM configurations are supported as shown in Table 11. The bank size information in the table also applies when system memory is configured as SRAM; however, SRAM uses a different addressing scheme than DRAM and shares the same address lines as the ISA bus. Chapter 2 in the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470, contains more information. Note that the configurations that use 512 Kbyte x 8 bit and 1 Mbyte x 16 bit DRAMs employ asymmetrical addressing. Table 16 and Table 17 show the relationship of the CPU address mapped to the DRAM memory.

Table 15. Supported DRAM/SRAM Configuration

	Bank Size (16-Bit Wide Only)		Index B1h		Index B4h	Index Reg. 66h		
Total DRAM/SRAM Size	Bank 0 DRAMs	Bank 1 DRAMs	Bit 7	Bit 6	Bit 7	MS2 Bit 4	MS1 Bit 3	MS0 Bit 2
512 Kbyte	4 256 K x 4 bits	—	0	0	1	x	x	x
512 Kbyte	1 256K x 16 bits	—	0	0	1	x	x	x
1 Mbyte	4 256 K x 4 bits	4 256 K x 4 bits	0	1	1	x	x	x
1 Mbyte	1 256K x 16 bits	1 256K x 4 bits	0	1	1	x	x	x
1 Mbyte[1]	2 512 K x 8 bits	—	x	x	0	0	0	1
2 Mbyte[1]	2 512 K x 8 bits	2 512 K x 8 bits	x	x	0	0	1	0
2 Mbyte[1]	4 1 Mbyte x 4 bits	—	x	x	0	0	1	1
2 Mbyte	1 1 Mbyte x 16 bits	—	1	0	1	x	x	x
4 Mbyte[1]	4 1 Mbyte x 4 bits,	4 1 Mbyte x 4 bits	x	x	0	1	0	0
4 Mbyte	1 1 Mbyte x 16 bits	1 1 Mbyte x 16 bits	1	1	1	x	x	x
8 Mbyte[1]	4 4 Mbyte x 4 bits	—	x	x	0	1	0	1
16 Mbyte[1]	4 4 Mbyte x 4 bits	4 4 Mbyte x 4 bits	x	x	0	1	1	0

Notes:

1. *SRAM configuration is supported. Bit 7 of the PCMCIA Card Reset Register, Index B4h, must be cleared. Setting MS2–MS0 of Index 66h as specified in the table selects the SRAM bank sizes.*

See Tables 16 and 17 for the DRAM address multiplexing schemes for normal page mode and Enhanced Page mode, respectively.

Table 16. DRAM Address Translation (Page Mode)

Index B4h	Index 66h	Index B1h	DRAM			DRAM Address												
Bit 7	Bits 4 3 2	Bits 7 6	Size (Byte)	Bank 0 (Byte)	Bank 1 (Byte)	RAS CAS	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
0	0 0 1[1]	x x	1M	1M	–	RAS CAS	– –	– –	A19 –	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A10 A1
0	0 1 0[1]	x x	2M	1M	1M	RAS CAS	– –	– –	A19 –	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A10 A1
0	0 1 1	x x	2M	2M	–	RAS CAS	– –	– –	A19 A10	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A20 A1
0	1 0 0	x x	4M	2M	2M	RAS CAS	– –	– –	A19 A10	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A20 A1
0	1 0 1	x x	8M	8M	–	RAS CAS	– –	A22 A11	A19 A10	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A21 A2	A20 A1
0	1 1 0	x x	16M	8M	8M	RAS CAS	– –	A22 A11	A19 A10	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A21 A2	A20 A1
1	x x x	0 0	512K	512K	–	RAS CAS	– –	– –	– –	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A10 A1
1	x x x	0 1	1M	512K	512K	RAS CAS	– –	– –	– –	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A10 A1
1	x x x[1]	1 0	2M	2M	–	RAS CAS	A20 –	A9 –	A19 –	A18 –	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A10 A1

Notes:

1. *Asymmetrical addressing applies to configurations using DRAM with 512K x 8 and 1M x 16 organizations.*

Page mode DRAM using two banks of 1 Mbyte x 16 DRAMs is not supported. Use Enhanced Page mode for two-bank configuration. See Table 17 for the supported Enhanced Page mode configurations. See Table 15 for the physical organization of the DRAM devices supported.

Bit 0 of the Memory Configuration 1 Register, Index 66h, must be cleared for normal (non-enhanced) page mode.

Table 17. DRAM Address Translation (Enhanced Page Mode)

Index B4h	Index 66h	Index B1h	DRAM			DRAM Address												
Bit 7	Bits 4 3 2	Bits 7 6	Size (Byte)	Bank 0 (Byte)	Bank 1 (Byte)	RAS CAS	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
0	0 1 0[1]	x x	2M	1M	1M	RAS CAS	– –	– –	A19 –	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A20 A1
0	1 0 0	x x	4M	2M	2M	RAS CAS	– –	– –	A19 A10	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A21 A2	A20 A1
0	1 1 0	x x	16M	8M	8M	RAS CAS	– –	A22 A11	A19 A10	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A23 A3	A21 A2	A20 A1
1	x x x	0 1	1M	512K	512K	RAS CAS	– –	– –	– –	A18 A9	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A19 A1
1	x x x[2]	1 1	4M	2M	2M	RAS CAS	A20 –	A21 –	A19 –	A18 –	A17 A8	A16 A7	A15 A6	A14 A5	A13 A4	A12 A3	A11 A2	A10 A1

Notes:

1. *Bit 4 of the Version Register, Index 64h must also be set for 2-Mbyte Enhanced Page mode. Also, bit 0 of Memory Configuration 1 Register, Index 66h, must be a 1.*
2. *When 16-Mbit asymmetric DRAMs are used in a two-bank configuration (4 Mbyte), bits 1 and 0 of the Memory Configuration 1 Register, Index 66h, must be set for Enhanced Page mode only.*

See Table 11 for a description of the physical organization of the DRAM devices supported.

Bit 0 of the Memory Configuration 1 Register, Index 66h must be set to enable Enhanced Page mode. Bit 1 of the Memory Configuration 1 Register, Index 66h, must be set for DRAM. If set for SRAM, bits 0 and 1 control wait states.

SRAM

When using SRAM instead of DRAM for main memory, up to 16 Mbyte can be accessed, the SRAM being organized as one or two banks. Each bank is 16 bits wide and is provided with a low and high byte select.

An SRAM memory interface is selected by setting bit 0 of the Miscellaneous 6 Register, Index 70h. If this is done, $\overline{\text{CAS1H}}$, $\overline{\text{CAS1L}}$, $\overline{\text{CAS0H}}$, and $\overline{\text{CAS0L}}$ will have their alternate function as SRAM chip select pins 3–0 ($\overline{\text{SRCS3}}$–$\overline{\text{SRCS0}}$). Table 18 shows the key SRAM access pins.

Table 18. SRAM Access Pins

Pin Name	I/O	Function
$\overline{\text{SRCS0}}$	O	SRAM Bank 0 Low Byte Select
$\overline{\text{SRCS1}}$	O	SRAM Bank 0 High Byte Select
$\overline{\text{SRCS2}}$	O	SRAM Bank 1 Low Byte Select
$\overline{\text{SRCS3}}$	O	SRAM Bank 1 High Byte Select
SA23–SA1	O	Address (16 Mbyte maximum)
$\overline{\text{MWE}}$	O	Write enable

See Table 15 on page 47 for bank size settings.

The MS2–MS0 bits in the Memory Configuration Register, Index 66, are also used to program the total SRAM size. Bit 7 of the PCMCIA Card Reset Register, Index B4h, must be cleared for SRAM configurations. Table 19 contains information about SRAM wait state logic, and Table 30 on page 71 contains SRAM interface alternate pin information.

Table 19. SRAM Wait State Select Logic

Configuration		Number of Wait States		SRAM Speed		
Index 63h Bit 4	Index 66h Bits 1 and 0	Read	Write	20 MHz	25 MHz	33 MHz
x	0 0	0	1	45 ns	35 ns	25 ns
0	0 1	1	1	80 ns	55 ns	35 ns
1	0 1	2	2	120 ns	100 ns	70 ns

Notes:

Refer to Index 70h, bit 0, in the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470 for information on how to select SRAM versus DRAM.*

PCMCIA Slots

The ÉlanSC300 microcontroller supports two revision 2.1 PCMCIA slots.

MMS mapping logic is used to access the PCMCIA memory address space. Up to twelve 16-Kbyte pages of the CPU's address space are mapped into windows of PCMCIA memory address space.

Depending on the system requirements, the address and data lines to the PCMCIA slots may or may not require external buffers (see Figure 7 on page 64). For more information, see Chapter 2 in the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470. Also see the *Élan™SC300 and ÉlanSC310 Microcontrollers Memory Management Application Note*, order #21823 and the *Using a PCMCIA Card as a Boot ROM on an Élan™SC300 Microcontroller Design Application Note*, order #21824.

The PMU Modes and Clock Generators

The Power Management Unit (PMU) monitors all system activities (e.g., keyboard, screen, and disk events), and, based on the state of the system, determines in which operating mode the system should be running. The PMU supports six operating modes, each defined by a different combination of CPU and peripheral operation, as shown in the list that follows.

1. **High-Speed PLL.** All clocks are at their fastest speed and all peripherals are powered up. This is the mode the system enters when activity is detected by the PMU.
2. **Low-Speed PLL.** The internal CPU clock is reduced to a maximum of 4.608 MHz. All other clocks and peripherals operate at full speed. This is the first level of power conservation; it is entered after a specified elapsed time with no activity.
3. **Doze.** The second level of power conservation. The CPU, system, and DMA clocks are stopped. The high-speed PLL is turned off. This mode is entered after a specified elapsed time with no activity.
4. **Sleep.** Additional clocks and peripherals are stopped after additional inactivity has been detected. The exact parameters can be programmed. The Low-Speed PLL can be left on, so a quick startup is possible.
5. **Suspend.** Virtually all of the system is shut down, including all clocks, the 8254 timer, and the Phase Locked Loops (a programmable recovery time is associated with this mode). The 32.768-kHz clock input is still running.
6. **Off.** This level is virtually the same as Suspend mode. Two outputs can be programmed to change state when the transition from Suspend mode to Off mode occurs. DRAM refresh can be disabled in OFF mode.

In addition, the ÉlanSC300 microcontroller can manage the power consumption of peripheral devices. This control can be forced upon entering a specific operating mode or it can be handled directly by firmware. The ÉlanSC300 microcontroller PMU controls five power management control (PMC) pins that are controlled by the operating modes.

Clock Generation

The ÉlanSC300 microcontroller requires only one 32.768-kHz clock input that is used to generate all other clock frequencies required by the system. This 32.768-kHz clock input is provided through the X32IN and X32OUT pins and the crystal oscillator circuit. This input frequency is then used to internally drive multiple Phase-Locked Loops that create all necessary frequencies.

The clock rate that is used to drive the internal CPU is determined by the mode of operation of the ÉlanSC300 microcontroller.

The clock generation, control, and distribution scheme are detailed in Figure 1 and Figure 2, which follow.

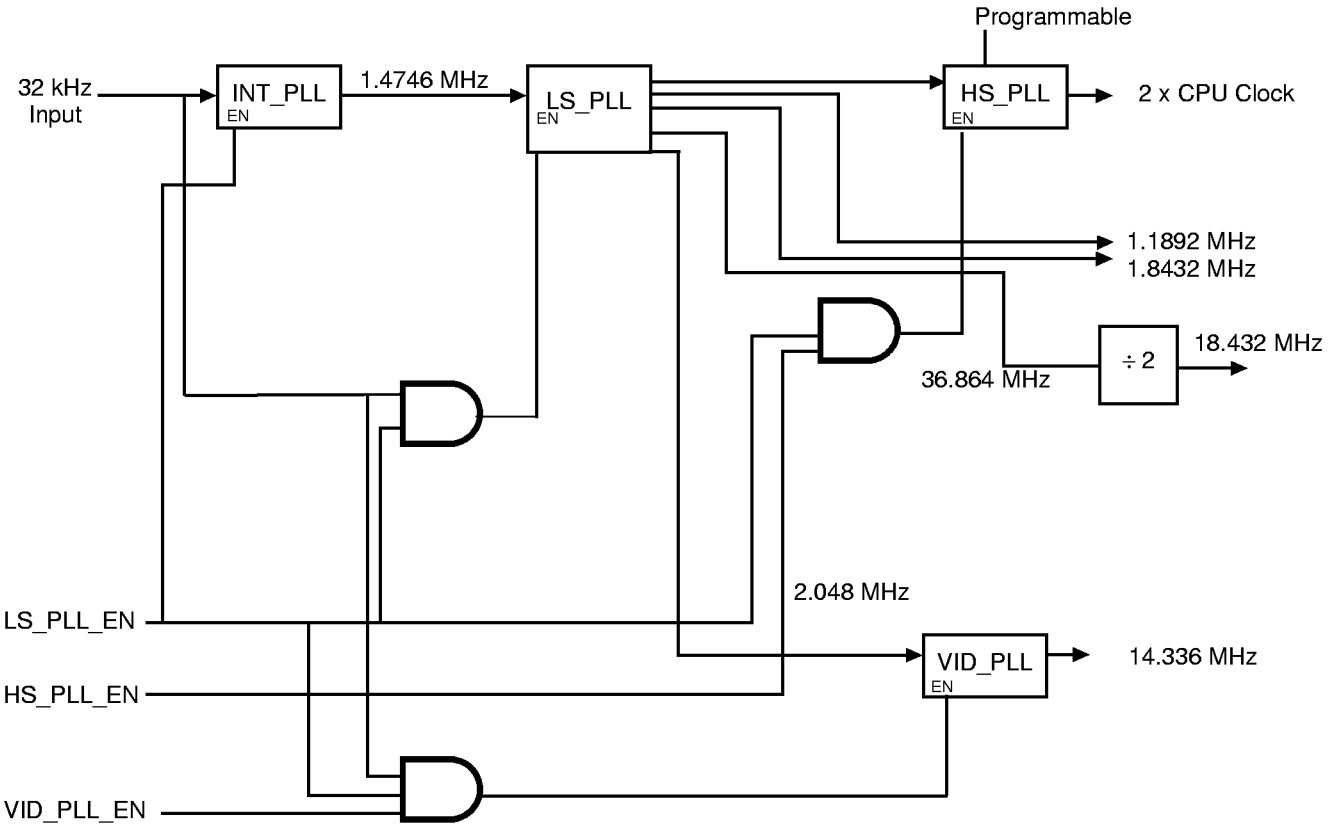


Figure 1. PLL Block Diagram

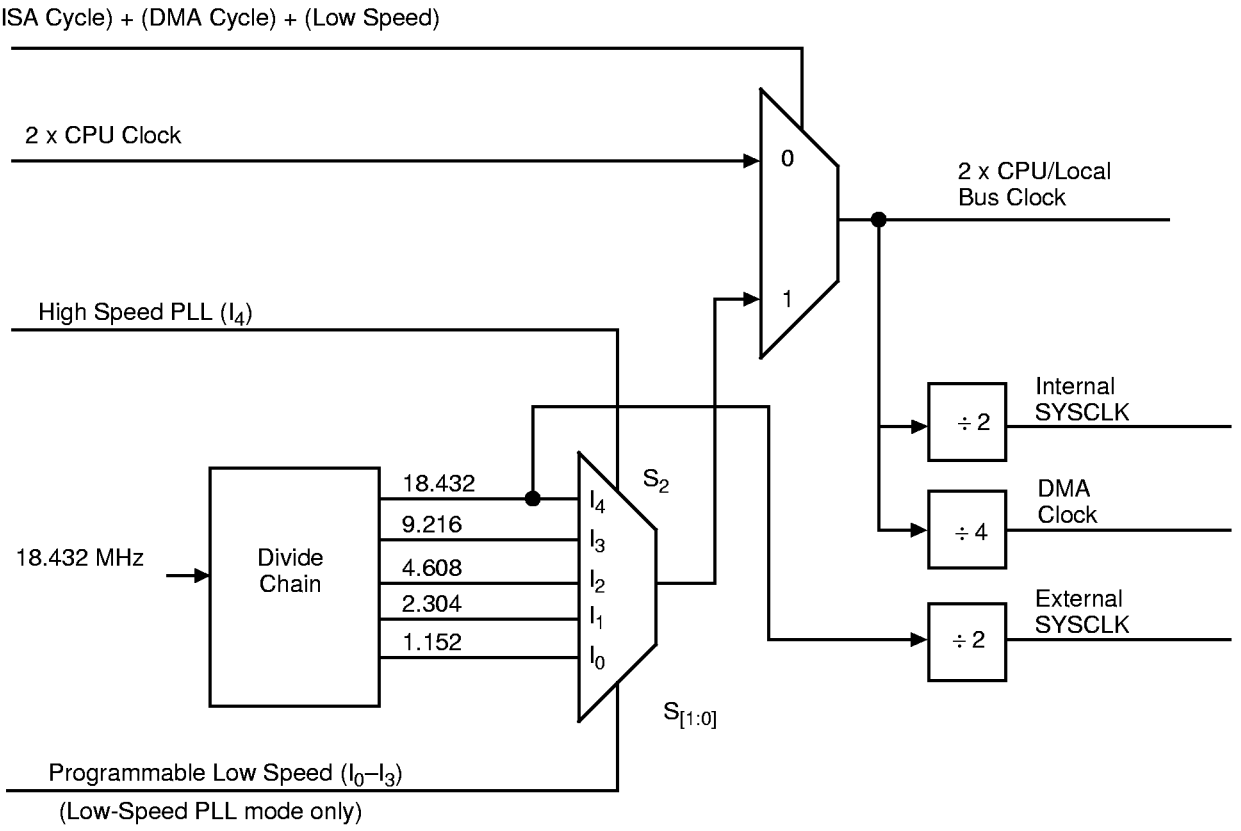


Figure 2. Clock Steering Block Diagram

In the PLL Block Diagram, the INT_PLL is the Intermediate PLL, and is used to multiply the 32.768-kHz input frequency by 45 to produce a 1.4746-MHz input for use by the LS_PLL and the VID_PLL. The LS_PLL, or Low-Speed PLL, is used to again multiply the 1.4746-MHz input by 25 to produce a 36.864-MHz output. This output of the LS_PLL is then divided down to provide the frequencies shown in Table 21.

The LS_PLL also generates a 2.048-MHz signal used by the VID_PLL or Video PLL to generate the 14.336-MHz clock used by the Internal LCD Controller. This frequency is also available on the X1OUT pin for use by an external video controller if selected.

The HS_PLL can be programmed to provide one of the high-speed CPU clock frequencies shown in Table 20.

Table 20. High-Speed CPU Clock Frequencies

2 x CPU Frequency	HS_PLL Output Frequency
40 MHz	39.496 MHz
50 MHz	50.023 MHz
66 MHz	65.829 MHz

ÉlanSC300 Microcontroller Power Management

Dynamic CPU clock switching is the primary form of power management in the ÉlanSC300 microcontroller. When the system is in the High-Speed PLL mode, the ÉlanSC300 microcontroller can be configured to use the High-Speed clock output of the PLL for main memory, local bus accesses, CPU idle cycles, and ROM accesses configured to use the High-Speed clock. During cycles to I/O devices, PCMCIA, ROM, and other external ISA devices, the CPU clock is dynamically switched to the output of the Low-Speed PLL.

During operation in Low-Speed PLL mode, the CPU clock is driven from Low-Speed clock output of the Low-Speed PLL divide chain. The CPU clock frequency used during Low Speed mode is programmable to the following frequencies: 4.608 MHz, 2.304 MHz, 1.152 MHz, and 0.567 MHz. During Doze, Sleep, and Suspend modes of operation, the CPU clock is normally stopped. This clock operates at 9.216 MHz when it is running.

Slow-refresh and self-refresh DRAMs are supported by the ÉlanSC300 microcontroller. The refresh timer source and the refresh rate are selectable. When the CPU clock is stopped, the only clock source for refresh is the 32-kHz clock. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ DRAM refresh is performed.

When the DMA subsystem is idle, the DMA clock control logic stops the clock input to the DMA controllers. The DMA clock is started whenever any of the DREQ inputs go High. When the DMA cycle is in progress, the DMA clock remains active as long as a DREQ input is High or the internal AEN signal is active.

To reduce power consumption in Doze, Sleep, and Suspend modes, the CPU clock is turned off. To further reduce the power consumption in these three modes, the High-Speed PLL is shut off. The Low-Speed PLL is left on by default, but can be programmed to turn off in all three modes.

For information about the signals associated with power management (ACIN, $\overline{\text{BL4}}$–$\overline{\text{BL1}}$, EXTSMI, $\overline{\text{LPH}}$, PGP3–PGP0, PMC4–PMC0, and $\overline{\text{SUS}}$/$\overline{\text{RES}}$), see "Power Management Interface" on page 40. For more information, see Chapter 1 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

Table 21. PLL Output

Phase-Locked Loops	Frequency	Where Used
INT_PLL	1.4746 MHz	LS_PLL and VID_PLL
LS_PLL	36.864 MHz	Divide by 2
	1.8432 MHz	16450 UART clock
	1.1892 MHz	8254 Timer clock
HS_PLL	39.496 MHz, 50.023 MHz, or 65.829 MHz	Input to high speed/low speed MUX
VID_PLL	14.336 MHz	LCD Controller

Table 22. PMU Modes

Mode	Description
Power On	After Power-on reset, system enters High-Speed PLL mode.
High-Speed PLL	The system will be in this mode as long as activities are detected by activity monitor (described in the Programmable Activity Mask Registers, Indexes 08h, 75h, and 76h).
Low-Speed PLL	The system will enter this mode from High-Speed PLL mode after a programmable 1/512 s to 1/2 s, or 1/16 s to 16 s of inactivity.
Doze	The system will enter this mode from Low-Speed PLL mode after a programmable 1/16 s to 16 s, or 1/2 s to 128 s of inactivity.
Sleep	The system will enter this mode from Doze mode after a programmable 4 s to 17 minutes of inactivity.
Suspend	The system will enter this mode from Sleep mode after a programmable 1/16 s to 16 s of inactivity.
Off	The system will enter this mode from Suspend mode after a programmable 1 to 256 minutes of inactivity.

Table 23. Internal Clock States

Mode	High-Speed CPU CLK	Low-Speed CPU CLK	VIDEO CLK	DMA CLK	SYSCLK	8254 CLK (Timer)	16450 CLK (UART)
High-Speed PLL	33/25/20 MHz	9.2 MHz	14.336 MHz	4.6 MHz	9.2 MHz	1.19 MHz	1.8432 MHz
Low-Speed PLL	4.608/2.304/ 1.152/0.567 MHz	4.608/2.304/ 1.152/0.567 MHz	14.336 MHz	2.3/1.2/ 0.58/0.29 MHz	9.2 MHz	1.19 MHz	1.8432 MHz
Doze	DC[1]	DC[1]	14.3 MHz/DC[2]	DC[1]	9.2 MHz/DC[2]	1.19 MHz/DC[2]	1.8 MHz/DC[2]
Sleep	DC	9.2 MHz/DC[4]	14.3 MHz/DC[2]	4.6 MHz/DC[4]	DC	1.19 MHz/DC[2]	1.8 MHz/DC[2]
Suspend	DC	9.2 MHz/DC[4]	14.3 MHz/DC[2]	4.6 MHz/DC[4]	DC	1.19 MHz/DC[2]	1.8 MHz/DC[2]
Off	DC	9.2 MHz/DC[4]	14.3 MHz/DC[3]	4.6 MHz/DC[4]	DC	1.19 MHz/DC[3]	1.8 MHz/DC[3]

Notes:

All power management features will be disabled when AC power is detected via the ACIN pin being High. A register is provided to implement "software ACIN" by writing 1 to bit 5 in the Miscellaneous 6 Register, Index 70h.

The DMA clock can be stopped except during DMA transfers. The Function Enable Register, Index B0h, controls this function.

The CPU clock speed in Low-Speed PLL mode is selectable, (see the PMU Control 3 Register, Index ADh).

The CPU Clock speed:

1. *Can be programmed to run intermittently (on IRQ0) at 9.2 MHz.*
2. *Programmable option (but not on per-clock basis; i.e., all clocks with this note are controlled by a single ON/OFF select for that PMU mode).*
3. *Programmable option, will reflect setting in Suspend mode.*
4. *Can be programmed to run at 9.2 MHz during temporary-on NMI/SMI handlers.*

PMC and PGP Pins

The ÉlanSC300 microcontroller supports five power management control (PMC) pins and four programmable general purpose (PGP) pins. The PMC pins can be used to control the VCC rails of peripheral devices. The PMC pins are related to the operating modes of the ÉlanSC300 microcontroller PMU. The PGP pins can be used as general I/O chip selects for various uses.

The PMC4–PMC0 pins are controlled by Configuration Registers at Indexes 80h, 81h, ABh, and ACh. Each pin can be programmed to be activated upon entry into any of the PMU modes or driven directly by software. PMC0 can be activated when the system is in High-Speed PLL or Low-Speed PLL modes; PMC1 when the system is in Doze mode; PMC2 when the system is in Sleep mode; PMC3 and PMC4 when the system is in Suspend mode; or just about any other combination. These pins can then be used by the system designer to shut off power to particular peripherals when the system enters certain modes, just as internal clocks are slowed or stopped in these modes. Upon the rising edge of $\overline{\text{RESIN}}$, PMC0, PMC1, PMC2, and PMC4 are asserted Low and PMC3 is asserted High. Prior to this edge, these signals are undefined.

The ÉlanSC300 microcontroller can be programmed to reset a timer when an I/O access to a preset address range is detected. If no I/O activity in that range occurs before the timer expires, the ÉlanSC300 microcontroller can assert a PMC signal to turn off the device. When S/W accesses that address range later, the ÉlanSC300 microprocessor can generate a System Management Interrupt (SMI) to the processor, which then activates an SMI handler routine. This routine then can determine the cause of the SMI and take appropriate action, such as powering the I/O device back on.

The PGP3–PGP0 pins are controlled by several configuration registers (70h, 74h, 89h, 91h, 94h, 95h, 9Ch, A3h, and A4h) and their behavior is very flexible. PGP0 and PGP1 can be programmed as input or output. PGP2 and PGP3 are dedicated outputs. PGP1 and PGP3 can be gated with I/O reads, PGP0 and PGP2 can be gated with I/O writes, or each can act as an address decode for a chip select.

Micro Power Off Mode

Micro Power Off mode is the power management mode that is used for battery backup.

Micro Power Off mode allows the system designer to remove power from the VCC1, VSYS, VSYS2, VCC5, and optionally, VMEM power inputs to the microcontroller. This allows the RTC timer and RAM contents to be kept valid by using a battery back-up power source on the VCC core and AVCC pins, which typically should use only 25 µA in this mode.

The following paragraphs describe the ÉlanSC300 microcontroller in Micro Power Off mode. The following are distinctive characteristics:

- Minimum Power Consumption mode (approximately 25 µA typical, AVCC, and Core VCC combined; AVCC and VCC are mandatory for Micro Power Off mode).
- Allows the system designer to utilize the internal RTC and RTC RAM to maintain time, date, and system configuration data while the other system peripherals are powered off.
- Provides the system designer with the option of keeping the system DRAM powered and refreshed while other system peripherals are powered off. Self-refresh and $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh DRAMs are supported.
- Minimal external logic required to properly control power supplies and/or power switching.
- No external buffering required to properly power down system hardware.

The ÉlanSC300 microcontroller allows a system designer to easily maintain the internal RTC and RTC RAM and optionally, the DRAM interface, while the rest of the system peripherals attached directly to the device are powered off. All ÉlanSC300 microcontroller power pins associated with the I/O pins of external powered-off peripherals must be powered down also. This, in addition to internal termination, provides the required isolation to allow the external peripherals to be powered off.

Automatically controlled internal I/O termination is provided to terminate the internal nodes of the ÉlanSC300 microcontroller properly when required.

The DRAM $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, or self-refresh, can be maintained by the ÉlanSC300 microcontroller in this Micro Power State, if configured to do so, utilizing the 32-kHz oscillator. This clock continues to drive the RTC and a portion of the core logic. See the *Élan™SC300 and Élan™SC310 Microcontrollers Solution For Systems Using a Back-up Battery Application Note*, order #20746 for more information about the 32-kHz oscillator and the RTC. The VMEM power plane (DRAM/SRAM section power) must remain powered on if the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh option is selected while in the Micro Power state. The VMEM power plane must also remain powered on if the self-refresh option is selected and the specific DRAM device requires any of its control pins (i.e., $\overline{\text{WE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, etc.) to remain inactive in the Self-Refresh mode. If this is not required, it may be possible for the system designer to remove power from the VMEM pins when entering the Micro Power state, even when the Self-Refresh mode DRAMs remain powered on.

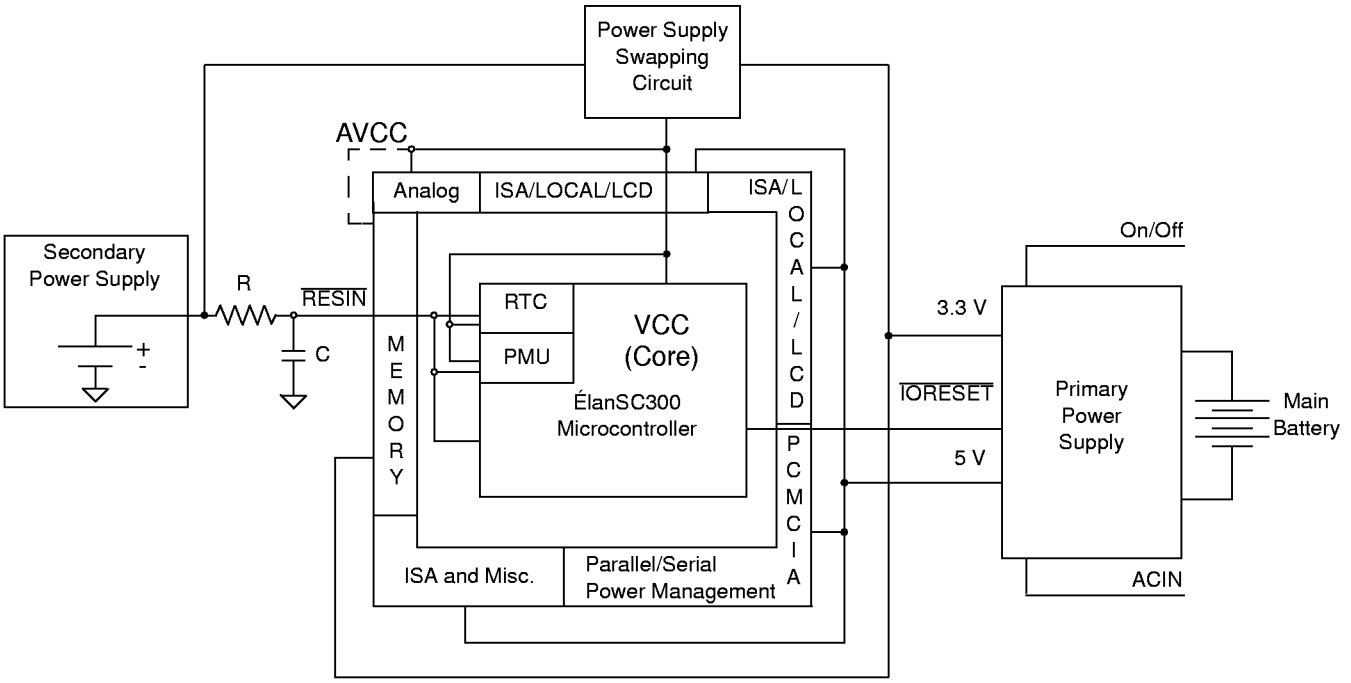


Figure 3. Typical System Design with Secondary Power Supply to Maintain RTC When Primary Power Supply is Off (DRAM Refresh is Optional.)

A portion of a typical system using a secondary power supply to maintain the RTC and RTC RAM (and optionally system DRAM) is shown in Figure 3. This secondary power supply could be as simple as a small lithium coin cell battery as indicated in the diagram, but is certainly not limited to this. Note that when all primary power supply outputs are turned off, all of the system's peripherals are powered off (DRAM optional), all of the ÉlanSC300 microcontroller's power planes are powered off except AVCC (analog) and VCC (core), and the secondary power supply is "switched in" to maintain the ÉlanSC300 microcontroller's core and analog power source.

For more information about back-up batteries, see the *Élan™SC300 and Élan™SC310 Microcontrollers Solution For Systems Using a Back-up Battery Application Note*, order #20746.

The $\overline{\text{RESIN}}$ pin acts as the master reset. When active, all of the internal registers and components are reset, including the RTC, and the RTC RAM invalid bit will be set. This causes an issue with the power-loss bit (VRT), Index 0Dh, bit 7 of the RTC map. The VRT bit is intended to provide a method of determining when the RTC core voltage supply has dropped below an acceptable level.

On a 146818A-compatible device, anything below 2.4 V will cause a low-battery condition and will cause the power-loss bit to go Low. On the ÉlanSC300 microcontroller, the 32-KHz clock used by RTC to maintain time stops oscillating before the VRT bit or RAM contents get cleared because the VRT bit will only get cleared when the $\overline{\text{RESIN}}$ pin is asserted Low. Thus, the RTC time will be inaccurate even though the RAM contents are valid and the VRT bit is still set.

Note: *Although the 32-KHz clock stops oscillating before the power-loss bit is cleared, this event occurs well before the 2.4-V specification for proper ÉlanSC300 microcontroller functionality.*

The $\overline{\text{RESIN}}$ pin should only be asserted (pulsed) Low when a power source is initially applied to the device's core and analog sections.

For more information about these notes, see the Élan™SC300 and Élan™SC310 Microcontrollers Solution For Systems Using a Back-up Battery Application Note*, order #20746.*

The $\overline{\text{IORESET}}$ signal is intended to be the normal "POWER GOOD" status from the primary power supply in the example design shown in Figure 3. The $\overline{\text{IORESET}}$ input does not reset the RTC and will not set the RTC RAM invalid bit.

$\overline{\text{IORESET}}$ (when the inactive state is detected) will cause the ÉlanSC300 microcontroller to go through its power-up sequence including PLL start-up for clock generation and an internal CPU reset. See Figure 32 through Figure 35, beginning page 100, for the initial power-up timing requirements and for Micro Power mode exit timing.

When entering Micro Power Off mode and the primary power supply outputs are turned off, all of the ÉlanSC300 microcontroller's powered-down I/O pins are essentially tri-stated and the internal pull-ups are removed because the VCCIO and VCC CLAMP of the output driver have been removed, as shown in Figure 34 on page 101. This provides the ability to power off external peripherals that are attached directly to the ÉlanSC300 microcontroller without concern of driving current into the pins of the external powered-down device.

To assure that the ÉlanSC300 microcontroller does not draw excessive power while in this state, internal pull-down resistors will be enabled. Enabling these resistors keeps the input buffers from floating (see Figure 4).

The ÉlanSC300 microcontroller samples the two reset inputs ($\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$) to logically determine what state the power pins are in; and, in turn, controls the internal pull-down resistors. Note that in Micro Power Off mode, the $\overline{\text{IORESET}}$ input should be terminated with a pull-down resistor if not driven Low by an external device (see Table 24 on page 59 for information about internal I/O pull-down states).

Micro Power Off DRAM Refresh

Refresh can be either enabled or disabled during Micro Power Off mode, and the VMEM power can be optionally removed, provided that either the memory is also powered off or all DRAM interface signals are kept at 0 V. See the timing diagrams in Figure 34 and Figure 35 on page 101 for more information.

The system designer has the option to keep the system DRAM powered up and refreshed while the ÉlanSC300 microcontroller is in the micro power state. A configuration bit, the Micro Power Refresh Enabled bit, exists in the PMU section of the core logic to realize this feature. This is bit 2 of the Miscellaneous 3 Register at Index BAh. If this bit is cleared (default), the core logic associated with the DRAM refresh will be disabled when the ÉlanSC300 microcontroller is in the Micro Power state. If the bit is set, the core logic associated with the DRAM refresh will be enabled and functional while the ÉlanSC300 microcontroller is in its Micro Power state.

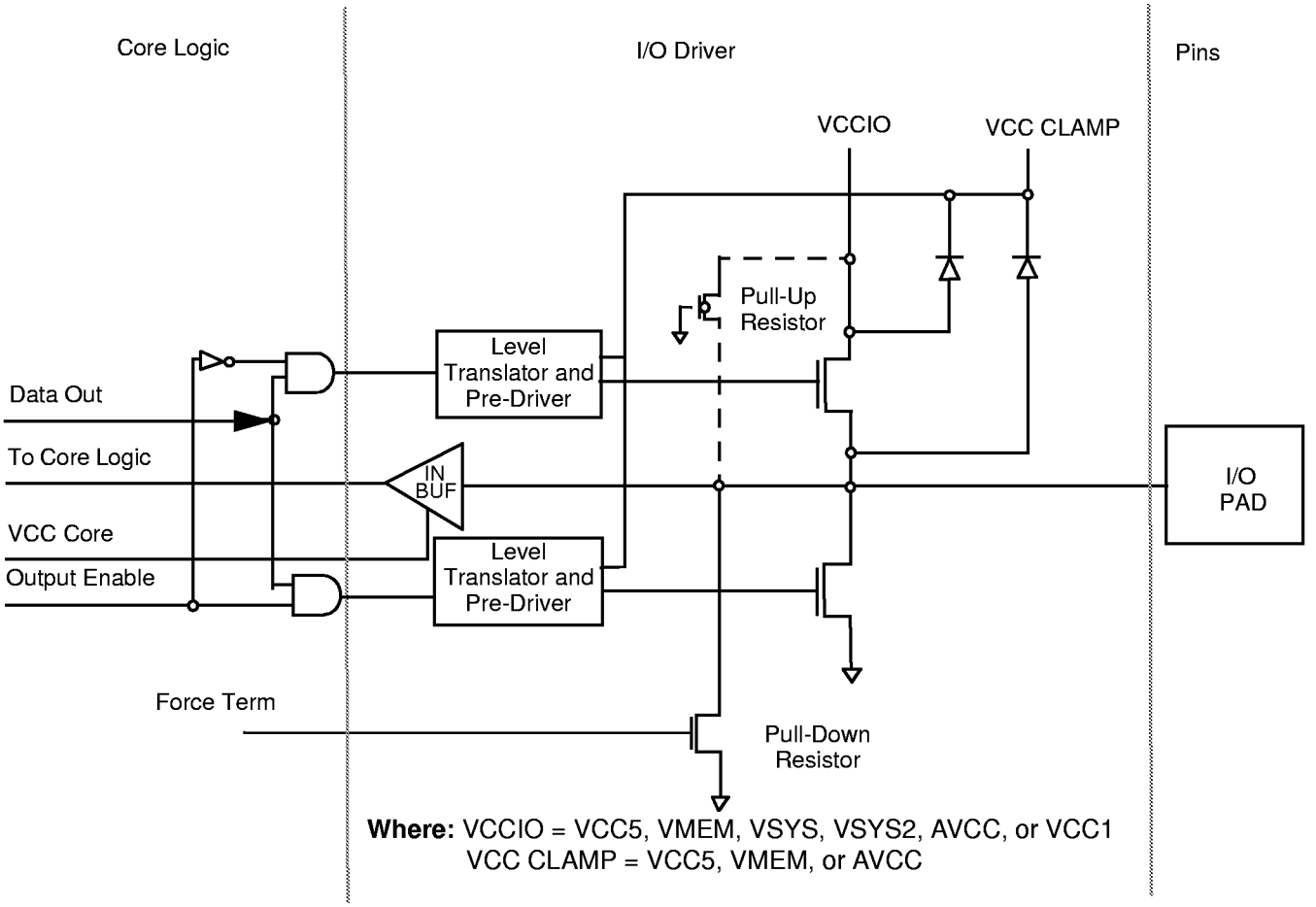


Figure 4. ÉlanSC300 Microcontroller I/O Structure

The type of Micro Power DRAM refresh performed (CAS-before-RAS refresh, or self refresh) will be the same as that for which the part was configured before the IORESET pin sampled Low. If the micro power refresh feature is enabled for CAS-before-RAS refresh, the system designer should maintain power on the VMEM power pin of the ÉlanSC300 microcontroller and not remove power from the DRAM devices. If the micro power refresh feature is enabled for self refresh, the system designer may or may not be required to maintain power on the VMEM power pin of the ÉlanSC300 microcontroller, depending on the specific requirement of the DRAM device in Self-Refresh mode. Power should not be removed from the DRAM device itself in either case.

The Micro Power Refresh bit will always be cleared whenever the RESIN input is sampled Low. Therefore, when the core is initially powered up, the Micro Power DRAM refresh feature will be disabled. This bit is unaffected by the IORESET input. This bit will provide the system BIOS with a mechanism to determine whether or not the system DRAM data has been retained after a reset (IORESET) has occurred.

If Self-Refresh mode is selected and enabled for Micro Power Off mode, then when Micro Power Off mode is exited, the ÉlanSC300 microcontroller will properly force a CAS-before-RAS refresh cycle to cause the DRAMs to exit the Self-Refresh mode. The ÉlanSC300 microcontroller then transitions to the normal CAS-before-RAS refresh mode. This functionality is exactly the same as the Self-Refresh mode exit when the CPU Clock Stopped mode is exited. The ÉlanSC300 microcontroller generates one CAS-before-RAS refresh cycle to force the DRAM to exit the Self-Refresh mode. This is also true for the Micro Power DRAM refresh feature.

The timing diagrams in Figure 34 and Figure 35, on page 101, show the sequence required to guarantee a proper transition into the Micro Power state. This sequence is especially critical when the DRAM refresh option is selected. Note that the power pins of the ÉlanSC300 microcontroller must be kept stable for some time after the IORESET input has gone active. "Stable" means that these power pins should remain at least at their VCC (min) value for the specified time indicated in Table 51 on page 99.

RESIN and IORESET

The ÉlanSC300 microcontroller has two reset inputs to support the Micro Power Off mode. These two inputs are RESIN and IORESET. If Micro Power off mode is not to be used, the system designer should drive these two inputs from a common power-on reset source. Note that the RESIN signal is a 3.3-V only input and is not 5-V safe. For more information, see Table 24 on page 59.

RSTDRV Signal Timing

RSTDRV is High True output of the ÉlanSC300 microcontroller and is a function of the internal core's reset state, the state of the RESIN and IORESET signals, and the value for the PLL start-up timer in the Clock Control Register (Index 8Fh). (See "Loop Filters" on page 97 for more information.) RSTDRV indicates that the PLLs are gated off from the core and prevents the CPU from executing instructions until the PLL outputs have stabilized.

RSTDRV is asserted immediately whenever VCC power is applied and either RESIN or IORESET is asserted. The pulse width of RSTDRV may vary and is determined by the PLL start-up timer and whether or not IORESET and/or RESIN is deasserted (i.e., cold boot versus warm reset or Micro Power Off mode exit).

On a cold boot, when RESIN is asserted while power is applied to the VCC inputs and then deasserted after time delay (t1), the RSTDRV is immediately asserted when power is applied, and then held True until RESIN and IORESET are deasserted. Because the assertion of RESIN causes all the configuration registers to be reset to their default values, the PLL start-up time value in the Clock Control Register is set to 4 ms and is insufficient time for the PLLs to start up. This is why the VCC-to-RESIN timing specification (t1) of 1 second is required to allow sufficient time for the crystal and the PLLs to power up and stabilize before RESIN and IORESET allow RSTDRV to be deasserted.

On a warm reset, the power stays on and the VCC inputs are already powered up while the PLLs are either powered and running or gated off. RSTDRV is asserted quickly after RESIN is asserted, with the pulse width also determined by the RESIN pulse width, because the default PLL start-up timer has a value of 4 ms. It is therefore recommended that the system design guarantees at least a minimum RESIN pulse width of 250 ms for warm resets.

On a wake-up from Micro Power Off mode, VCC and AVCC power to the core is maintained active, and the Clock Configuration Register value for the PLL start-up timer is preserved, but power is removed from all the other VCC inputs, and the PLLs are gated off. RSTDRV is asserted internally, and the output is driven active as soon as VSYS is powered up. When IORESET is first asserted to go into Micro Power Off Mode, RSTDRV is immediately asserted High. When power is removed from the VSYS input (which is also VCCIO for RSTDRV), the voltage level of RSTDRV begins to decay at the same rate as VSYS until it reaches approximately 0.7 V, where it remains while in Micro Power Off mode. This indicates that RSTDRV is still asserted internally inside the microcontroller and is attempting to drive the external pin High, but is unable to without power applied to its I/O driver. When exiting Micro Power Off

mode, as soon as VSYS is powered up, RSTDRV is immediately driven High and will remain High until the IORESET signal is deasserted and the preserved programmed value in the PLL start-up timer has expired.

Force Term

Figure 4 on page 57 shows the schematic diagram, and Table 24 shows the function of the IORESET, RESIN, and Force Term. When in Micro Power Off mode, it is important not to back power any of the powered-off internal power planes. Table 2–Table 11 show the VCCIO and VCC clamp voltage sources for each signal pin. Ensure that all signals, which are either driven by (VCCIO) or clamped to (VCC Clamp) a powered-off voltage source, are also either powered off or driven Low.

PGP Pins

PGP2 and PGP3 can be programmed to be set to a pre-defined state for Micro Power Off mode. For more information, see the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order # 18470.

Micro Power Off Mode Implementation

The system should not be powered up directly into Micro Power Off mode. The system must be allowed to fully power up into High Speed mode upon initial power application of any power source. If a battery has insufficient power for the ÉlanSC300 microcontroller to initialize into High Speed mode, the system design must first power up the ÉlanSC300 microcontroller from the main source, and not allow the chip to be powered from the battery until after it is fully initialized in High Speed mode and properly transitioned into Micro Power Off mode.

This requirement presents an issue when using (for example) a 3-V Lithium battery cell as a back-up power source to prevent the RTC from losing its contents during Micro Power Off mode. If the battery is installed before any other power source is available, the requirement cannot be met because such a small battery is incapable of supplying sufficient power to fully initialize the system. The ÉlanSC300 microcontroller comes up in an undefined state, perhaps drawing sufficient current to drain the battery.

The ÉlanSC300 microcontroller backup power source should be installed only after the system is powered by the main power source prior to a transition into Micro Power Off mode. When the system has transitioned into Micro Power Off mode properly, the simultaneous benefits of low power consumption while maintaining RTC data such as time, date, and system configuration can be realized.

Note: *The timing sequence and specifications for power-up, entering, and exiting Micro Power Off mode must be met. The timing specifications are shown in Table 51 on page 99.*

For more information, see the Élan™SC300 and Élan™SC310 Microcontrollers Solution For Systems Using a Back-up Battery Application Note*, order #20746 and the* Troubleshooting Guide for Micro Power Off Mode on Élan™SC300 and ÉlanSC310 Microcontrollers and Evaluation Boards Application Note*, order #21810.*

Table 24. Internal I/O Pulldown States

IORESET	RESIN	Force Term	Comments
0	0	Active	This condition occurs when any power source is initially turned on. The ÉlanSC300 microcontroller's core and analog VCC is transitioning to on and RESIN is active (the initial power-up state). See the Micro Power Off Mode Implementation section below for more details.
0	1	Active	This condition occurs when the core and analog VCC is stable, the RESIN pin has been inactive, and the primary power supply outputs are off (the normal Micro Power Off state).
1	0	Active	This condition should be treated as condition 0,0 above.
1	1	Inactive	This occurs when the secondary power supply is on, the RESIN input is inactive, and the primary power supply is on and has deasserted IORESET (normal system operating state).

Core Peripheral Controllers

The ÉlanSC300 microcontroller includes all the standard peripheral controllers that make up a PC/AT system, including interrupt controller, DMA controller, counter/timer, and ISA bus controller. For more information, see Chapter 4 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

Interrupt Controller

The ÉlanSC300 microcontroller interrupt controller is functionally compatible with the standard cascaded 8259A controller pair as implemented in the PC/AT.

The interrupt controller block accepts requests from peripherals, resolves priority on pending interrupts and interrupts in service, issues an interrupt request to the processor, and provides the interrupt vector to the processor.

The two devices are internally connected and must be programmed to operate in Cascade mode for operation of all 15 interrupt channels. Interrupt controller 1 occupies I/O addresses 020h–021h and is configured for master operation in Cascade mode. Interrupt controller 2 occupies I/O addresses 0A0h–0A1h and is configured for slave operation. Channel 2 (IRQ2) of interrupt controller 1 is used for cascading and is not available externally.

The output of Timer 0 in the counter/timer section is connected to Channel 0 (IRQ0) of Interrupt controller 1. IRQ0 can be programmed to generate an SMI. See Chapter 1 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470. Interrupt request from the Real-Time Clock is connected to Channel 0 (IRQ8) of Interrupt Controller 2. IRQ13 is reserved for the coprocessor in a PC/AT system and is unavailable on the ÉlanSC300 microcontroller. The other interrupts are available to external peripherals as in the PC/AT architecture via the IRQ15, IRQ14, IRQ12–IRQ9, IRQ7–IRQ3, and IRQ1 inputs. Other sources of interrupts are SMI/NMI and the PIRQ1–PIRQ0 inputs.

The ÉlanSC300 microcontroller interrupt controller has programmable sources for interrupts. These programmable sources are controlled by the configuration registers. For more information, see Chapter 5 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

The Interrupt controller provides interrupt information to the ÉlanSC300 microcontroller power management unit to allow the monitoring of system activity. The ÉlanSC300 microcontroller power management unit can then use the interrupt activity to control the Power Management mode of the ÉlanSC300 microcontroller. For more information, see Chapter 1 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

DMA Controller

The ÉlanSC300 microcontroller DMA controller is functionally compatible with the standard cascaded 8237 controller pair. Channels 0, 1, 2, and 3 are externally available 8 bit channels. DMA Channel 4 is the cascade channel. Channels 5, 6, and 7 are externally available as 16 bit channels.

All the DMA channels are masked off on hardware reset or when writing the DMA master reset register.

Note: *To enable the master to percolate the request to the CPU, you must also unmask the cascade channel (0) on the master.*

The ÉlanSC300 microcontroller supports the power-saving clock stop feature that causes the clock to the DMA controller to stop except when actually needed to perform a DMA transfer. For more information about clock states and programmable clock frequencies, see Table 23 on page 54.

The ÉlanSC300 microcontroller supports Single, Block, and Demand transfer modes; however, software-initiated DMA requests, Cascade mode for additional external DMA controllers, and Verify mode are not supported.

For more information about the DMA controller, see the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

Counter/Timer

The ÉlanSC300 microcontroller's counter/timer is functionally compatible with the 8254 device. A 3-channel, general-purpose, 8254 compatible, 16-bit counter/timer is integrated into the ÉlanSC300 microcontroller. It can be programmed to count in binary or in Binary Coded Decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter. All three are controlled from a common set of control logic, which provides controls to load, read, configure, and control each counter.

All of the 8254 compatible counter/timer channels are driven from a common clock that is internally generated from the LS_PLL 1.1892-MHz output. The output of Counter 0 is connected to IRQ0.

Additional Peripheral Controllers

The ÉlanSC300 microcontroller also integrates three other peripheral controllers commonly found in PCs, but not considered part of the "core peripherals," namely a serial port or a Universal Asynchronous Receiver Transmitter (UART), a real-time clock (RTC),

and a parallel port. See Chapter 4 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

16450 UART

The ÉlanSC300 microcontroller chip includes a UART, providing ÉlanSC300 microcontroller systems with a serial port. This serial controller is fully compatible with the industry-standard 16450. In handheld systems, this port can connect to the pen input device or to a modem.

Real-Time Clock

The ÉlanSC300 microcontroller contains a fully 146818A-compatible real-time clock (RTC) implemented in a PC/AT-compatible fashion. The RTC drives its interrupt to power-management logic.

The RTC block in the ÉlanSC300 microcontroller consists of a time-of-day clock with alarm and 100-year calendar. The clock/calendar can be represented in binary or BCD. It has a programmable periodic interrupt, and 114 bytes of general purpose static RAM (an extension of the 146818A standard, see the programmer's reference manual for more details).

Parallel Port

The ÉlanSC300 microcontroller parallel port is functionally compatible with the PS/2 parallel port. The ÉlanSC300 microcontroller parallel port interface provides the parallel port control outputs and status inputs, and also the control signals for the parallel port data buffers. The parallel port data path is external to the ÉlanSC300 microcontroller. This interface can be configured to operate in either a Unidirectional (normal) mode or Bidirectional (EPP) mode.

The unidirectional parallel port requires only one external component, the parallel port data latch. This latch is used to latch the data from the data bus and drive the data onto the parallel port data bus, as shown in Figure 5.

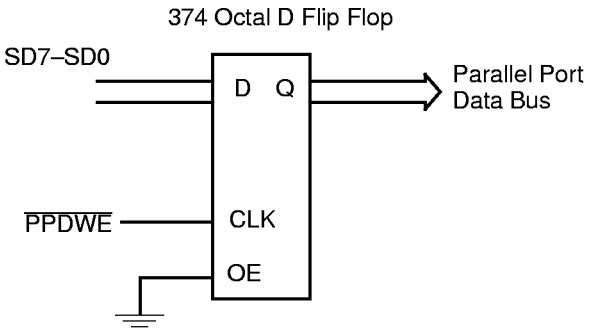


Figure 5. ÉlanSC300 Microcontroller Unidirectional Parallel Port Data Bus Implementation

When the ÉlanSC300 microcontroller parallel port is configured for Bidirectional mode operation, the PPDWE pin is reconfigured via firmware to function as the Parallel Port Data Register address decode (PPDCS). The PPOEN output from the ÉlanSC300 microcontroller is controlled via the Parallel Port Control Register Bit 5. This signal is then used to control the output enable of the external parallel port data latch. By setting this bit, the parallel port data latch is disabled, and then data can be transferred from an external parallel port device into the ÉlanSC300 microcontroller through an external 244 type buffer. A typical bidirectional Parallel Port Data Bus implementation is shown in Figure 6.

If the VCC5 supply pins are connected to a 5-V power supply, then the Parallel Port control signals will be driven by 5-V outputs and can be connected directly to the parallel port connector. If VCC5 is connected to 3.3 V, the parallel port control signals should be translated to 5 V.

The ÉlanSC300 CPU also supports Enhanced Parallel Port (EPP) mode. The EPP mode pins are defined in Table 25.

Note: *If PCMCIA write enable (PCMCWE) and PCMCIA output enable (PCMCOE) are used, the parallel port signals INIT and SLCTIN are not available.*

Table 25. Parallel Port EPP Mode Pin Definition

Normal Mode	EPP Mode	Description
STRB	WRITE	EPP write signal. This signal is driven active during writes to the EPP data or address register.
AFDT	DSTRB	EPP data strobe. This signal is driven active during reads or writes to the EPP data register.
SLCTIN	ASTRB	EPP address strobe. This signal is driven active during reads or writes to the EPP address register.
ACK	INTR	EPP interrupt. This signal is an input used by the EPP device to request service.
BUSY	WAIT	EPP wait. This signal is used to add wait states to the current cycle. It is similar to the ISA IOCHRDY signal.

In Normal mode, the outputs shown in Table 25 function as open-collector or open-drain outputs. In EPP mode, these outputs must function as standard CMOS outputs that are driven High and Low. Figure 6 shows the design that should be used to support EPP mode.

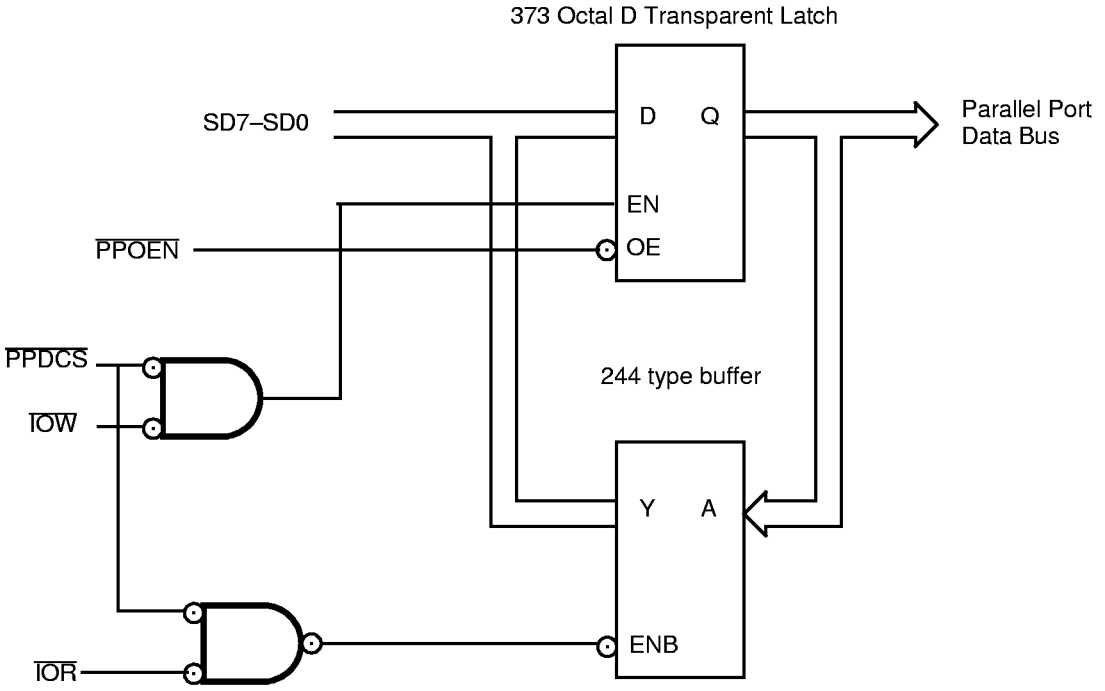


Figure 6. The ÉlanSC300 CPU Bidirectional Parallel Port and EPP Implementation

Parallel Port Anomalies

General

The ÉlanSC300 microcontroller parallel port can be physically mapped to three different I/O locations or can be completely disabled. These I/O locations are 3B(x)h, 37(x)h, and 27(x)h. Typically the system BIOS or a software driver sets up the port at system boot time. Generally, LPT1 is set up by software to be associated with IRQ7, and LPT2 (and LPT3 if desired) is set up to be associated with IRQ5. In the ÉlanSC300 microcontroller, the parallel port is always associated with IRQ7. This cannot be changed regardless of the I/O location to which the parallel port is mapped.

Local Bus or Maximum ISA Configuration

When the ÉlanSC300 microcontroller is configured for some bus mode other than the internal CGA controller option, the system BIOS should disable the internal video controller at boot time. This is done by setting bit 5 of the Screen Control Register 2, Index 19h in the CGA Index address space.

Control Register 1, Index 20h in the CGA Index address space, controls the parallel port mapping. When the internal CGA controller is disabled, Control Register 1 cannot be accessed until the part is reset. Therefore, once the internal CGA controller has been disabled, the parallel port cannot be remapped. This can cause the system boot sequence to require modification such that the parallel port is set up prior to the disabling of the internal video controller. In addition, any software driver or setup utility which was loaded after the internal video controller was disabled would not have the ability to remap the parallel port location if it was required. For more information about parallel ports, see Chapter 4 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

PC/AT Support Features

The ÉlanSC300 microcontroller provides all of the support functions found in the original PC/AT. These include the Port B status and control bits, speaker control, extensions for fast reset, and A20 gate control. (Fast CPU reset and fast A20 gate functions are controlled by either the Miscellaneous 1 Register, Index 6Fh, or port 92h). For more information, see Chapter 4 of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

The ÉlanSC300 microcontroller also includes support for port B, and a miscellaneous PC/AT register that allows direct programming of the speaker via the SPK line. In addition, the ÉlanSC300 microcontroller also generates a chip select and clock source for an external, standard 8042 keyboard controller or the PC/XT keyboard feature. For more information, see Appendix B of the *Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.

Port B and NMI Control

Port B is a PC/AT-standard miscellaneous feature control register that is located at I/O address 061h. The

lower 4 bits of the 8-bit register are read/write control bits that enable or disable NMI check condition sources and sound generation features. The top, or most significant, 4 bits are read/write bits that return status and diagnostic information and control the PC/XT keyboard interface.

There is a master NMI enable function provided that can inhibit any NMIs from reaching the CPU regardless of the state of the individual source enables. This master NMI control is located as a single bit (7) of the register at I/O address 070h. The default value for the NMI enable bit is 1, which inhibits NMI generation.The NMI enable bit (7) is a write-only bit, and is active Low. The remaining bits of the register located at 070h (6–0) control the RTC function. Because the RTC portion of this register is only 7 bits wide and is also write only, there is no conflict between the two functions. This register is discussed in more detail in the RTC section of Chapter 4 of the *ÉlanSC300 Microcontroller Programmer's Reference Manual*, order #18470.

Speaker Interface

The PC/AT standard tone generation interface for the system speaker is implemented in the ÉlanSC300 microcontroller. There are two data paths to the SPKR pin of the device. The first path is driven by the output Channel 2 of the internal 82C54 counter/timer. The counter/timer can be programmed in various ways to generate a waveform at the output, OUT2. Also, the gate input of timer Channel 2 is controlled by the T2G bit in Port B. The timer gate can be used to inhibit tone generation by the timer channel. The second path is driven directly by the SPK bit in port B. This bit can be manipulated by the CPU to generate almost any digital waveform at the SPKR pin.

Fast A20 Address Control

With the ÉlanSC300 microcontroller, full Real mode address compatibility requires that address rollover at the 1-Mbyte address boundary be handled the same way as the early 8088-based PCs were handled. This requires the system address line 20 to have the capability of being forced to 0 during Real mode execution. Control of the A20 line is supported from multiple sources.

The A20G signal in PC/AT systems is normally connected to an output of the PC/AT keyboard controller. A logic High on this input forces the pass through of the CPU's A20 onto the internal system address bus. A logic Low on this input forces the system address bus A20 line Low, as long as the internal A20 gate control is not being utilized.

The ÉlanSC300 microcontroller provides a high-performance method for controlling the system A20 line, independent of the relatively slow PC/AT keyboard controller. This internal A20 gate control is generated by the Miscellaneous 1 Register, Index 6Fh, and Port 92h.

For more information, see the *Élan™SC300 and ÉlanSC310 Microcontrollers GATEA20 Function Clarification Application Note*, order #21811.

Reset Control

An external hardware reset is required in order to correctly initialize internal logic after system power-up. See the required timings in Table 51 on page 99. System power supplies typically have a POWERGOOD output signal that is used as an active Low asynchronous reset input for the device. $\overline{\text{IORESET}}$ is intended to be driven by a POWERGOOD-compatible signal. When $\overline{\text{IORESET}}$ is driven Low, the ÉlanSC300 microcontroller resets all of its internal logic with the exception of the RTC Valid Data/Time bit (Register D, RTC Index 0Dh, bit 7) and some internal register configuration bits. The $\overline{\text{RESIN}}$ input is intended to be driven by a signal that indicates that the battery back-up source has been disconnected. When $\overline{\text{RESIN}}$ is driven Low, the ÉlanSC300 microcontroller resets all of its internal logic. The $\overline{\text{RESIN}}$ input buffer is a Schmitt trigger for tolerance of slow rise and fall times on the signal. $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ are internally synchronized to the CPU clock to provide the internal hardware reset.

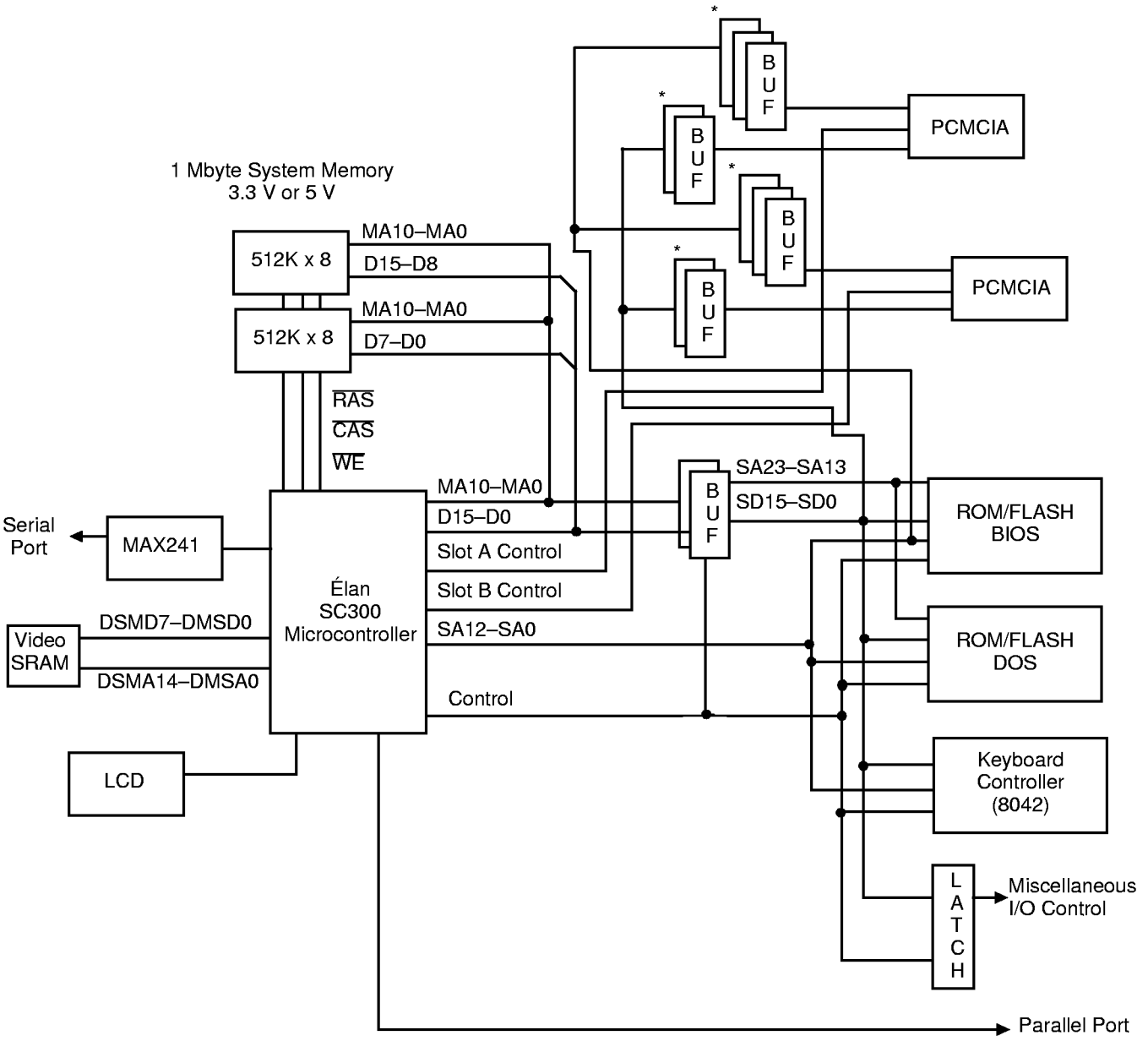
For more information, see Table 24 on page 59 and "Micro Power Off Mode" on page 55.

Besides the device hardware reset, the internal CPU has several other possible reset sources. These other sources only generate CPU reset.

In a standard PC/AT-type system, an $\overline{\text{RC}}$ (CPU Reset) pin is typically connected to an output of the 8042 keyboard controller.

Also, an internal configuration register can be used to reset the CPU in less time than that required by the external keyboard controller. The internal reset is controlled by the Miscellaneous 1 Register, Index 6Fh, and Port 92h.

The ÉlanSC300 microcontroller provides both of the CPU reset functions described above and also triggers a CPU reset upon processor shutdown. If the CPU reaches a state where it cannot continue to execute because of faults and error conditions, it will issue a status code indicating shutdown, and the CPU will halt operation with no means of continuing except for a reset. If this shutdown status is detected, a 16 clock minimum pulse width reset is automatically sent to the CPU.



Note:

**Optional*

Figure 7. Typical System Block Diagram (Internal LCD Controller)

LCD, Local Bus, or Maximum ISA Bus Controller

Depending on the configuration chosen, the ÉlanSC300 microcontroller's pin functionality will differ. The three different options are Internal CGA Controller, Local Bus, and Maximum ISA Bus modes. The pin options are selected upon power-up reset. Only Internal CGA, Local Bus, or Maximum ISA Bus mode is available in a particular design. Both Internal CGA and Local bus modes do, however, provide a subset of the ISA bus.

The three sets of pin descriptions are described in "Alternate Pin Functions Selected Via Firmware" on page 71.

Internal CGA Controller Option

The internal video controller is fully 6845 compatible, supporting up to 640 x 200 pixel LCD panels. This option supports an external 32-Kbyte SRAM for video memory. The smallest subset of the ISA bus is available when using the internal CGA controller.

Local Bus Option

The local bus interface is integrated with the memory controller and the ISA bus controller, and it permits fast transfers to and from external local bus peripherals, such as video controllers. The local bus option is basically an Am386SXLV microprocessor local bus with an $\overline{\text{LDEV}}$, $\overline{\text{LRDY}}$, and CPUCLK added. Additional ISA bus signals are available in this mode.

Maximum ISA Bus Option

The Maximum ISA option provides the most ISA bus signals of any of the ÉlanSC300 microcontroller bus options. Since master cycles and ISA refresh are not necessary in handheld designs, the ÉlanSC300 microcontroller does not provide these signals in any bus mode. The SYSCLK output from the ÉlanSC300 microcontroller is a clock that is normally only used for the external keyboard controller if one exists. This clock is 9.2 MHz and can be stopped completely.

This clock is not related to any of the ISA bus cycle timings. The ISA bus cycle timings vary depending on the clock speed selected for the internal ISA bus clock.

Internal Resistors

The ÉlanSC300 microcontroller's internal pull-down and pull-up resistors are approximately 100-KΩ ± 50% tolerance. They don't provide the level of termination that may be necessary to meet design noise margins or the timing and termination requirements for different bus specifications (e.g., ISA bus or local bus).

The internal pull-up and pull-down resistors only provide adequate termination for when the input is floating and is in a very low noise environment, or for systems where power consumption is too critical to allow for the additional current associated with stronger pullups. Because of this, it is recommended that the designer use the external pull-up and pull-down resistors (shown in Table 26) on signals with critical timing or noise immunity requirements. The external pull-up and pull-down resistors are also recommended for additional design margin, provided that space and power consumption are not major issues.

Table 26. External Resistor Requirements

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
PIRQ0 (PIRQ0/IRQ3)	194	10K		10K		10K		
PIRQ1 (PIRQ1/IRQ6)	193	10K		10K		10K		
IRQ1	195	10K		10K		10K		
IOCHRDY	192	1K		1K		1K		
$\overline{\text{IOCS16}}$ [LCDDL0]	196	1K[–]		1K[–]		1K[–]		1
$\overline{\text{MCS16}}$ [LCDDL1]	197	1K[–]		1K[–]		1K[–]		1
IRQ14 [LCDDL2]	198	10K[–]		10K		10K		1
$\overline{\text{DTR}}$/CFG1	92		100K	10K			100K	2
$\overline{\text{RTS}}$/CFG0	93		100K		100K	10K		2
$\overline{\text{IORESET}}$	140		10K		10K		10K	

Table 26. External Resistor Requirements (Continued)

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
LVEE (IRQ15/IRQ15)	182			10K		10K		
M (IRQ4/IRQ4)	173			10K		10K		
LCDD2 (IOCHCHK/IOCHCHK)	177			1K		1K		
DSWE (PULLUP/PULLUP)	183			100K		100K		
FRM (IRQ12/IRQ12)	181			10K		10K		
CP2 (PULLUP/IRQ10)	179			1K		10K		
DSMA1 (PULLUP/IRQ7)	164			10K		10K		
DSMD0 (LDEV/RESERVED)	148			1K				
LCDD3 (DRQ1/ DRQ1)	174				10K		10K	3
LCDD1 (DRQ5/ DRQ5)	175				10K		10K	3
CP1 (PULLDN/ IRQ5)	178				10K	10K		
DSMD7 (ADS/0WS)	172					1K		
DSMD3 (BHE/IRQ9)	168					10K		
DSMD2 (BLE/IRQ11)	167					10K		
DSMA3 (CPUCLK/PULLUP)	162					1M		
DSMA0 (NC/PULLUP)	165					1M		
DSMD6 (D/C / DRQ0)	171						10K	3
DSMD5 (M/IO / DRQ3)	170						10K	3
DSMD4 (W/R / DRQ7)	169						10K	3
DSMD1 (LRDY / DRQ6)	166			1K			10K	3
DRQ2 [TDO]	76		10K		10K		10K	3
BVD2_A	113	10K		10K		10K		4
BVD1_A	114	10K		10K		10K		4
BVD2_B	119	10K		10K		10K		4
BL1	106	100K		100K		100K		5
BL2	107	100K		100K		100K		5
BL3	108	100K		100K		100K		5
BL4	109	100K		100K		100K		5
SOUT	94			10K				
RST_A	133		100K		100K		100K	
RST_B	127		100K		100K		100K	
BVD1_B	120	10K		10K		10K		4
WAIT_AB	115	10K		10K		10K		4
CD_A	110	10K		10K		10K		4
CD_B	116	10K		10K		10K		4

Table 26. External Resistor Requirements (Continued)

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
RDY_A	111	10K		10K		10K		4
RDY_B	117	10K		10K		10K		4
WP_A	112	10K		10K		10K		
WP_B	118	10K		10K		10K		
$\overline{DCD}$	98	1M		1M		1M		
$\overline{DSR}$	97	1M		1M		1M		
SIN	99	1M		1M		1M		
$\overline{CTS}$	96	1M		1M		1M		
$\overline{RIN}$	100	1M		1M		1M		
$\overline{STRB}$	83	4.7K		4.7K		4.7K		
$\overline{AFDT}$	80	4.7K		4.7K		4.7K		
$\overline{INIT}$	89	4.7K		4.7K		4.7K		
$\overline{SLCTIN}$	84	4.7K		4.7K		4.7K		
$\overline{ERROR}$	86	4.7K		4.7K		4.7K		
$\overline{ACK}$	88	4.7K		4.7K		4.7K		
BUSY	85	4.7K		4.7K		4.7K		
PE	82	4.7K		4.7K		4.7K		
SLCT	87	4.7K		4.7K		4.7K		
PGP0	189		100K		100K		100K	6
PGP1	188		100K		100K		100K	6
ACIN	101		10K		10K		10K	5

Notes:

All pull-up and pull-down resistor requirements are specified in ohms.

1. *A [–] implies that for this "programmable" pin function, no external termination is required.*
2. *This pin is an "alternate pin function select input" that is sampled at reset. This pin functions as a normal serial port output after $\overline{RESIN}$ and $\overline{IORESET}$ are deasserted.*
3. *When this pin's function is a DMA request input, it should be terminated with a pull-down resistor if not connected to an external device that drives to a known state.*
4. *If this ÉlanSC300 microcontroller input is driven directly with a logic gate, then no external termination is required at the ÉlanSC300 microcontroller pin. The termination on the PCMCIA socket signal is still required per the PCMCIA 2.1 specification.*
5. *If this ÉlanSC300 microcontroller input is always driven to a known state, then no external termination is required.*
6. *If the pin is configured as an input, it should be terminated with a discrete pull-up or pull-down resistor, or it should always be driven to a known state.*

ALTERNATE PIN FUNCTIONS

To provide the system designer with the most flexibility, the ÉlanSC300 microcontroller provides a means for reconfiguring some of the pin functions, depending on the system requirements. Reconfiguration of the ÉlanSC300 microcontroller pin functions is accomplished in one of two ways, depending on the pin functions that are to be reconfigured. To select the internal LCD controller, CPU local bus interface, or maximum ISA bus interface, the state of the $\overline{DTR}$ and $\overline{RTS}$ pins are sampled on the rising edge of the $\overline{RESIN}$ and $\overline{IORESET}$ signals when power is first applied to the ÉlanSC300 microcontroller. This is shown in Figure 8.

After power has been initially applied and $\overline{RESIN}$ and $\overline{IORESET}$ are deasserted, additional assertions of $\overline{IORESET}$ while $\overline{RESIN}$ = 1 will not cause the pin configurations to change. However, the pin configuration inputs are always sampled in response to $\overline{RESIN}$ assertions. Table 27 shows the pin states at reset to enable the three different pin configurations involving the LCD controller, Local Bus, and Maximum ISA Bus.

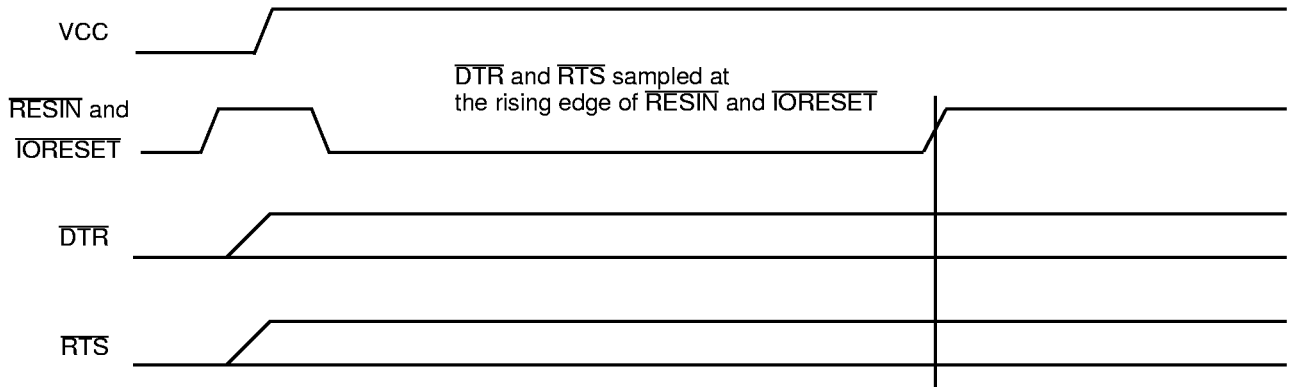
The bus configuration selected can be read in bits 5–6 of the Memory Configuration 1 Register, Index 66h, after the reset.

Table 27. Bus Option Select Bit Logic

Bus Selected	$\overline{DTR}$/CFG1	$\overline{RTS}$/CFG0
Internal LCD	0	0
Local Bus	1	0
Full/Maximum ISA	X	1

The second method of reconfiguring ÉlanSC300 microcontroller pin functions is accomplished by programming the internal configuration registers. This method is used to configure the following functions:

- DRAM or SRAM main memory interface
- Dual-scan LCD interface
- Unidirectional or bidirectional parallel port
- The clock source driving the X1OUT[BAUDOUT] pin
- PCMCIA memory commands
- 14.336-MHz clock



Notes:

This is shown to illustrate when CFG0 and CFG1 are sampled and is not intended to be used for reset timings. For reset timings, refer to Table 51 on page 99

Figure 8. Bus Option Configuration Select

CPU Local Bus Interface versus Internal LCD Interface

The tables of this section are brief descriptions of the alternate pin functions/names and the pin name of the Internal LCD mode function that the alternate function replaces. The CPU Local Bus Interface alternate functions are configured via the $\overline{DTR}$ and $\overline{RTS}$ pin states when the ÉlanSC300 microcontroller is reset.

Table 28. Pins Shared Between CPU Local Bus and Internal LCD Interface Functions

CPU Local Bus Interface Pin Name	Pin Type	CPU Local Bus Interface Pin Description/Notes	Internal LCD Controller Mode Function Pin Name	Pin No.
A23–A12	O	Local Bus Address Bus	DSMA14–DSMA4 $\overline{LVDD}$	145 149–155 158–161
$\overline{ADS}$	O	Address Strobe	DSMD7	172
D/$\overline{C}$	O	Data/Code Cycle Status signal	DSMD6	171
M/$\overline{IO}$	O	Memory/I/O Cycle Status signal	DSMD5	170
W/$\overline{R}$	O	Write/Read Cycle Status signal	DSMD4	169
$\overline{BHE}$	O	Byte High Enable	DSMD3	168
$\overline{BLE}$	O	Byte Low Enable	DSMD2	167
$\overline{LRDY}$	I	Local Device Ready	DSMD1	166
$\overline{LDEV}$	I	Local Bus Device Acknowledge	DSMD0	148
$\overline{CPURDY}$	O	CPU Ready	$\overline{DSOE}$	147
CPUCLK	O	CPU Clock	DSMA3	162
CPURST	O	CPU Reset	DSMA2	163

Notes:

1. *The SA11–SA0 pins are the lower order address lines for local bus cycles in the Local Bus Interface mode.*
2. *See the Table 26 on page 65 for information on required termination for Local Bus and Internal LCD Controller modes.*
3. *Other Internal LCD Controller mode pin functions, which are not listed in this table, change when the Local Bus mode is entered. These pins change to an ISA bus function when Local Bus mode is entered.*

Maximum ISA Interface versus Internal LCD Interface

The maximum ISA interface alternate functions are configured via the $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ pin states when the ÉlanSC300 microcontroller is reset.

Table 29. Pins Shared Between Maximum ISA Bus and Internal LCD Interface Functions

ISA Interface Pin Name	Pin Type	ISA Interface Pin Description/Notes	Internal LCD Controller Mode Function Pin Name	Pin No.
$\overline{\text{IOCHCHK}}$	I	ISA I/O Channel Check input	LCDD2	177
BALE	O	ISA Bus Address Latch Enable	$\overline{\text{LVDD}}$	145
DRQ0	I	DMA Channel 0 Request	DSMD6	171
DRQ1	I	DMA Channel 1 Request	LCDD3	174
DRQ3	I	DMA Channel 3 Request	DSMD5	170
DRQ5	I	DMA Channel 5 Request	LCDD1	175
DRQ6	I	DMA Channel 6 Request	DSMD1	166
DRQ7	I	DMA Channel 7 Request	DSMD4	169
$\overline{\text{DACK0}}$	O	DMA Channel 0 Acknowledge	DSMA7	158
$\overline{\text{DACK1}}$	O	DMA Channel 1 Acknowledge	$\overline{\text{DSCE}}$	146
$\overline{\text{DACK3}}$	O	DMA Channel 3 Acknowledge	DSMA6	159
$\overline{\text{DACK5}}$	O	DMA Channel 5 Acknowledge	LCDD0	144
$\overline{\text{DACK6}}$	O	DMA Channel 6 Acknowledge	DSMA4	161
$\overline{\text{DACK7}}$	O	DMA Channel 7 Acknowledge	DSMA5	160
IRQ4	I	Interrupt Request input	M	173
IRQ5	I	Interrupt Request input	CP1	178
IRQ7	I	Interrupt Request input	DSMA1	164
IRQ9	I	Interrupt Request input	DSMD3	168
IRQ10	I	Interrupt Request input	CP2	179
IRQ11	I	Interrupt Request input	DSMD2	167
IRQ12	I	Interrupt Request input	FRM	181
IRQ15	I	Interrupt Request input	$\overline{\text{LVEE}}$	182
LA23–LA17	O	ISA Non-Latched Address Bus	DSMA14–DSMA8	149–155
LMEG	O	ISA Memory Address Decode Below 1 Mbyte	$\overline{\text{DSOE}}$	147
$\overline{\text{0WS}}$	I	Zero Wait State	DSMD7	172

Notes:

See the External Resistor Requirements section for information on required termination for Maximum ISA Bus and Internal LCD Controller modes.

ALTERNATE PIN FUNCTIONS SELECTED VIA FIRMWARE

The following tables contain brief descriptions of the alternate pin functions/names and the pin names of the default function that the alternate function replaces. These alternate functions are selected via system firmware only.

SRAM Interface

This alternate function is configured by setting bit 0 of the Miscellaneous 6 Register, Index 70h.

Table 30. SRAM Interface

SRAM Pin Name	Pin Type	SRAM Interface Pin Description/Notes	Default Pin Name/Function	Pin No.
[$\overline{\text{SRCS0}}$]	O	SRAM Bank 0 Chip Select. Low Byte	$\overline{\text{CAS0L}}$	6
[$\overline{\text{SRCS1}}$]	O	SRAM Bank 0 Chip Select. High Byte	$\overline{\text{CAS0H}}$	7
[$\overline{\text{SRCS2}}$]	O	SRAM Bank 1 Chip Select. Low Byte	$\overline{\text{CAS1L}}$	4
[$\overline{\text{SRCS3}}$]	O	SRAM Bank 1 Chip Select. High Byte	$\overline{\text{CAS1H}}$	5

Dual-Scan LCD Data Bus

This alternate function is configured via selecting a dual-scan LCD Panel mode in the CGA index address space at Index 18h.

Table 31. Dual-Scan LCD Data Bus

Dual-Scan Pin Name	Pin Type	Dual-Scan LCD Data-Bus Pin Description/Notes	Default Pin Name/Function	Pin No.
[LCDDL0]	O	Dual screen data bit	$\overline{\text{IOCS16}}$	196
[LCDDL1]	O	Dual screen data bit	$\overline{\text{MCS16}}$	197
[LCDDL2]	O	Dual screen data bit	IRQ14	198
[LCDDL3]	O	Dual screen data bit	$\overline{\text{SBHE}}$	143

Notes:
In the dual-scan LCD configuration, $\overline{\text{IOCS16}}$ and $\overline{\text{MCS16}}$ are internally forced inactive.

Unidirectional/Bidirectional Parallel Port

This alternate function is configured via selecting either the Normal Bidirectional mode configuration or the EPP mode configuration for the parallel port in the Function Enable 1 Register, Index B0h.

Table 32. Bidirectional Parallel Port Pin Description

Bidirectional Pin Name	Pin Type	Bidirectional Parallel Port Pin Description/Notes	Default Pin Name/Function	Pin No.
[$\overline{\text{PPDCS}}$]	O	Parallel Port data register address decode	$\overline{\text{PPDWE}}$	90

X1OUT [BAUD_OUT] Clock Source

The internal clock source driving out on this pin is configured via register bits of the Function Enable Registers, Indexes B0h and B1h.

Table 33. X1OUT Clock Source Pin Description

BAUDOUT Pin Name	Pin Type	X1OUT [BAUD_OUT] Pin Description/Notes	Default Pin Name/Function	Pin No.
[BAUD_OUT]	O	Serial baud rate clock	X1OUT	200

Notes:
The default function of this pin is that no clock is driven out and the pin is tri-stated.

PC/XT Keyboard

The PC/XT keyboard functionality is enabled via bit 3 of PMU Control 3 Register, Index ADh.

Table 34. XT Keyboard Pin Description

PC/XT Keyboard Pin Name	Pin Type	PC/XT Keyboard Pin Description/Notes	Default Pin Name/Function	Pin No.
[XTDAT]	I/O	Keyboard data	$\overline{8042CS}$	75
[XTCLK]	I/O	Keyboard clock	SYSCLK	45

PCMCIA Data Path Control

Setting bit 4 of Miscellaneous 3 Register, Index BAh, enables the PCMCIA memory commands on the Parallel port pins SLCTIN and INIT.

Table 35. PCMCIA Data Path Control

PCMCIA Control Pin Name	Pin Type	Data Path Control Pin Description/Notes	Default Pin Name/ Function	Pin No.
[$\overline{PCMCOE}$]	O	PCMCIA Output Enable	$\overline{SLCTIN}$	84
[$\overline{PCMCWE}$]	O	PCMCIA Write Enable	$\overline{INIT}$	89

14-MHz Clock Source

Setting bit 3 of Miscellaneous 3 Register, Index BAh, enables the 14.336-MHz clock signal on the parallel port pin AFDT.

Table 36. 14-MHz Clock Source

14-MHz Pin Name	Pin Type	14-MHz Clock Pin Description/Notes	Default Pin Name/ Function	Pin No.
[X14OUT]	O	14.336 MHz Clock	$\overline{AFDT}$	80

ISA BUS DESCRIPTIONS

The three bus configuration options (Internal LCD controller, local bus, or maximum ISA bus) each support a somewhat different subset of the ISA bus standard. The Internal LCD controller option supports the smallest ISA subset, defined in Table 37.

Table 37. Internal LCD Controller Bus Mode ISA Bus Functionality

Pin Name	I/O	Function
SA23–SA0	O	System Address Bus
D15–D0	B	System Data Bus
IOCHRDY	I	I/O Channel Ready
RSTDRV	O	System Reset
$\overline{\text{MEMW}}$	O	Memory Write
$\overline{\text{MEMR}}$	O	Memory Read
$\overline{\text{IOW}}$	O	I/O Write
$\overline{\text{IOR}}$	O	I/O Read
AEN	O	DMA Address Enable
TC	O	Terminal Count
SYSCLK	O	System Clock (ISA bus timing is not derived from this clock)
IRQ1	I	Interrupt IRQ1
PIRQ0	I	Programmable IRQx
PIRQ1	I	Programmable IRQx
$\overline{\text{DACK2}}$	O	DMA Channel 2 Acknowledge
DRQ2	I	DMA Channel 2 Request
$\overline{\text{IOCS16}}$	I	I/O Device is 16 bits[1]
$\overline{\text{MCS16}}$	I	Memory Device is 16 bits[1]
IRQ14	I	Interrupt Request Input[1]
$\overline{\text{SBHE}}$	O	Byte High Enable[1]
X1OUT [BAUDOUT]	O	Video Oscillator (14.336 MHz)/ Serial Port Output

Notes:

1. *These ISA functions are available in this mode as long as the internal LCD controller is not configured for a dual-scan LCD panel in which case these pins would be used as additional data bits for the LCD panel. In Local Bus mode and Maximum ISA mode, the ISA function is always available.*

The Local Bus configuration supports a larger ISA subset. The additional pins supported are shown in Table 38. The Maximum ISA Bus configuration adds the pins found in Table .

Table 38. Local Bus Mode Additional ISA Bus Functionality

Pin Name	I/O	Function
IOCHCHK	I	ISA I/O Channel Check
DRQ1	I	DMA Channel 1 Request
$\overline{\text{DACK1}}$	O	DMA Channel 1 Acknowledge
DRQ5	I	DMA Channel 5 Request
$\overline{\text{DACK5}}$	O	DMA Channel 5 Acknowledge
IRQ4	I	Interrupt Request Input
IRQ12	I	Interrupt Request Input
IRQ15	I	Interrupt Request Input

Table 39. Maximum ISA Bus Mode Additional ISA Bus Functionality

Pin Name	I/O	Function
BALE	O	ISA Bus Address Latch Enable
DREQ0	I	DMA Channel 0 Request
DREQ3	I	DMA Channel 3 Request
DREQ6	I	DMA Channel 6 Request
DREQ7	I	DMA Channel 7 Request
$\overline{\text{DACK0}}$	O	DMA Channel 0 Acknowledge
$\overline{\text{DACK3}}$	O	DMA Channel 3 Acknowledge
$\overline{\text{DACK6}}$	O	DMA Channel 6 Acknowledge
$\overline{\text{DACK7}}$	O	DMA Channel 7 Acknowledge
IRQ7	I	Interrupt Request Input
IRQ9	I	Interrupt Request Input
IRQ11	I	Interrupt Request Input
$\overline{\text{0WS}}$	I	Zero Wait State Request
LA23–LA17	O	ISA Non-Latched Address
$\overline{\text{LMEG}}$	O	ISA Memory Cycle Below 100000h
IRQ5	I	Interrupt Request Input
IRQ10	I	Interrupt Request Input

System Test and Debug

The ÉlanSC300 microcontroller provides test and debug features compatible with the standard Test Access Port (TAP) and Boundary-Scan Architecture (JTAG).

The test and debug logic contains the following elements:

- Five extra pins—TDI, TMS, TCK, TDO, and $\overline{\text{TRST}}$ (JTAGEN). JTAGEN is dedicated; the other four are multiplexed.
- Test Access Port (TAP) controller, which decodes the inputs on the Test Mode Select (TMS) line to control test operations.
- Instruction Register (IR), which accepts instructions from the Test Data Input (TDI) pin. The instruction codes select the specific test or debug operation to be performed or the test data register to be accessed.
- Test Data Registers: Boundary Scan Register (BSR), Device Identification Register (DID), and Bypass Register (BPR).

Test Access Port (TAP) Controller

The TAP controller is a synchronous, finite state machine that controls the sequence of operations of the test logic. The TAP controller changes state in response to the rising edge of TCK and defaults to the test-logic-reset state at power-up. Reinitialization to the test-logic-reset state is accomplished by holding the TMS pin High for five TCK periods.

Instruction Register

The Instruction Register is a 4-bit register that allows instructions to be serially shifted into the device. The instruction determines either the test to execute or the data register to access, or both. The least significant bit is nearest the TDO output. When the TAP controller enters the capture-IR state, the instruction register is loaded with the default instruction IDCODE. This is done to test for faults in the boundary scan connections at the board level.

Boundary Scan Register

The Boundary Scan Register is a serial shift register from TDI to TDO, consisting of all the boundary scan register bits and control cells in each I/O buffer.

Device Identification Register

The Device Identification Register is a 32-bit register that contains the AMD ID code for the ÉlanSC300 microcontroller: 195FA003h.

Bypass Register

The Bypass Register provides a path from TDI to TDO with one clock cycle latency. It helps to bypass a chip completely while testing boards containing many chips.

Test Access Port Instruction Set

The following instructions are supported:

- Sample/Preload. This instruction enables the sampling of the contents of the boundary scan registers as well as the serial loading of the boundary scan registers through TDI.
- Bypass. This instruction connects TDI and TDO through a 1-bit shift register, the Bypass Register.
- Extest. This instruction enables the parallel loading of the boundary scan registers. The device inputs are captured at the input boundary scan cell and the device outputs are captured at the output boundary scan cells.
- IDCODE. This instruction connects the ID code register between TDI and TDO. The ID code register contains the fixed ID code value for the device.

JTAG Software

The ÉlanSC300 microcontroller uses combined bidirectional cells. The total number of shifts required to load the ÉlanSC300 Boundary Scan Register is 173.

The following table shows the relative position of all the ÉlanSC300 JTAG cells. Note that:

- The chain starts at PMC2 (pin 77) connected to TDI.
- The chain ends at 8042CS (pin 75) connected to TDO.
- The control cells are located within the chain, their relative position being indicated in the table.
- The MUXed signals (TCK, TDI, TDO, and TMS) are not part of the cell chain.
- Control cells are active Low.
- Refer to Figure 10–22 of the IEEE 1149 standard.

Table 40. Boundary Scan (JTAG) Cells—Order and Type

Pin No.	Name	Cell Position	Cell Type	Notes
77	PMC2	1	output	
78	$\overline{RC}$	2	input	
79	A20GATE	3	input	
80	$\overline{AFDT}$	4	output	
82	PE	5	input	
83	$\overline{STRB}$	6	output	
84	$\overline{SLCTIN}$	7	output	
85	BUSY	8	input	
86	$\overline{ERROR}$	9	input	
87	SLCT	10	input	
88	$\overline{ACK}$	11	input	
89	$\overline{INIT}$	12	output	
90	$\overline{PPDWE}$	13	bidir	
91	$\overline{PPOEN}$	14	bidir	
92	$\overline{DTR}$	15	bidir	
93	$\overline{RTS}$	16	bidir	
94	SOUT	17	bidir	
96	$\overline{CTS}$	18	input	
97	$\overline{DSR}$	19	input	
98	$\overline{DCD}$	20	input	
99	SIN	21	input	
100	$\overline{RIN}$	22	input	
101	ACIN	23	input	
102	EXTSMI	24	input	
103	$\overline{SUS/RES}$	25	input	
*	*	26	control	Control cell for pins 106–155
106	$\overline{BL1}$	27	input	
107	$\overline{BL2}$	28	input	
108	$\overline{BL3}$	29	input	
109	$\overline{BL4}$	30	input	
110	$\overline{CD\_A}$	31	input	
111	RDY_A	32	input	
112	WP_A	33	input	
113	BVD2_A	34	input	
114	BVD1_A	35	input	
115	$\overline{WAIT\_AB}$	36	input	
116	$\overline{CD\_B}$	37	input	
117	RDY_B	38	input	
118	WP_B	39	input	
119	BVD2_B	40	input	
120	BVD1_B	41	input	
122	ICDIR	42	output	

Table 40. Boundary Scan (JTAG) Cells—Order and Type (Continued)

Pin No.	Name	Cell Position	Cell Type	Notes
123	MCEL_B	43	output	
124	MCEH_B	44	output	
125	VPP_B	45	output	
126	REG_B	46	output	
127	RST_B	47	output	
129	MCEL_A	48	output	
130	MCEH_A	49	output	
131	VPPA	50	output	
132	REG_A	51	output	
133	RST_A	52	output	
134	CA24	53	output	
136	CA25	54	output	
137	PMC0	55	output	
138	PMC1	56	output	
139	SPKR	57	output	
140	IORESET	58	input	
141	RESIN	59	input	
143	SBHE	60	output	
144	LCDD0	61	output	
145	LVDD	62	output	
146	DSCE	63	output	
147	DSOE	64	output	
148	DSMD0	65	bidir	
149	DSMA14	66	output	
150	DSMA13	67	output	
151	DSMA12	68	output	
152	DSMA11	69	output	
153	DSMA10	70	output	
154	DSMA9	71	output	
155	DSMA8	72	output	
*	*	73	control	Control cell for pins 158–200
158	DSMA7	74	output	
159	DSMA6	75	output	
160	DSMA5	76	output	
161	DSMA4	77	output	
162	DSMA3	78	output	
163	DSMA2	79	output	
164	DSMA1	80	bidir	
165	DSMA0	81	output	
166	DSMD1	82	bidir	
167	DSMD2	83	bidir	
168	DSMD3	84	bidir	
169	DSMD4	85	bidir	

Table 40. Boundary Scan (JTAG) Cells—Order and Type (Continued)

Pin No.	Name	Cell Position	Cell Type	Notes
170	DSMD5	86	bidir	
171	DSMD6	87	bidir	
172	DSMD7	88	bidir	
173	M	89	bidir	
174	LCDD3	90	bidir	
175	LCDD1	91	bidir	
177	LCDD2	92	bidir	
178	CP1	93	bidir	
179	CP2	94	bidir	
181	FRM	95	bidir	
182	$\overline{\text{LVEE}}$	96	bidir	
183	$\overline{\text{DSWE}}$	97	bidir	
184	PMC4	98	output	
185	PMC3	99	output	
186	PGP3	100	bidir	
187	PGP2	101	bidir	
188	PGP1	102	bidir	
189	PGP0	103	bidir	
190	$\overline{\text{LPH}}$	104	output	
191	IOCHRDY	105	input	
193	PIRQ(1)	106	input	
194	PIRQ(0)	107	input	
195	IRQ1	108	input	
196	$\overline{\text{IOCS16}}$	109	bidir	
197	$\overline{\text{MCS16}}$	110	bidir	
198	IRQ14	111	bidir	
200	CLK14_O	112	output	
*	*	113	control	Control cell for pins 2–51
2	$\overline{\text{RAS0}}$	114	output	
3	$\overline{\text{RAS1}}$	115	output	
4	$\overline{\text{CAS1L}}$	116	output	
5	$\overline{\text{CAS1H}}$	117	output	
6	$\overline{\text{CAS0L}}$	118	output	
7	$\overline{\text{CAS0H}}$	119	output	
8	$\overline{\text{MWE}}$	120	output	
10	MA10	121	output	
11	MA9	122	output	
13	MA8	123	output	
14	MA7	124	output	
15	MA6	125	output	
16	MA5	126	output	
17	MA4	127	output	
18	MA3	128	output	

Table 40. Boundary Scan (JTAG) Cells—Order and Type (Continued)

Pin No.	Name	Cell Position	Cell Type	Notes
19	MA2	129	output	
21	MA1	130	output	
24	MA0	131	output	
25	D15	132	bidir	
26	D14	133	bidir	
27	D13	134	bidir	
28	D12	135	bidir	
29	D11	136	bidir	
30	D10	137	bidir	
31	D9	138	bidir	
32	D8	139	bidir	
34	D7	140	bidir	
36	D6	141	bidir	
37	D5	142	bidir	
38	D4	143	bidir	
39	D3	144	bidir	
40	D2	145	bidir	
41	D1	146	bidir	
42	D0	147	bidir	
43	$\overline{\text{DOSCS}}$	148	output	
44	$\overline{\text{ROMCS}}$	149	output	
45	SYSCLK	150	bidir	
46	$\overline{\text{DACK2}}$		*	This pin becomes TCK when JTAGEN is High.
47	AEN		*	This pin becomes TDI when JTAGEN is High.
49	TC		*	This pin becomes TMS when JTAGEN is High.
50	ENDIRL	151	output	
51	ENDIRH	152	output	
*	*	153	control	Control cell for pins 54–103
54	$\overline{\text{IOR}}$	154	output	
55	$\overline{\text{IOW}}$	155	output	
56	$\overline{\text{MEMR}}$	156	output	
57	$\overline{\text{MEMW}}$	157	output	
58	RSTDRV	158	output	
59	$\overline{\text{DBUFOE}}$	159	output	
60	SA12	160	output	
61	SA11	161	output	
62	SA10	162	output	
63	SA9	163	output	
64	SA8	164	output	
66	SA7	165	output	
67	SA6	166	output	
69	SA5	167	output	
70	SA4	168	output	

Table 40. Boundary Scan (JTAG) Cells—Order and Type (Continued)

Pin No.	Name	Cell Position	Cell Type	Notes
71	SA3	169	output	
72	SA2	170	output	
73	SA1	171	output	
74	SA0	172	output	
75	$\overline{8042CS}$	173	bidir	
76	DRQ2		*	This pin becomes TDO when JTAGEN is High.

JTAG Instruction Opcodes

Table 41 lists the ÉlanSC300 microcontroller's public JTAG instruction opcodes. Note that the JTAG Instruction Register is 4 bits wide.

Table 41. ÉlanSC300 Microcontroller JTAG Instruction Opcodes

Instruction	Opcode
EXTEST	0000
BYPASS	1111
SAMPLE/PRELOAD	0001
IDCODE	0010
HI-Z	0011

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature Under Bias ... −65°C to +125°C

Supply Voltage V_{CC} with Respect to V_{SS} .....−0.5 V to +7 V

Voltage on Other Pins.....−0.5 V to (V_{CC}+0.5 V)

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Operating ranges define those limits between which the functionality of the device is guaranteed.

Table 42. DC Characteristics over Commercial and Industrial Operating Ranges (Plastic Shrink Quad Flat Pack (QFP), 33 MHz, 3.3 V)

VCCIO = 3.0 V – 3.6 V; $T_{AMBIENT}$ = 0°C to +70°C (commercial); T_{CASE} = -40° to +85°C (industrial)

Symbol	Parameter Description	Preliminary			Unit
		Min	Typ	Max	
f_{osc}	Frequency of Operation (internal CPU clock)	0		33	MHz
P_{CC}[2]	Supply Power—CPU clock = 33 MHz (VCCMEM=3.3 V)		582	778	mW
P_{CCSS}[2]	Suspend Power—CPU idle, all internal clocks stopped except 32.768 kHz		0.12		mW
$V_{OH(CMOS)}$	Output High Voltage $I_{OH(CMOS)}$ = –0.5 mA	VCC–0.45			V
$V_{OL(CMOS)}$	Output Low Voltage $I_{OL(CMOS)}$ = 0.5 mA			0.45	V
$V_{IH(CMOS)}$	Input High Voltage	2.0		VCC+0.3	V
$V_{IL(CMOS)}$	Input Low Voltage	–0.3		+0.8	V
I_{LI}	Input Leakage Current (0.1 V≤V_{OUT}≤VCC) (all pins except those with internal pull-up/pull-down resistors)			±10	µA
I_{IH}	Input Leakage Current V_{IH} = VCC – 0.1 V (all pins with internal pull-down resistors)			60	µA
I_{IL}	Input Leakage Current V_{IL} = 0.1 V (pins with internal pull-up resistors)			–60	µA
I_{LO}	Output Leakage Current (0.1 V≤V_{OUT}≤VCC)			±15	µA
C_{in}[3]	I/O Capacitance			15	pF
$AVCC_{RP-P}$	Analog V_{CC} ripple peak to peak			100	mV

Notes:

1. *Current out of a pin is given as a negative value.*
2. *VCC, VCC1, AVCC = 3.3 V and VCC5, VCCSYS, VCCSYS2 = 5.0 V.*
3. *Fc = 1 MHz.*

Table 43. DC Characteristics over Commercial and Industrial Operating Ranges (Plastic Shrink Quad Flat Pack (QFP), 33 MHz, 5 V)

VCCIO = 4.5 V – 5.5 V; $T_{AMBIENT}$ = 0°C to +70°C (commercial); T_{CASE} = -40° to +85°C (industrial)

Symbol	Parameter Description	Preliminary			Unit
		Min	Typ	Max	
f_{osc}	Frequency of Operation (internal CPU clock)	0		33	MHz
P_{CC}[2]	Supply Power—CPU clock = 33 MHz (VCCMEM=5 V)		660	862	mW
P_{CCSB}[2]	Suspend Power—CPU idle, all internal clocks stopped except 32.768 kHz		0.17		mW
$V_{OH(CMOS)}$	Output High Voltage $I_{OH(CMOS)} = -0.5$ mA	VCC–0.45			V
$V_{OL(CMOS)}$	Output Low Voltage $I_{OL(CMOS)} = 0.5$ mA			0.45	V
$V_{IH(CMOS)}$	Input High Voltage	2.0		VCC+0.3	V
$V_{IL(CMOS)}$	Input Low Voltage	–0.3		+0.8	V
I_{LI}	Input Leakage Current ($0.1-V \le V_{OUT} \le VCC$) (all pins except those with internal pull-up/pull-down resistors)			±10	µA
I_{IH}	Input Leakage Current $V_{IH} = VCC-0.1$ V (all pins with internal pull-down resistors)			90	µA
I_{IL}	Input Leakage Current $V_{IL} = 0.1$ V (pins with internal pull-up resistors)			–90	µA
I_{LO}	Output Leakage Current ($0.1-V \le V_{OUT} \le VCC$)			±15	µA
C_{in} (3)	I/O Capacitance			15	pF
$AVCC_{RP-P}$	Analog VCC ripple peak to peak (3.3 V only)			100	mV

Notes:

1. *Current out of a pin is given as a negative value.*
2. *VCC, VCC1, AVCC = 3.3 V and VCC5, VCCSYS, VCCSYS2 = 5 V.*
3. *Fc = 1 MHz.*

Table 44. Commercial and Industrial Operating Voltage Ranges at 25°

Power Pin Name	3.0 V–3.6 V	4.5 V–5.5 V
VCC[1]	√	N/A
VCC1	√	√
AVCC[1]	√	N/A
VCC5	√	√
VCCMEM	√	√
VCCSYS2	√	√

Notes:

1.VCC and AVCC are 3.3 V only.

THERMAL CHARACTERISTICS

The ÉlanSC300 microcontroller is specified for operation with a case temperature range from 0°C to 100°C for a commercial device. Table 45 shows the thermal resistance for 208-pin QFP and TQFP packages.

Table 45. Thermal Resistance (°C/Watt) ψ_{JT} and θ_{JA} for 208-pin QFP and TQFP packages

Package	ψ_{JT}	θ_{JA} vs. Airflow-Linear ft/min. (m/s)				
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
QFP	4.7	33	26	25	23	22
TQFP	7	37.4	31.0	28.5	26.9	26.6

TYPICAL POWER NUMBERS

Table 46 and Table 47 show the typical power numbers that were measured for the ÉlanSC300 microcontroller. These measurements reflect the part when it is configured for Maximum ISA and Internal CGA modes of operation at operating speeds of 33 MHz, 25 MHz, and 9.2 MHz. The connection of the various power sections of the part are outlined in the tables so that the designer may have some relative information for the power consumption differences between 3.3 V operation and 5 V operation. Please see the notes associated with the tables for specifics on the test conditions.

Table 46. Typical Maximum ISA Mode Power Consumption

Power Pin			Maximum ISA Mode					
Group	Name	Volts	33 MHz	25 MHz	9.2 MHz	Doze[2]	Suspend[3]	µ Pwr Off[4]
CPU Core	VCC	3.3	119 mA	94.3mA	39.1mA	6.12 mA	5.7 µA	4.1 µA
I/O VCC	VCC1	5	5.55 mA	5.55mA	5.55mA	5.55 mA	0 µA	OFF
Analog	AVCC	3.3	2.58 mA	2.36 mA	2.24 mA	1.39 mA	19.9 µA	19.8 µA
I/O	VCC5	5	772 µA	680 µA	434 µA	293 µA	0 µA	OFF
Memory	VCCMEM	3.3	16.4 mA	12.6 mA	4.9 mA	190 µA	10.5 µA	OFF
Sub ISA Bus	VCCSYS	5	16.8 mA	13.7 mA	7.76 mA	3.6 mA	0 µA	OFF
Full ISA Bus	VCCSYS2	5	2.06 mA	1.57 mA	0.9 mA	21 µA	0 µA	OFF
Total (mW)			582 mW	468mW	226mW	72.7 mW	0.12 mW	0.08 mW
Memory[5]	VCCMEM	5	26.5 mA	20.3 mA	8.75 mA	304 µA	17 µA	OFF
Total (mW)			660 mW	528 mW	470 mW	73.6 mW	0.17 mW	0.08 mW

See notes on page 83.

Table 47. Typical Internal LCD Mode Power Consumption

T_A= 70°C, $V_{OL_{TTL}}$ = 0.4 V, $V_{OH_{TTL}}$ = 2.4 V

Power Pin			Internal CGA Mode					
Group	**Name**	**Volts**	**33 MHz**	**25 MHz**	**9.2 MHz**	**Doze[2]**	**Suspend[3]**	**μ Pwr Off[4]**
CPU Core	VCC	3.3	121 mA	95.2 mA	40.1 mA	6.24 mA	5.5 μA	4.1 μA
I/O VCC	VCC1	5	14.8 mA	14.8 mA	14.8 mA	14.7 mA	0 μA	OFF
Analog	AVCC	3.3	2.62 mA	2.4 mA	2.24 mA	1.4 mA	19.9 μA	19.8 μA
I/O	VCC5	5	867 μA	765 μA	562 μA	448 μA	0 μA	OFF
Memory	VCCMEM	3.3	17 mA	13 mA	4.9 mA	182 μA	11.3 μA	OFF
Sub ISA Bus	VCCSYS	5	18.9 mA	15.3 mA	8.1 mA	3.85 mA	0 μA	OFF
Full ISA Bus	VCCSYS2	5	3.88 mA	3.86 mA	3.82 mA	3.79 mA	0 μA	OFF
Total (mW)			656 mW	539 mW	292 mW	140 mW	0.12 mW	0.08 mW
Memory [5]	VCCMEM	5	26.8 mA	20.4 mA	7.6 mA	300 μA	17.6 μA	OFF
Total (mW)			734 mW	598 mW	314 mW	141 mW	0.17 mW	0.08 mW

Notes:

All measurements were obtained at typical room temperature (ambient).

1. *In normal operating mode measurements, the ÉlanSC300 microcontroller is running the LandMark Speedcom benchmark (Version 2.00). All CPU idle cycles are run at the high-speed rate.*
2. *In Doze mode, the Doze mode configuration is such that the low-speed CPU clock is programmed to turn on for 64 refresh cycles upon an IRQ0 (DOS timer) generation. After 64 refresh cycles, the low-speed CPU clock is turned off again. The IRQ0 timer is set for an approximate 55 ms interval and the refresh duty cycle is approximately 15.6 μs. In Doze mode, the high-speed PLL is always turned off and, in this case, the low-speed PLL and video PLLs are on to allow the IRQ0 periodic wake-up.*
3. *Suspend mode measurements were taken with DRAM refresh rate set at 8192 Hz (126 μs).*
4. *Micropower measurements were taken with DRAM unpowered and the DRAM refresh rate set at 8192 Hz.*
5. *These measurements were taken with the memory interface powered at 5 V, rather than 3.3 V.*

DERATING CURVES

This section describes how to use the derating curves on the following pages in order to determine potential specified timing variations based on system capacitive loading. The pin characteristics tables in this document (see page 24) have a column called “Spec. Load.” This column describes the specification load presented to the specific pin when testing was performed to generate the timing specification documented in “AC Switching characteristics and Waveforms” on page 98.

For example, to find out the effect of capacitive loading on a DRAM specification such as $\overline{\text{MWE}}$ hold from $\overline{\text{CAS}}$ Low, first find the specification load for $\overline{\text{MWE}}$ from the pin characteristics table. The value here is 70 pF. Note the output drive type is D. Also, assume that the system DRAM interface is 3.3 V and our system load on the ÉlanSC300 microcontroller’s $\overline{\text{MWE}}$ pin is 90 pF.

Referring to Figure 13, 3.3 V I/O Drive Type D Rise Time, a time value of approximately 9.8 ns corresponds to a capacitive load of 70 pF.

Also referring to Figure 13, a time value of approximately 12.3 ns corresponds to a capacitive load of 90 pF. Subtracting 9.8 ns from the 12.3 ns, it can be seen that the rise time on the $\overline{\text{MWE}}$ signal will increase by 2.5 ns. Therefore, the $\overline{\text{MWE}}$ hold from $\overline{\text{CAS}}$ Low (min) parameter will increase from 15 ns to 17.5 ns (15 ns + 2.5 ns).

If the capacitive load on $\overline{\text{MWE}}$ was less than 70 pF, the time given in the derating curve for the load would be subtracted from the time given for the specification load. This difference can then be subtracted from the $\overline{\text{MWE}}$ hold from $\overline{\text{CAS}}$ Low (min) parameter (ISNS) to determine the derated AC Timing parameter.

Table 48. I/O Drive Type Description (Worst Case)

T_A= 70°C, $V_{OL_{TTL}}$ = 0.4 V, $V_{OH_{TTL}}$ = 2.4 V

I/O Drive Type	VCCIO (V)	IOL_{TTL} (mA)	IOH_{TTL} (mA)[1]
A	3.0 4.5	2.6 3.7	–3.5 –13.9
B	3.0 4.5	5.1 7.3	–5.2 –20.7
C	3.0 4.5	7.7 10.8	–8.6 –34.2
D	3.0 4.5	7.7 10.8	–10.3 –40.8
E	3.0 4.5	10.2 14.1	–13.6 –53.9

Notes:

1. Current out of pin is given as a negative value.

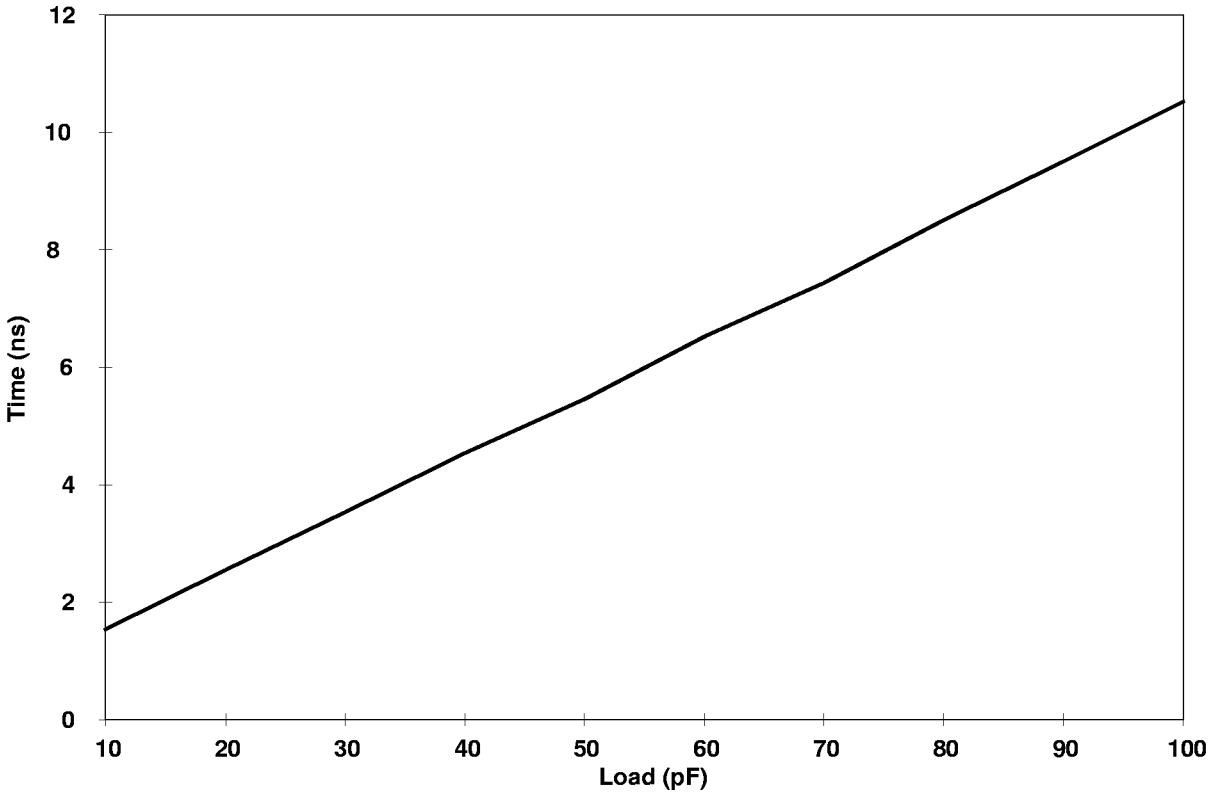


Figure 9. 3.3-V I/O Drive Type E Rise Time

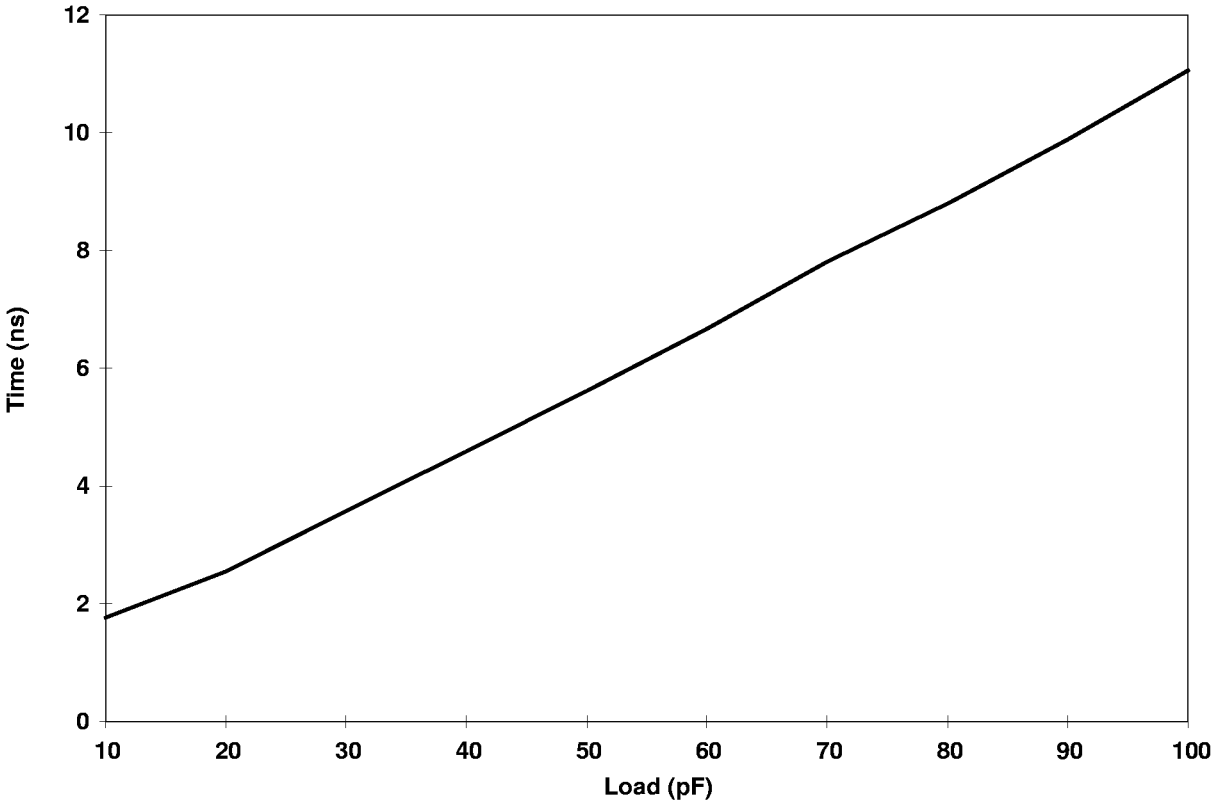


Figure 10. 3.3-V I/O Drive Type E Fall Time

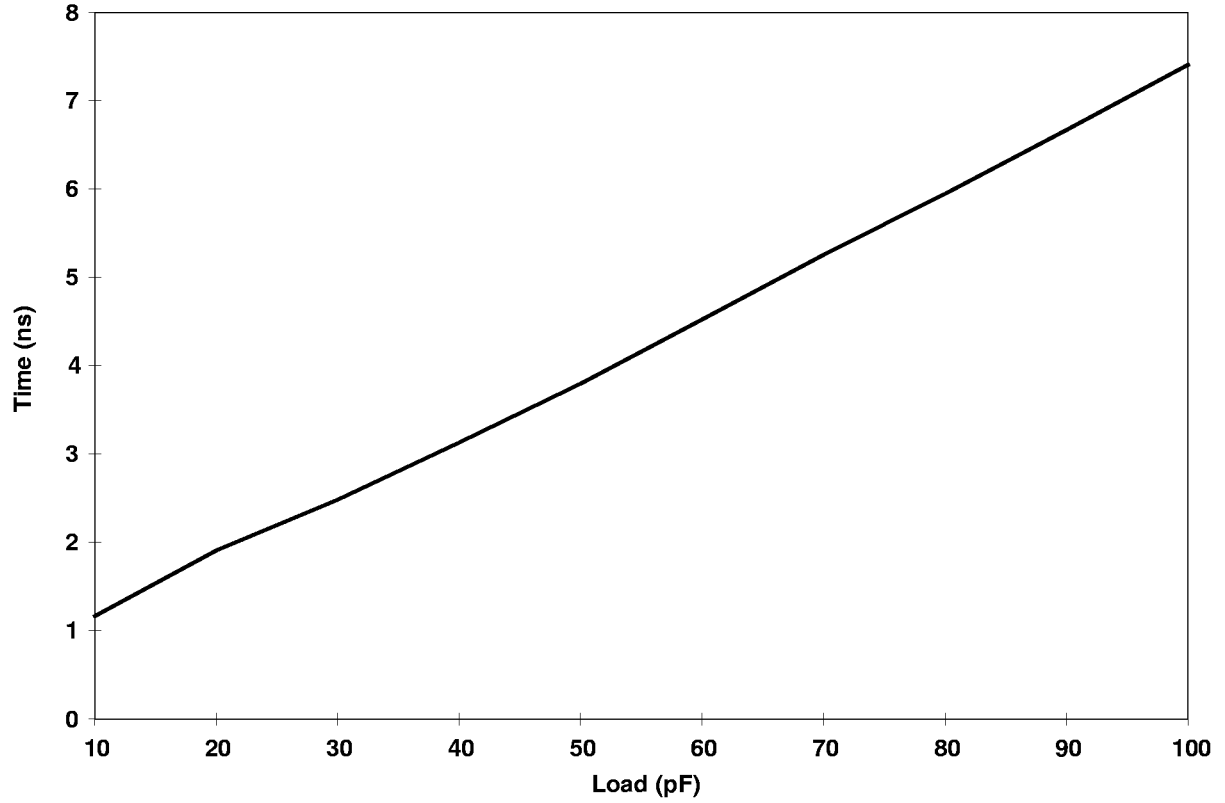


Figure 11. 5-V I/O Drive Type E Rise Time

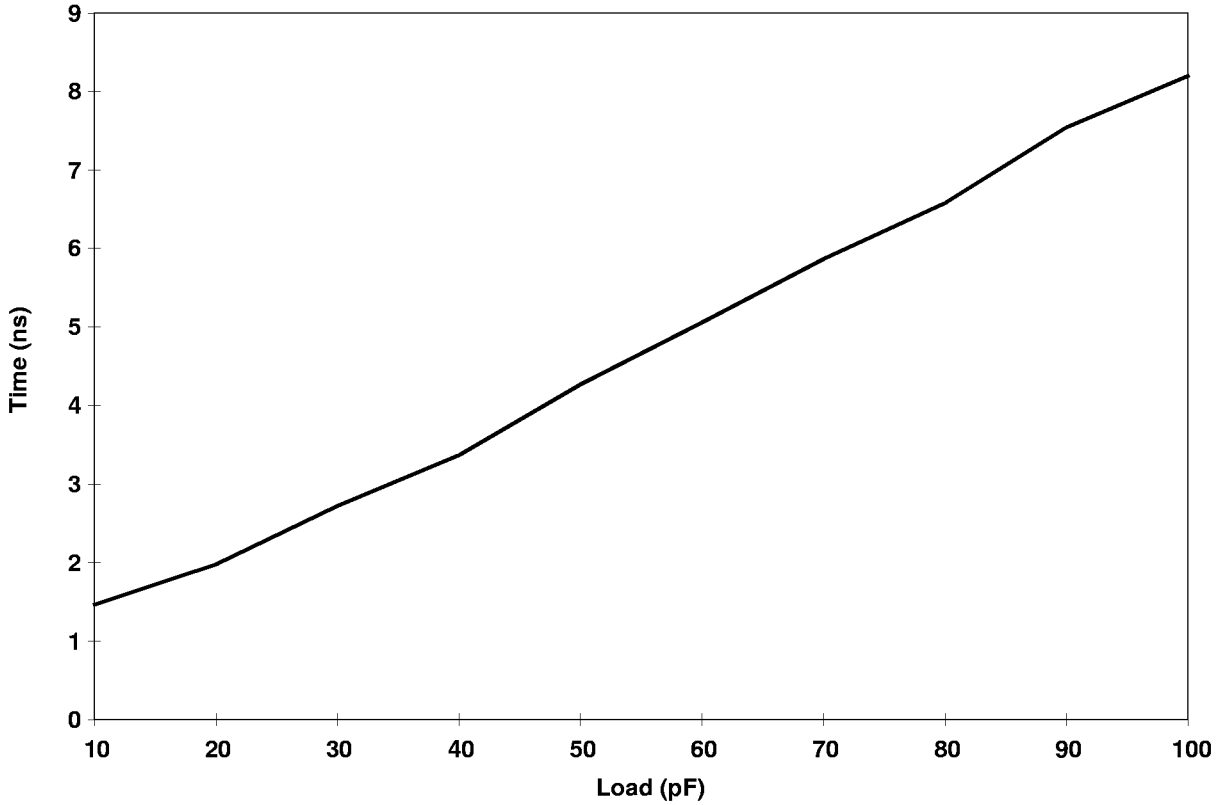


Figure 12. 5-V I/O Drive Type E Fall Time

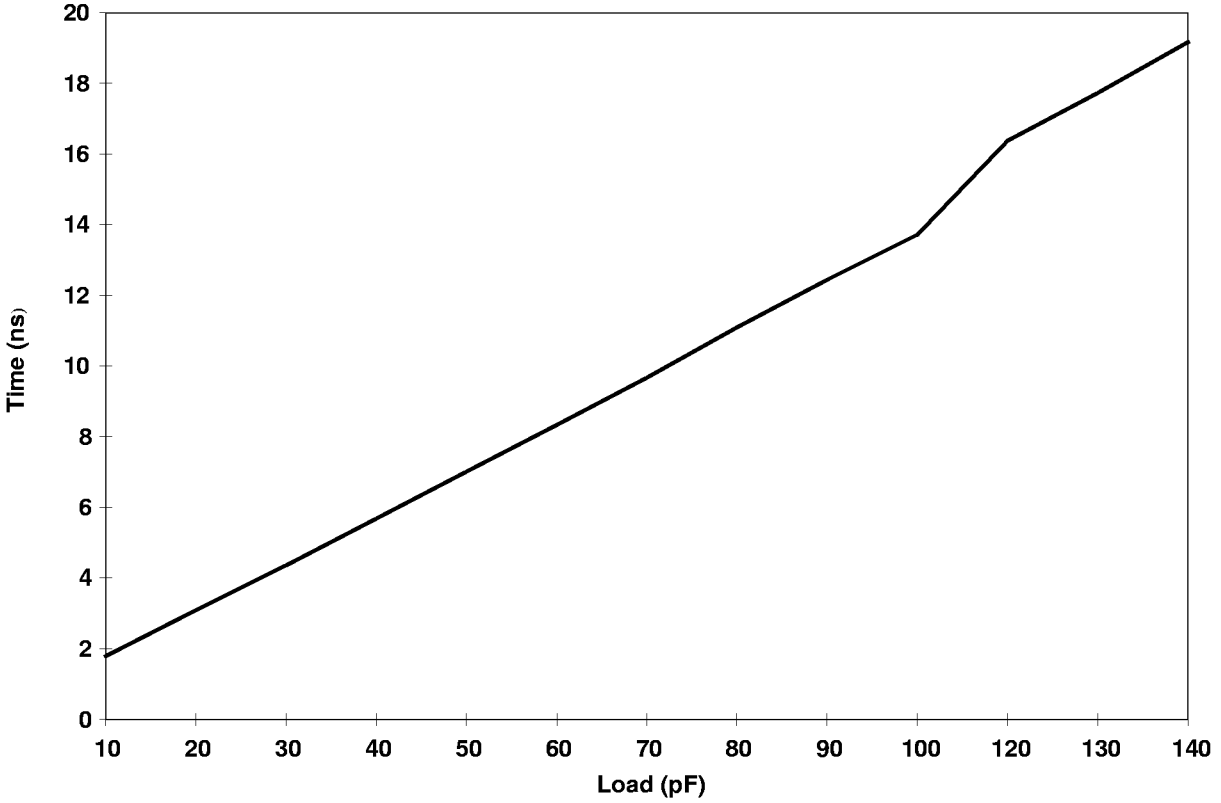


Figure 13. 3.3-V I/O Drive Type D Rise Time

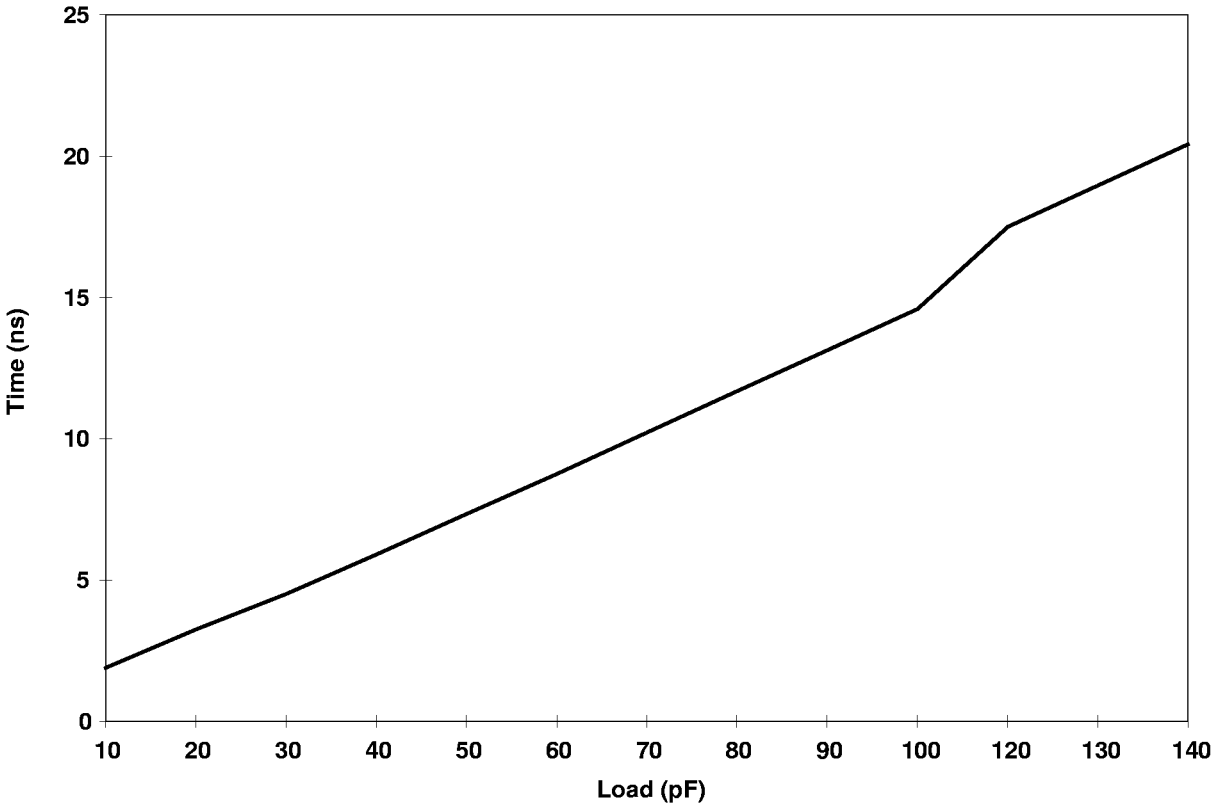


Figure 14. 3.3-V I/O Drive Type D Fall Time

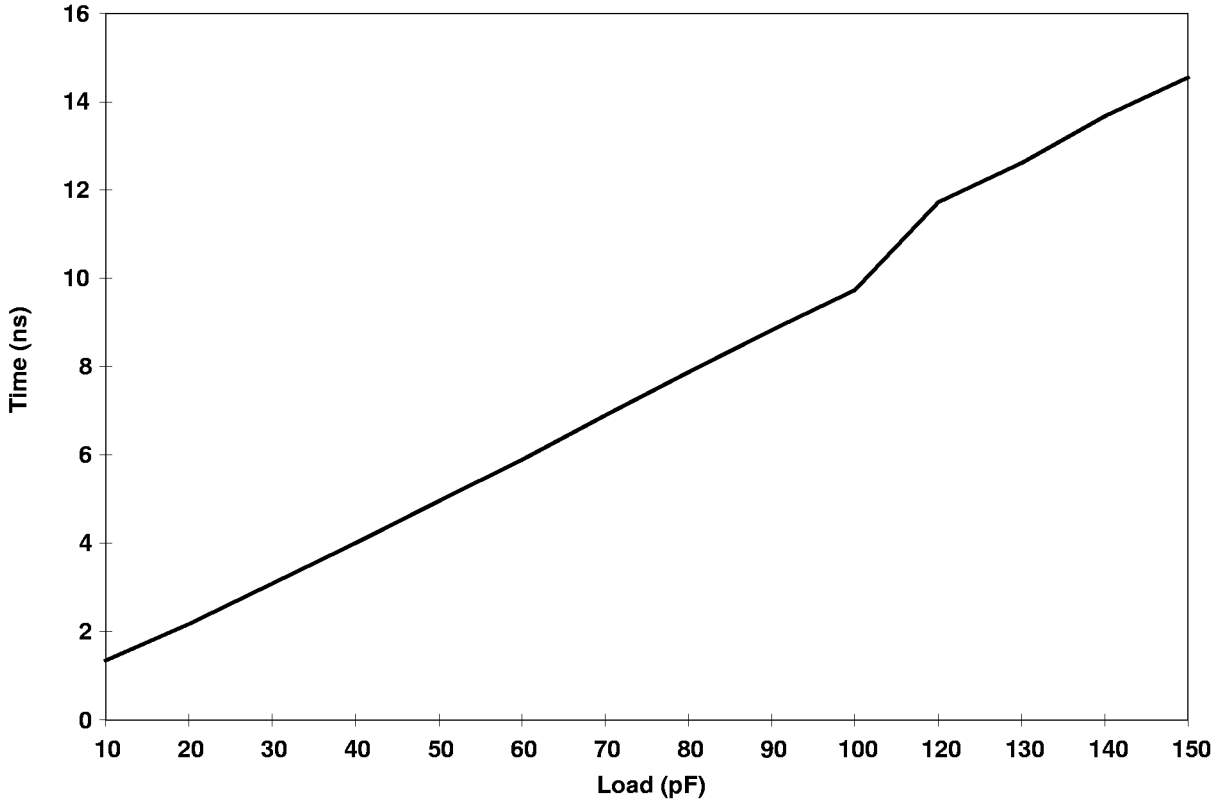


Figure 15. 5-V I/O Drive Type D Rise Time

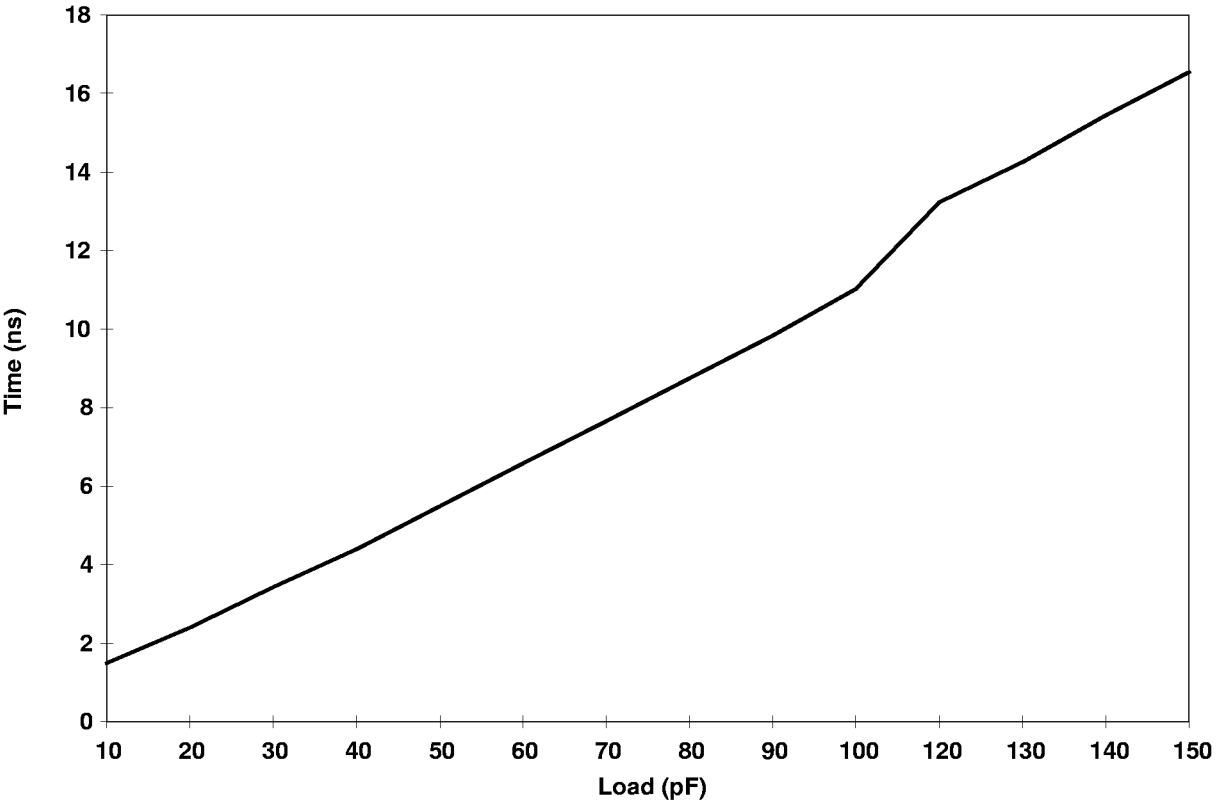


Figure 16. 5-V I/O Drive Type D Fall Time

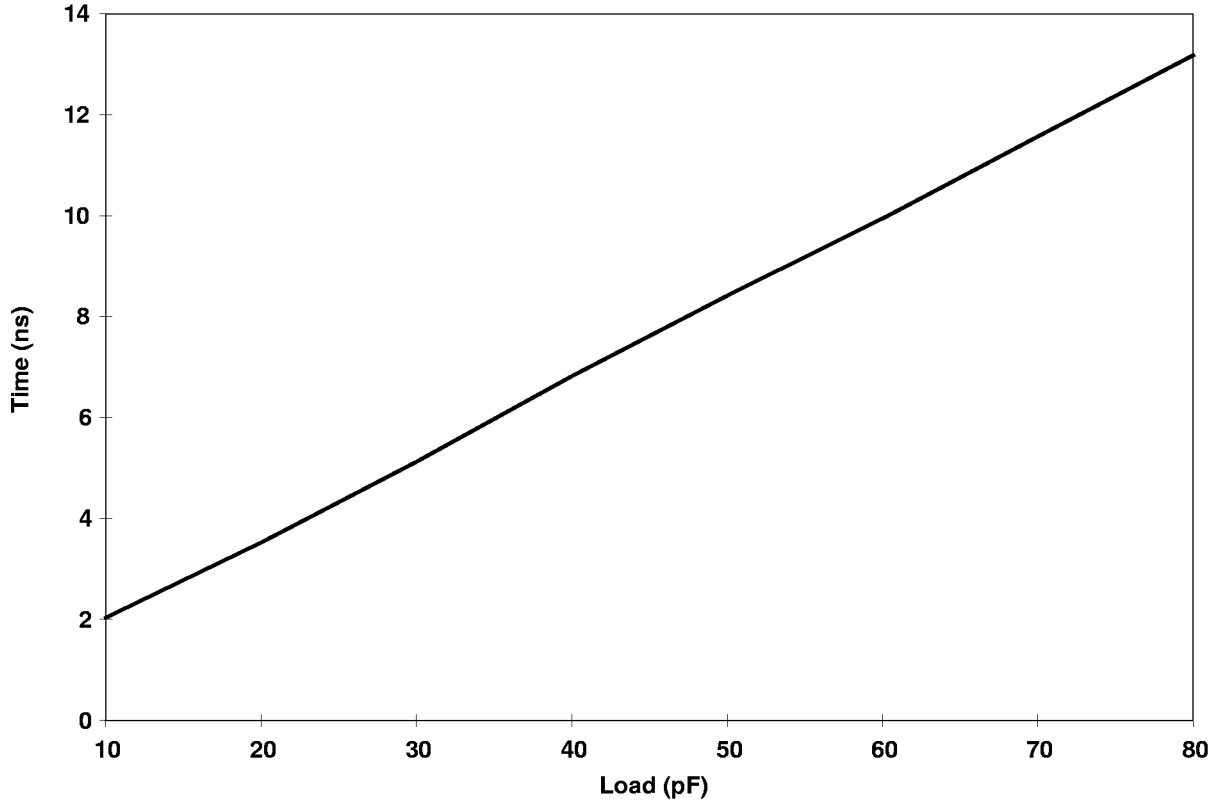


Figure 17. 3.3-V I/O Drive Type C Rise Time

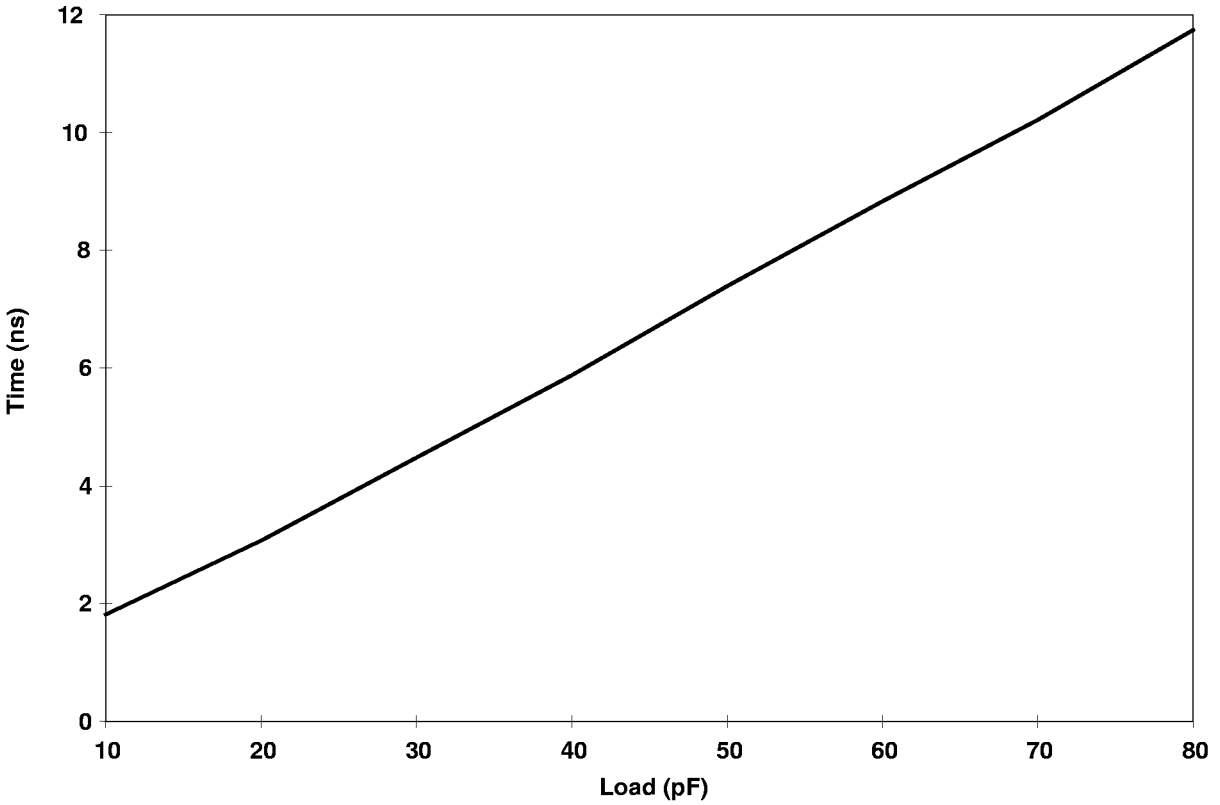


Figure 18. 3.3-V I/O Drive Type C Fall Time

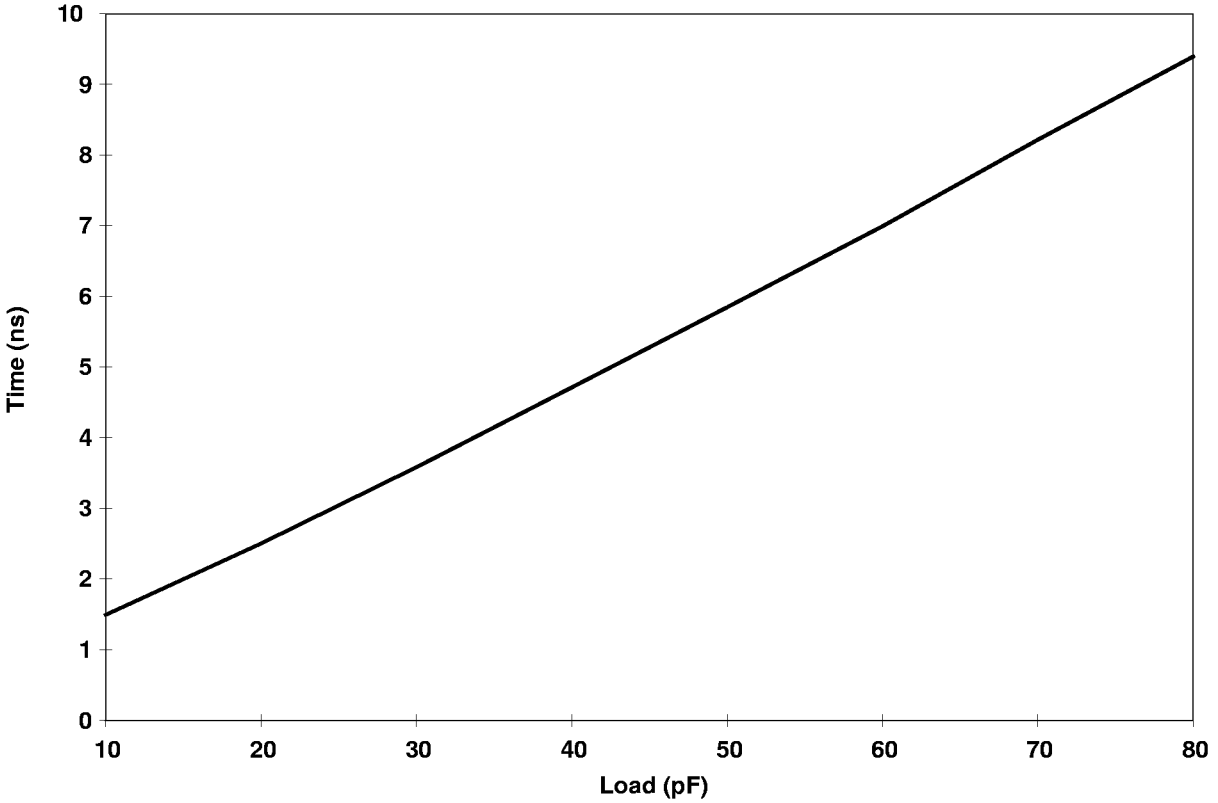


Figure 19. 5-V I/O Drive Type C Rise Time

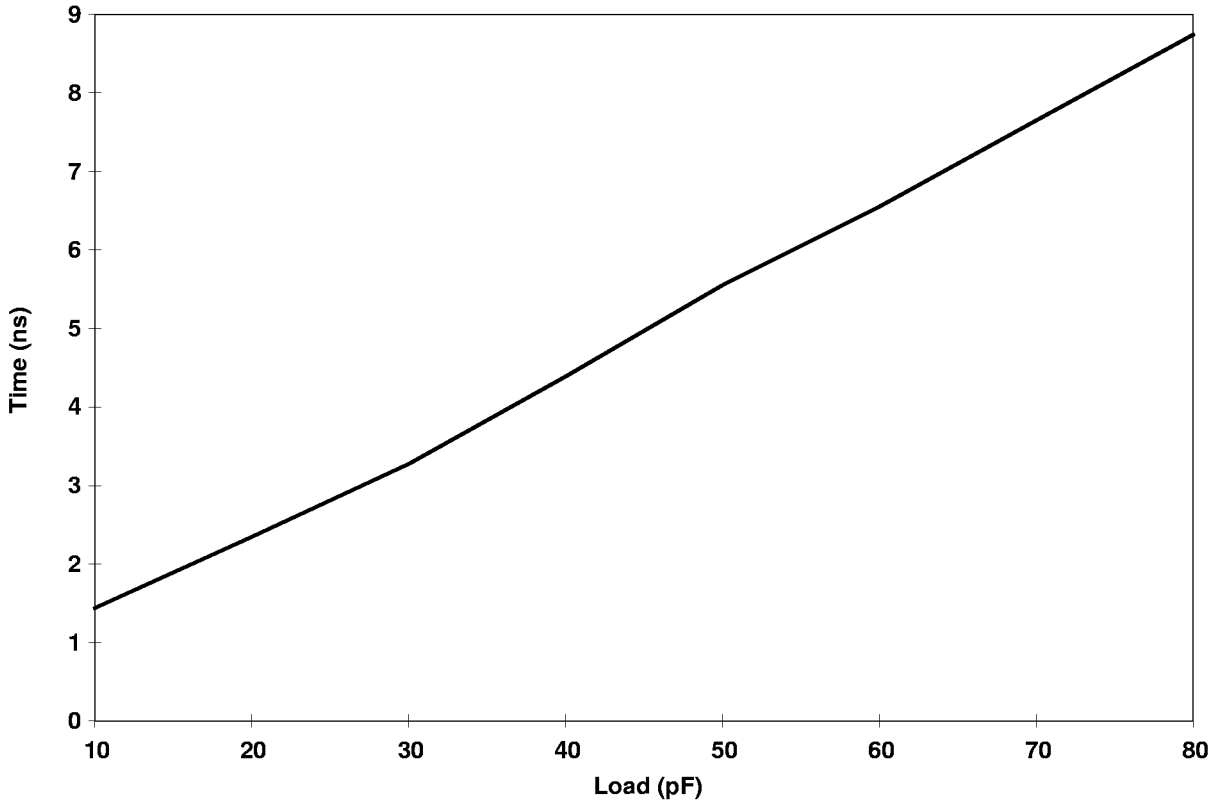


Figure 20. 5-V I/O Drive Type C Fall Time

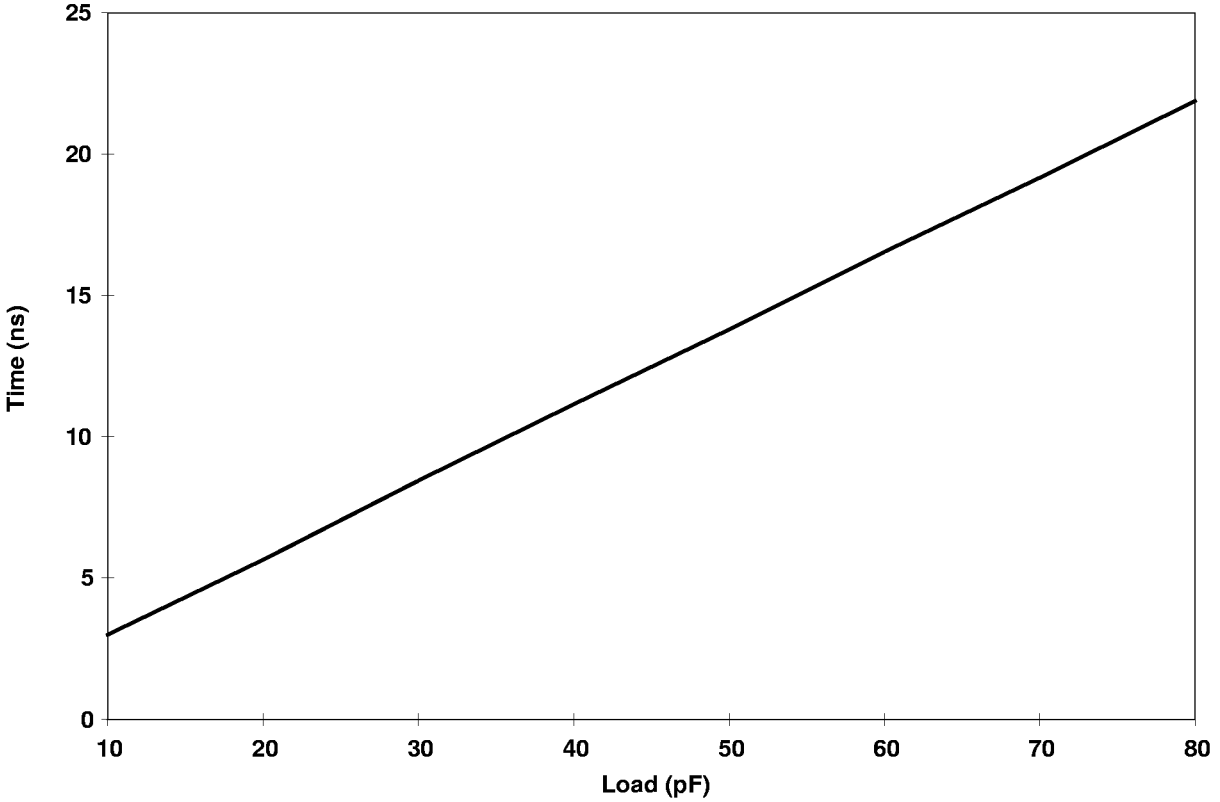


Figure 21. 3.3-V I/O Drive Type B Rise Time

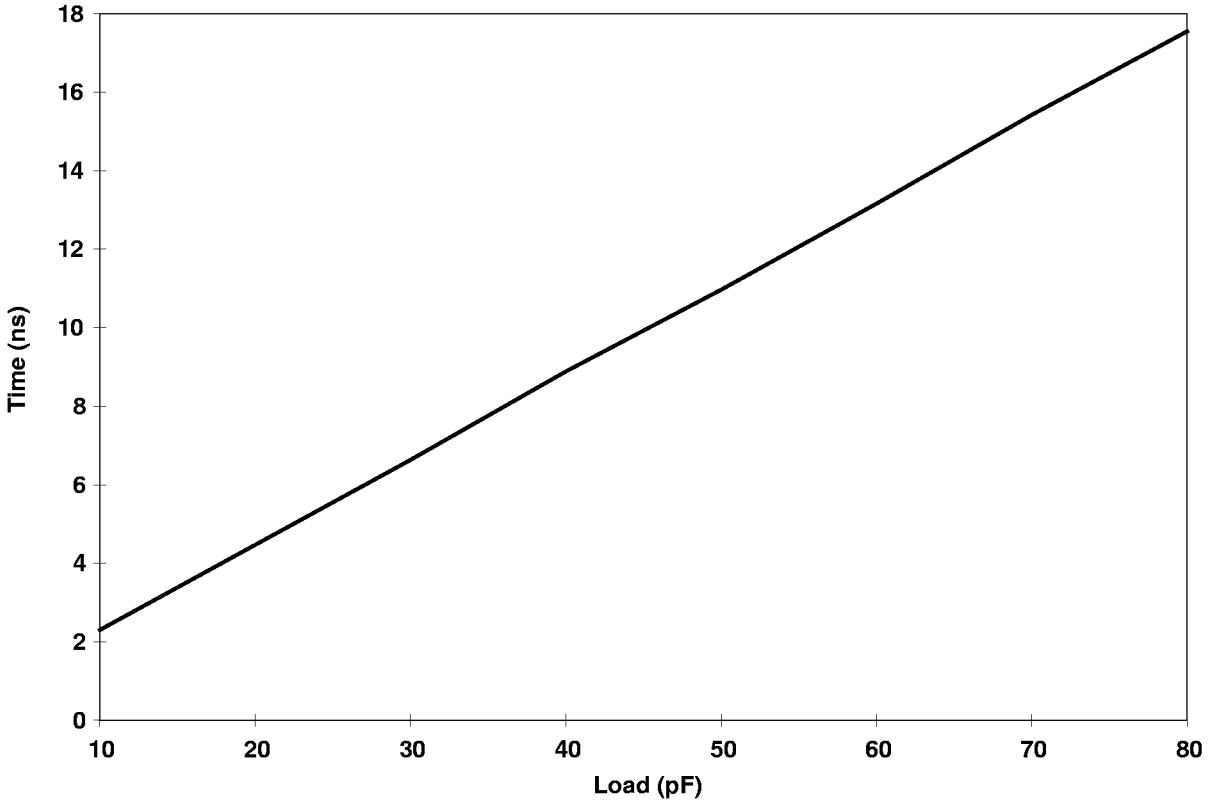


Figure 22. 3.3-V I/O Drive Type B Fall Time

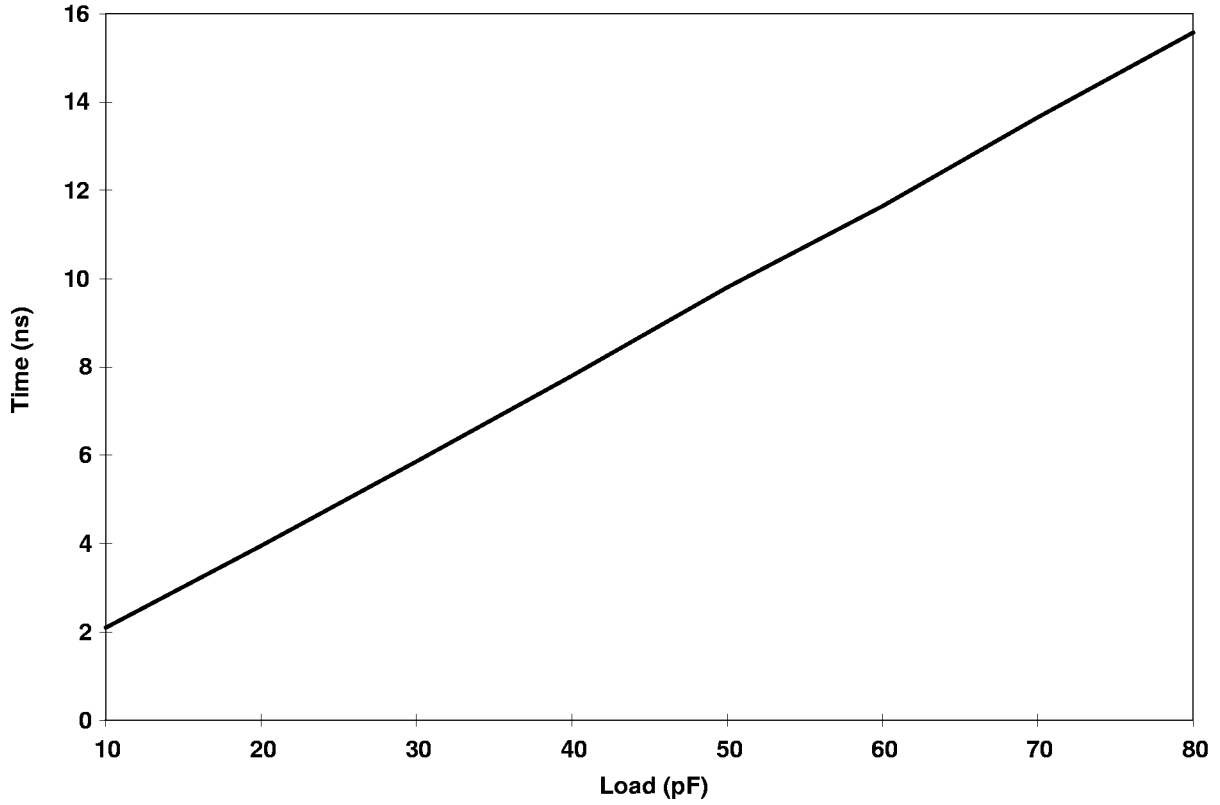


Figure 23. 5-V I/O Drive Type B Rise Time

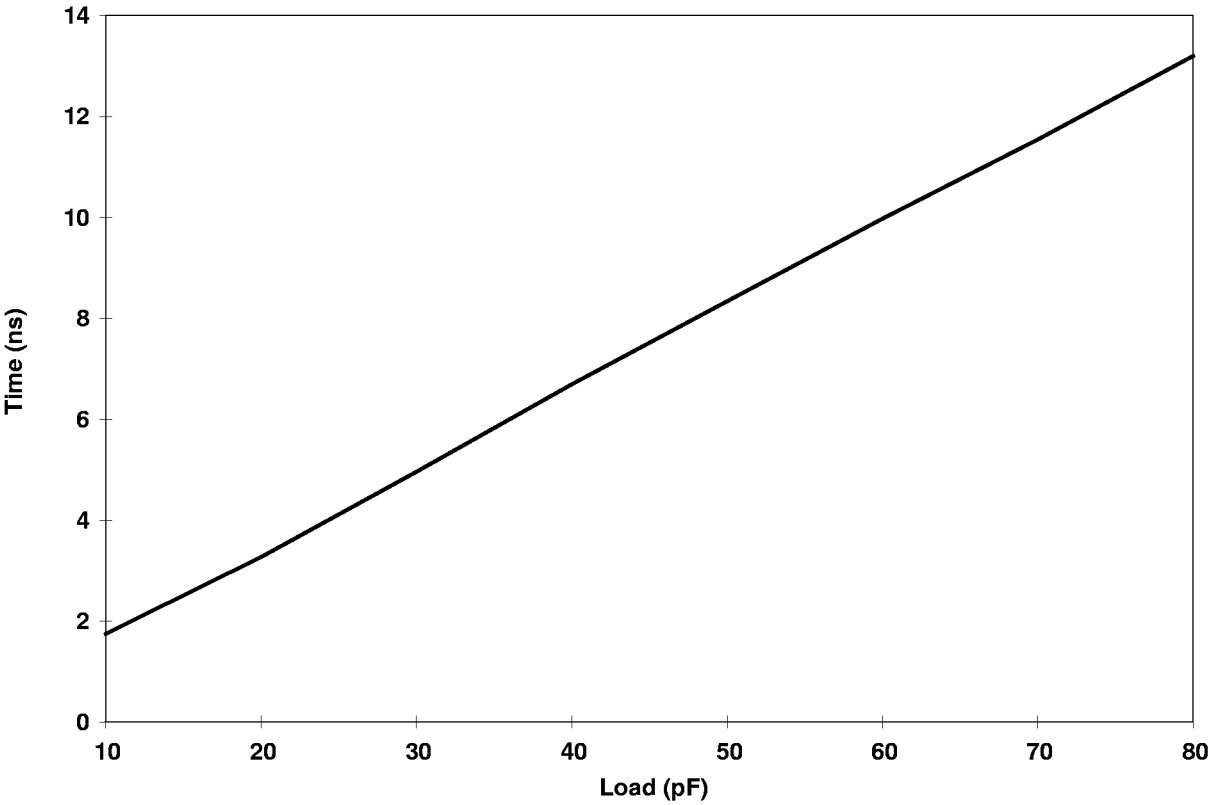


Figure 24. 5-V I/O Drive Type B Fall Time

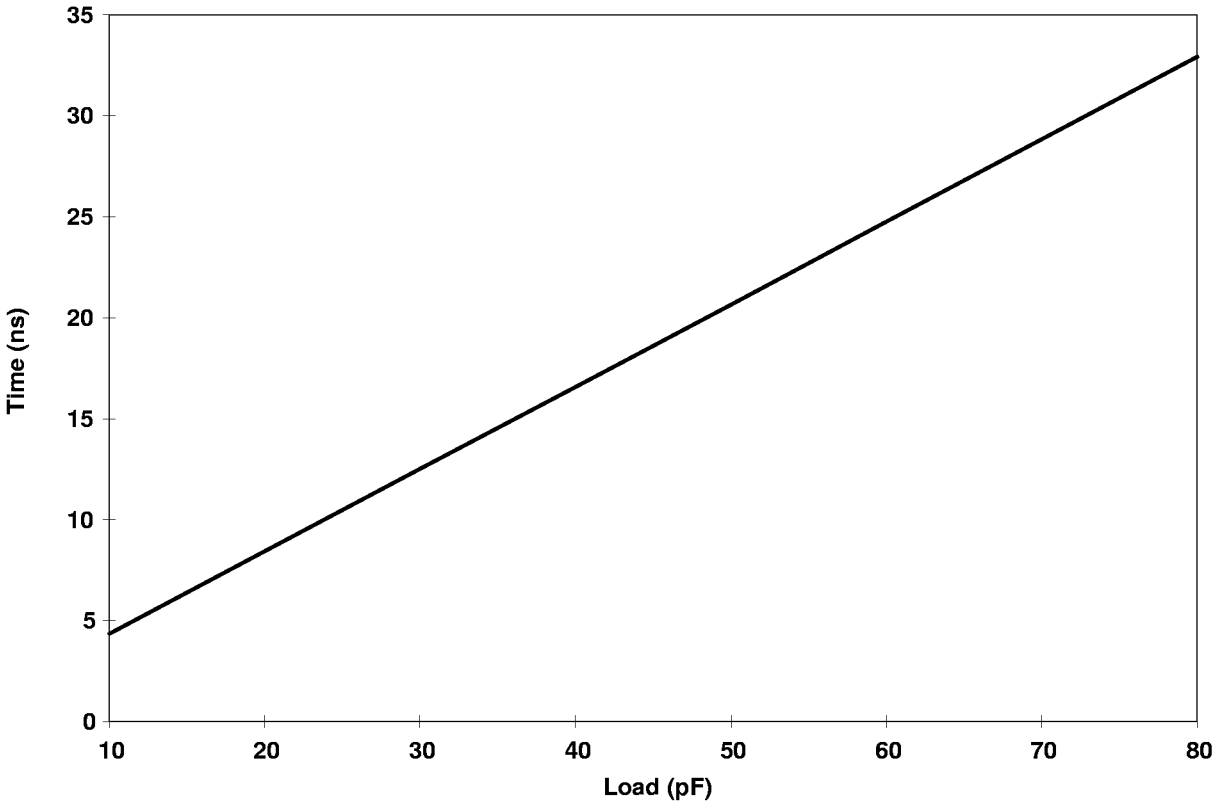


Figure 25. 3.3-V I/O Drive Type A Rise Time

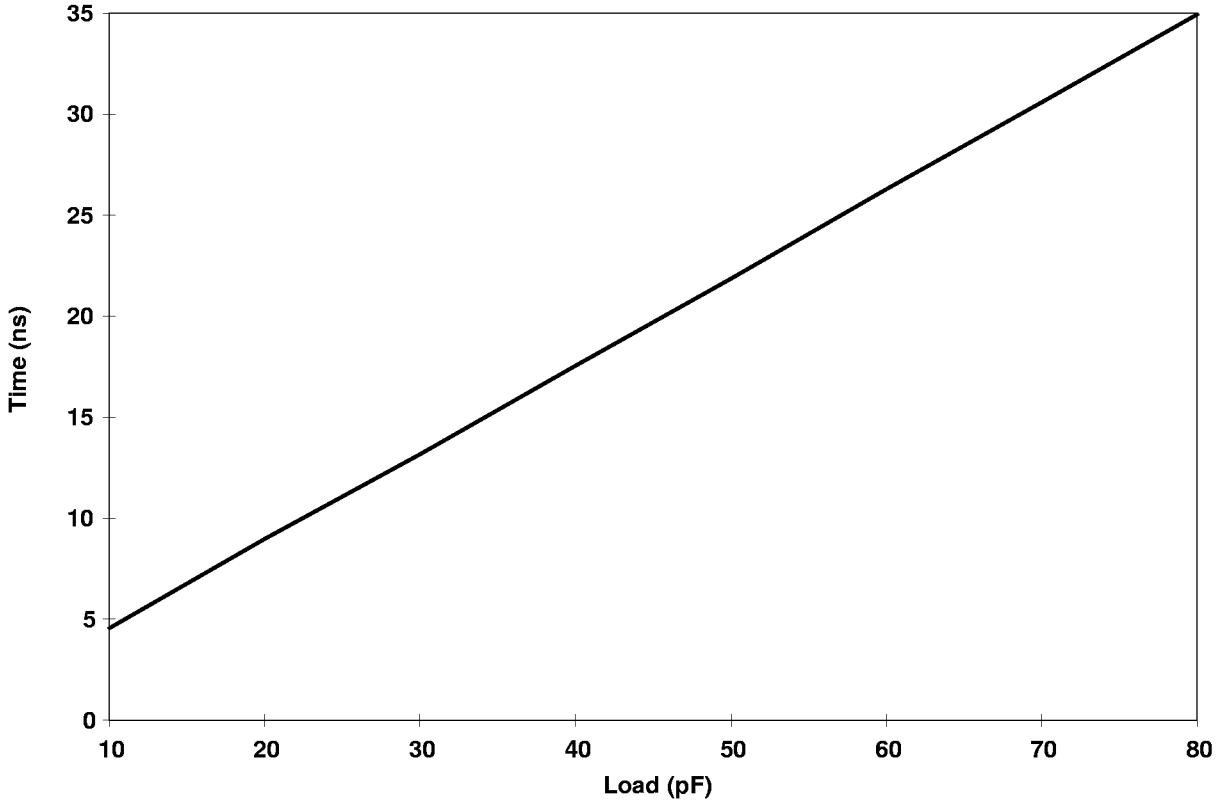


Figure 26. 3.3-V I/O Drive Type A Fall Time

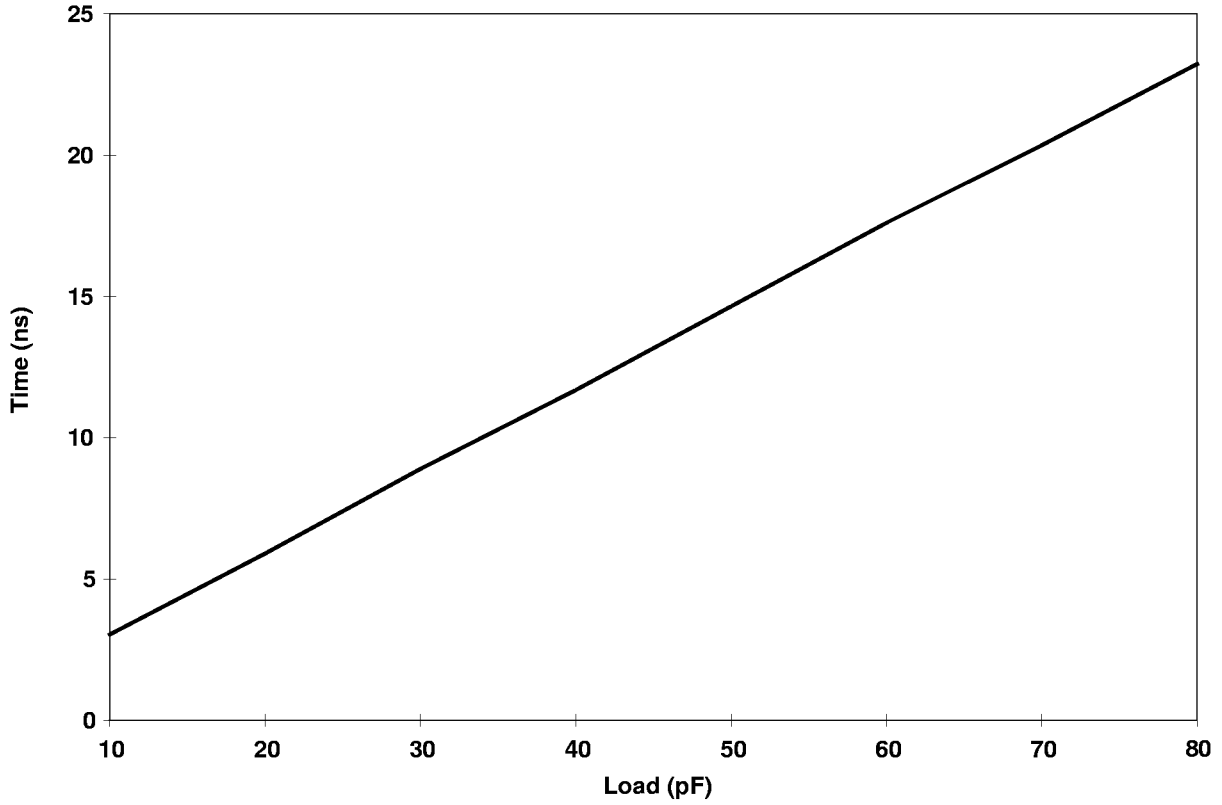


Figure 27. 5-V I/O Drive Type A Rise Time

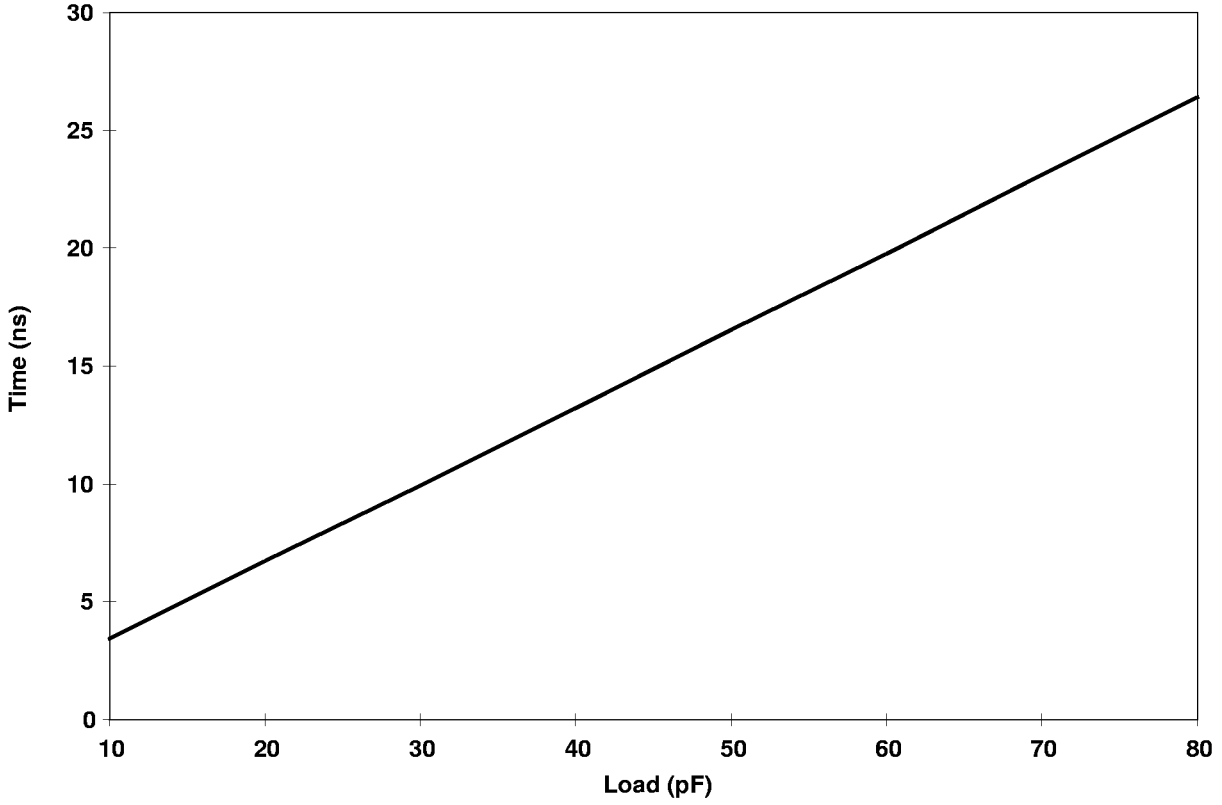


Figure 28. 5-V I/O Drive Type A Fall Time

VOLTAGE PARTITIONING

The ÉlanSC300 microcontroller supports both 3.3-V system designs and mixed 3.3-V and 5-V system designs. For 3.3-V-only operation, all supply pins (VCC, VCC1, VCC5, VMEM, VSYS, VSYS2, and AVCC) should be connected to the 3.3-V DC supply. To operate an interface at 5 V, the VCCIO pins associated with that I/O interface should be connected to 5 V. All supply pins of the same name should be connected to the same voltage plane. The different supply pins and their functions are described in this section.

Refer to the Pin Characteristics section beginning on page 24 of this data sheet for the internal VCC rail (VCCIO and VCC Clamp) to which each pin is electrically attached.

For more details about the information in this section, see the commercial and industrial operating voltage ranges beginning on page 80. Also see Table 51 on page 99 and its corresponding notes.

"Typical Power Numbers" on page 82 details the power consumption of each of these supply pins in Maximum ISA mode or Internal LCD mode.

VCC — These supply pins are used to provide power to the ÉlanSC300 microcontroller core only. They should always be connected to a 3.3-V source.

VCC1 — This supply pin provides power to a subset of the LCD/alternate, power management, and ISA interface pins. It can be connected to either a 3.3-V or 5-V source, depending on the logic threshold requirements of the external peripherals attached to these interfaces. When connected to the 5-V supply, all outputs with VCC1 as their VCCIO will be 5 V. If connected to 3.3 V, all of these outputs will be 3.3 V.

VCC5 — These supply pins are used to provide a 5-V source for the 5-V input and output pins. If the system design requires that the ÉlanSC300 microcontroller support 5-V tolerant inputs, then this pin should be connected to a 5-V DC source. This supply pin is the VCCIO for the Parallel Port, Serial Port, and PCMCIA interfaces.

VMEM — This supply pin controls the operating voltage of the memory interface. When connected to the 5-V supply, all outputs to the main memory will be 5 V. This includes the ÉlanSC300 microcontroller data bus. Therefore, translation buffers may be required when interfacing to 5-V devices on the data bus when the memory interface is operating at 3.3 V.

VSYS — These supply pins provide power to a subset of the ISA address and command signal pins, external memory chip selects, buffer direction controls, and other miscellaneous functions. They can be required to operate at 3.3 V or 5 V, depending on the system design.

VSYS2 — This supply pin controls the operating voltage for some of the LCD/alternate function pins. This voltage pin should be connected to either 3.3 V or 5 V, depending on the type of bus option selected, the voltage threshold requirements of attached devices, and the state of the other voltage pins associated with the LCD/alternate function interface pins (i.e., VCC1 and VSYS).

AVCC — This supply pin provides power to the analog section of the ÉlanSC300 microcontroller. It should always be connected to a low-noise 3.3-V supply. For more information, see the DC characteristics specifications, beginning on page 80.

CRYSTAL SPECIFICATIONS

The ÉlanSC300 microcontroller on-chip oscillator is the primary clock source driving all of the on-chip PLL clock generators and the real-time clock (RTC) function directly.

For problems with crystal startup, check that the specifications listed in this section are met, and refer to the *Troubleshooting Guide for Micro Power Off Mode on Élan™SC300 and ÉlanSC310 Microcontrollers and Evaluation Boards Application Note*, order #21810.

Externally, a parallel resonant PC/AT cut crystal (32.768 kHz), two capacitors, and two resistors are required for the oscillator to function properly. It is critical that the frequency of the oscillator circuit be as close as possible to the nominal 32.768 kHz frequency for RTC accuracy. By selecting the appropriate external circuit components, this oscillator circuit can be made to operate at very close to the nominal 32.768 kHz.

Figure 29 shows the complete oscillator circuit, including the discrete component model for the crystal. In this figure, the external discrete components that must be supplied by the system designer are R_F, R_B, C_D, C_G, and XTAL. R_F is the external feedback resistor for the on-chip amplifier. R_B provides some isolation between the parasitic capacitance of the chip and the crystal. The value of this resistor also has a very small effect on the operating frequency of the circuit. C_D and C_G are the external load capacitors. The value of these capacitors, in conjunction with the other capacitive values discussed below, have the most affect on the operating frequency of this circuit.

The discrete components inside the dotted line represent the circuit model for the crystal, with C_O representing the crystal lead shunt capacitance. The dashed line component C_{STRAY} represents the stray capacitance of the printed circuit board. Typically, a crystal manufacturer provides values for all of the equivalent circuit

model components for a given crystal (i.e., L_1, C_1, R_1, and C_O). In addition to these parameters, the manufacturer will provide a load capacitance specification usually designated as C_L. The load capacitance specification is the capacitive load at which the manufacturer has tuned the crystal for the specified frequency. It is therefore required that the load capacitance in the oscillator circuit is duplicated as closely as possible to the manufacturer's load capacitance specification.

The crystal load capacitance in the circuit consists of the capacitor network C_O, C_{STRAY}, C_D, and C_G. This network reduces to (C_O + C_{STRAY}) in parallel with the series combination of C_D and C_G. Therefore, the desired series combination of C_D and C_G is equal to C_L – (C_O + C_{STRAY}), where C_L is the crystal manufacturer's load capacitance specification.

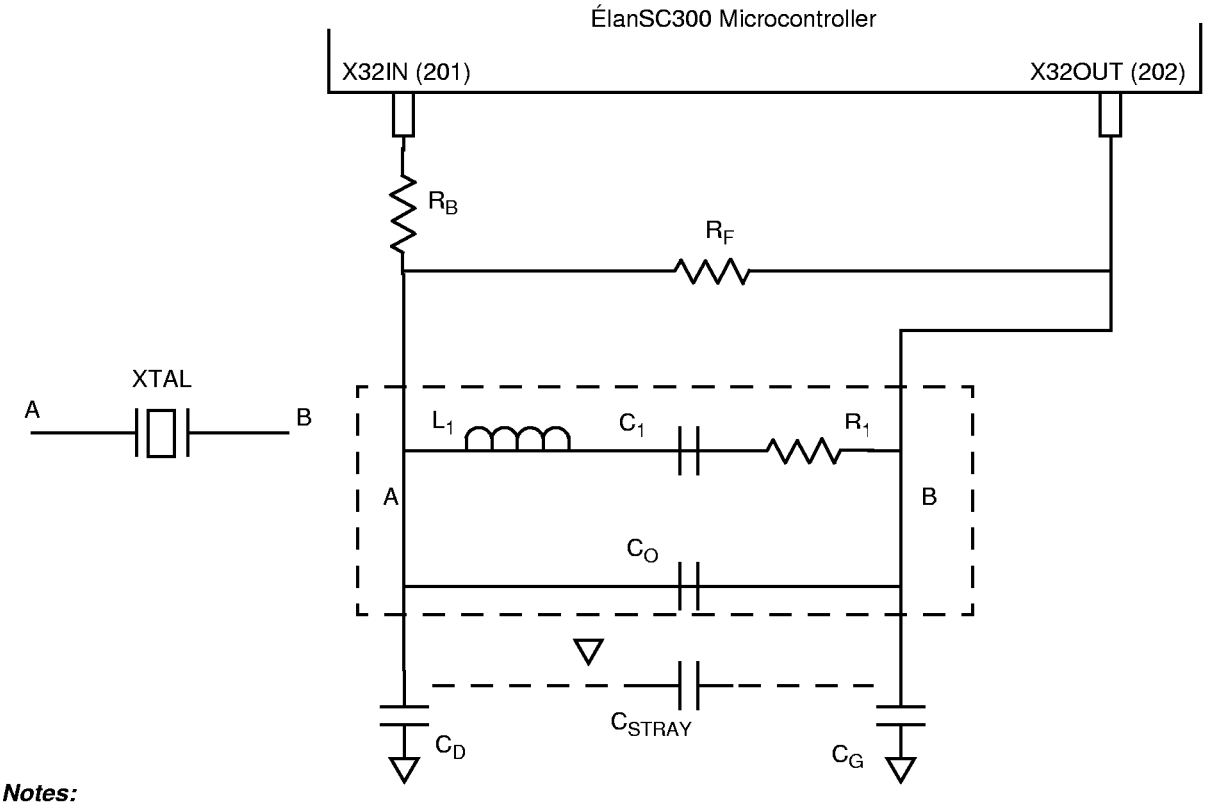
The series combination of C_D and C_G =

$$\left(\frac{(C_D \times C_G)}{(C_D + C_G)}\right)$$

C_{STRAY} is typically difficult to determine. Some value can be assumed and experimentation will determine the optimal value for C_D and C_G. In determining the external component values to provide the optimal operating frequency, there are some recommended limits to ensure a reasonable start-up time for the oscillator circuit. These limits are shown in Table 49.

Table 49. Recommended Oscillator Component Value Limits

	Minimum	Maximum
R_F	14 MΩ	18 MΩ
R_B	0 Ω	10 kΩ
C_D	10 pF	30 pF
C_G	10 pF	30 pF



Notes:

For board layout suggestions, refer to the ÉlanSC300 Microcontroller Evaluation Board User's Manual available in PDF format on the AMD web site.

Figure 29. X32 Oscillator Circuit

LOOP FILTERS

Each of the Phase-Locked Loops (PLLs) in the ÉlanSC300 microcontroller requires an external Loop Filter. Figure 30 describes each of the Loop Filters and the recommended component values. The recommended component values are shown in Table 50.

The system designer shall include the pads on the printed circuit board to accommodate the future installation/change of C2 and R1. This is recommended because the PLL performance can be affected by the physical circuit board design. In addition, future revisions of the ÉlanSC300 microcontroller with a modified PLL design may require the addition of these components to the system board.

The component value(s) of the Loop Filter directly affect the acquisition (start up) time of the PLL circuit. With the values recommended, the approximate acquisition time is 200 ms. Therefore, the system designer should program the Clock Control Register at Index 8Fh appropriately. Bits 0, 1, and 2 set the PLL restart delay time. When the PLLs are shut off for any reason (i.e., power management), the PLL will be allowed an amount of time equal to that programmed in this register to start up before the PLL outputs are enabled for the internal device logic. A PLL restart delay time of 256 ms should be set in the Clock Control Register.

The pulse width of the RSTDRV signal is adjustable based on the PLL start-up timing. See the timing specifications in Table 51 and Figure 32–Figure 35.

Table 10 on page 33 shows the pin characteristics for the Loop Filters, including the reset voltage level of each pin when $\overline{\text{RESIN}}$ is active.

For more information about Loop Filters, see the *Troubleshooting Guide for Micro Power Off Mode on the Élan™SC300 and ElanSC310 Microcontrollers and Evaluation Boards Application Note,* order #21810.

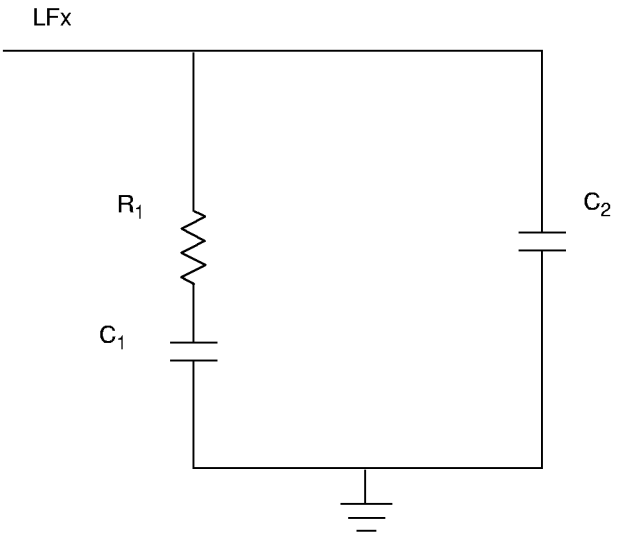


Figure 30. Loop-Filter Component

Table 50. Loop-Filter Component Values

LFx	R_1	C_1	C_2
1	0	0.47 µF	Not Installed
2	0	0.47 µF	Not Installed
3	0	0.47 µF	Not Installed
4	0	0.47 µF	Not Installed

Notes:

1. *When the PLL is on, V_{LFx} should be approximately between 1 V and 2 V.*

AC SWITCHING CHARACTERISTICS AND WAVEFORMS

The AC specifications provided in the AC characteristics tables that follow consist of output delays, input setup requirements, and input hold requirements. Figure 31 provides a key to the switching waveforms.

AC specifications measurement is defined by the figures that follow each timing table.

Output delays are specified with minimum and maximum limits, measured as shown. The minimum delay times are hold times provided to external circuitry.

Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct microcontroller operation.

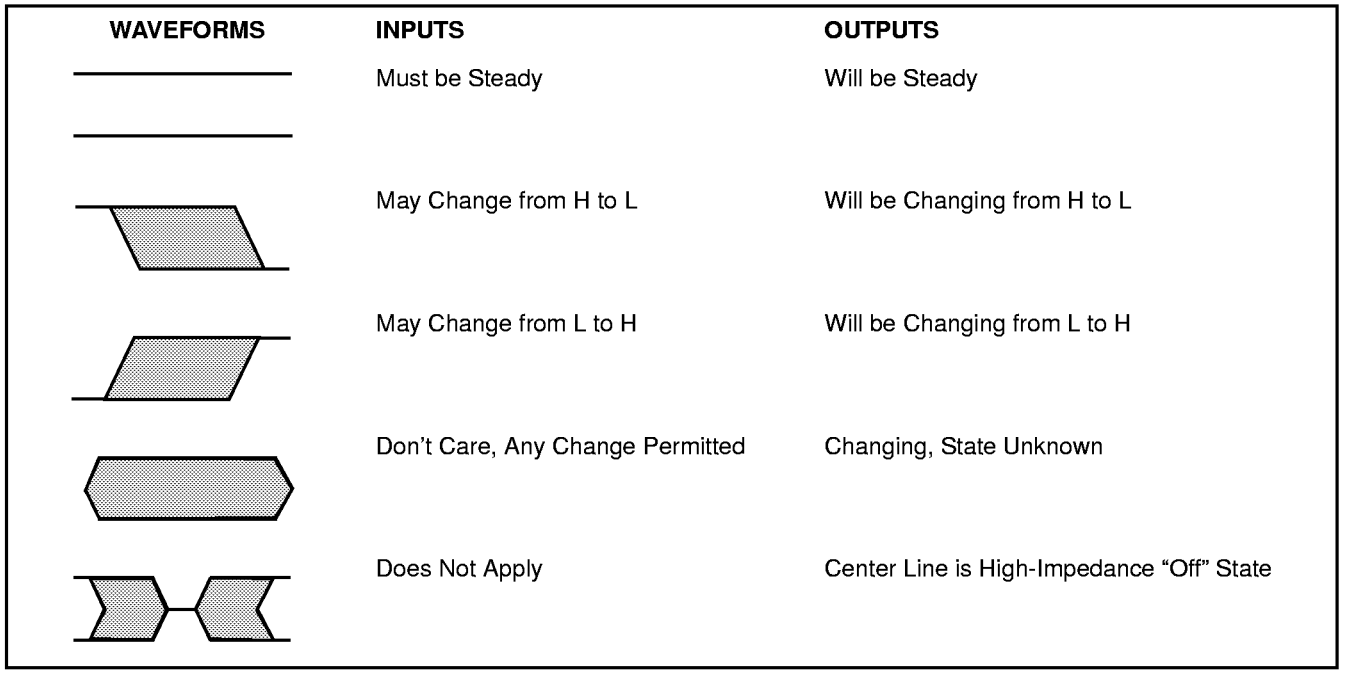
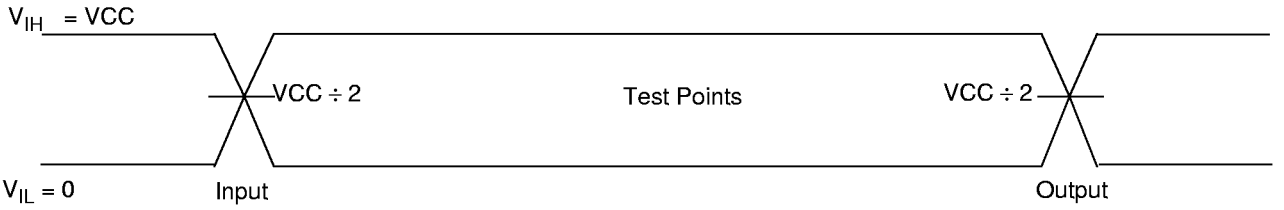


Figure 31. Key to Switching Waveforms

AC Switching Test Waveforms



Notes:

AC Testing: Inputs are driven at 3 V for a logic 1 and 0 V for a logic 0.

AC Switching Characteristics over Commercial and Industrial Operating Ranges

Table 51. Power-Up Sequencing (See Figures 32, 33, 34, and 35)

Symbol	Parameter Description	Notes	Preliminary			Unit
			Min	Typ	Max	
t1	All VCC valid to $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ inactive	1, 2		1		s
t2	$\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ inactive to RSTDRV inactive	2, 3	300			µs
t3	$\overline{\text{IORESET}}$ active to RSTDRV active		0			ns
t4	VSYS2, VCC1, and VSYS valid delay from VCC5		0			ns
t5	VSYS2, VCC1, VSYS, and optionally VMEM valid to $\overline{\text{IORESET}}$ inactive		5			µs
t6	VCC5, VSYS2, VCC1, VSYS hold time from $\overline{\text{IORESET}}$ active		5			µs
t7	VCC5 hold time from VSYS2, VCC1, and VSYS inactive		0			ns

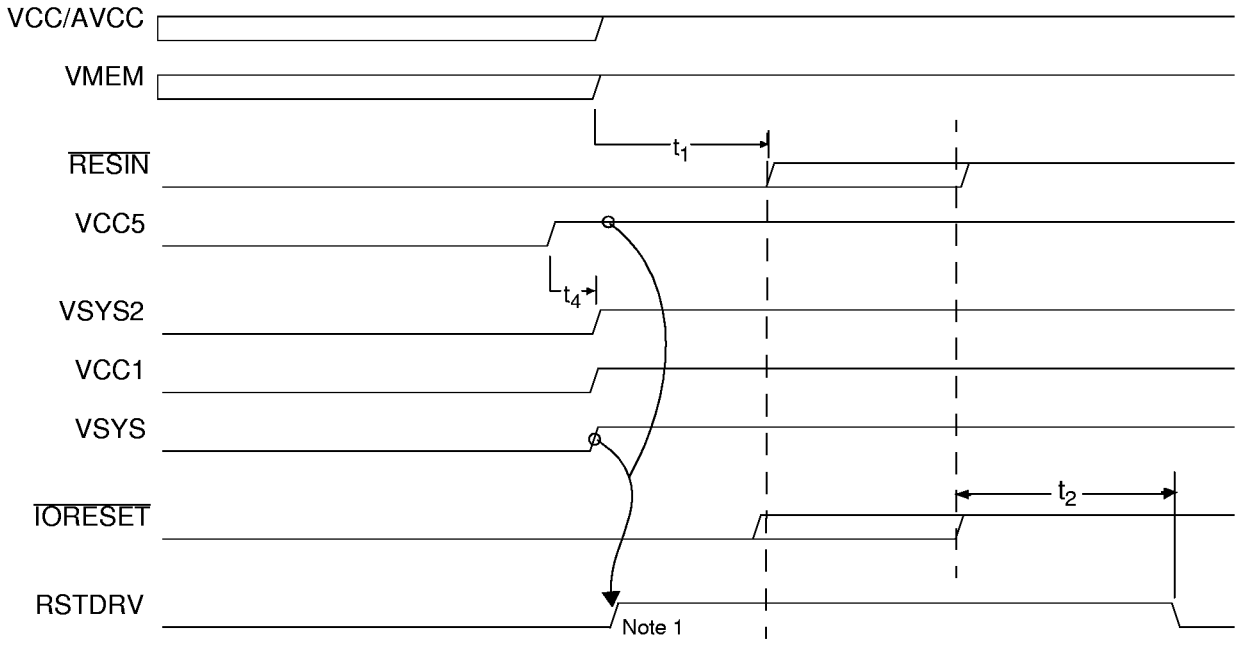
Notes:

1. *This parameter is dependent on the 32-kHz oscillator start-up time. The oscillator start-up time is dependent on the external component values used, board layout, and power supply noise. See the Crystal Specifications section on page 95 for more information.*
2. *$\overline{\text{RESIN}}$ remains inactive during Micro Power Off mode and Micro Power Off mode exit.*
3. *The pulse width of RSTDRV is adjustable based on PLL startup timing. For more information, see "Loop Filters" on page 97.*

Voltage sequencing on power-up for the ÉlanSC300 microcontroller should be observed as follows:

- *VCC*
- *All VCC clamp sources (VCC, VMEM, VSYS, VCC5, and AVCC)*
- *All VCCIO sources (VCC5, VMEM, VSYS, VCC1, VSYS2, and AVCC).*

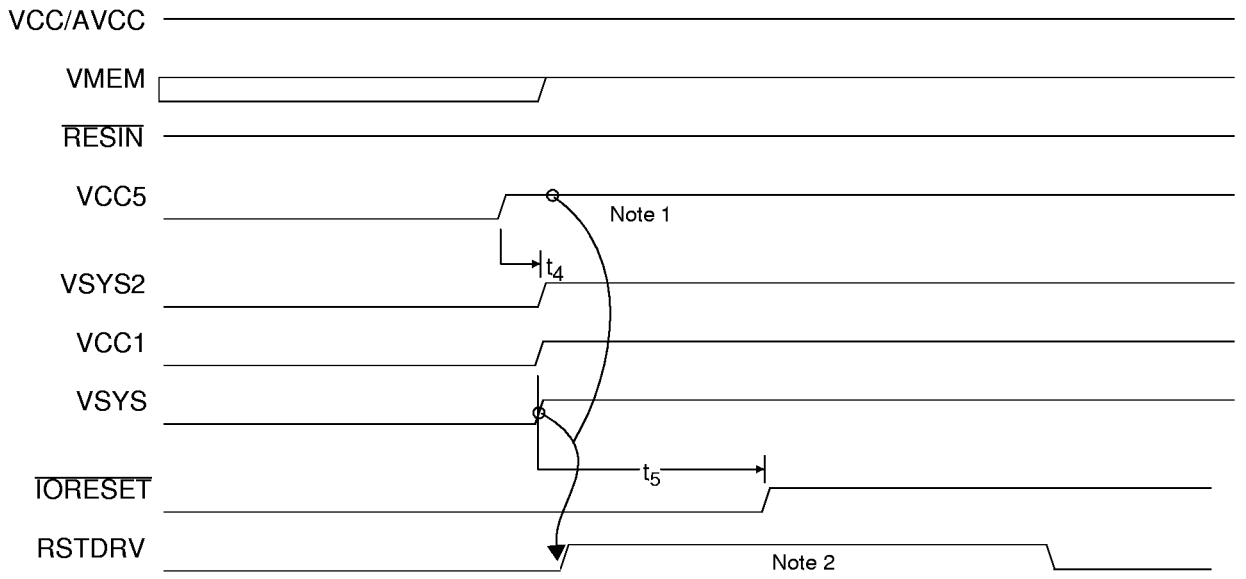
The reverse is true when powering down. For any particular I/O pin, the VCCIO may come up simultaneously with the VCC clamp, but should never precede the VCC clamp. Refer to the Pin Characteristics table (page 24) for detailed I/O information.



Notes:

1. *RSTDRV external driver is powered by: VCCIO = VSYS and VCC Clamp = VCC5.*

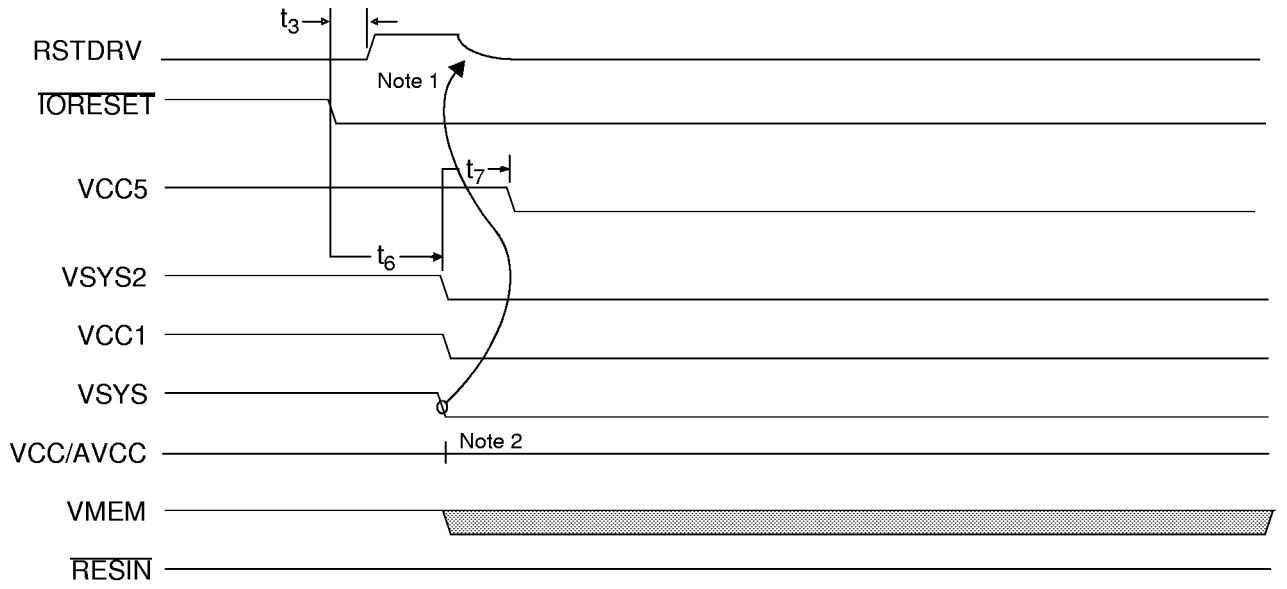
Figure 32. Power-Up Sequence Timing



Notes:

1. *RSTDRV external driver is powered by: VCCIO = VSYS and VCC Clamp = VCC5.*
2. *The pulse width of RSTDRV is adjustable based on PLL startup timing. See the Loop Filters section on page 97 for more information.*

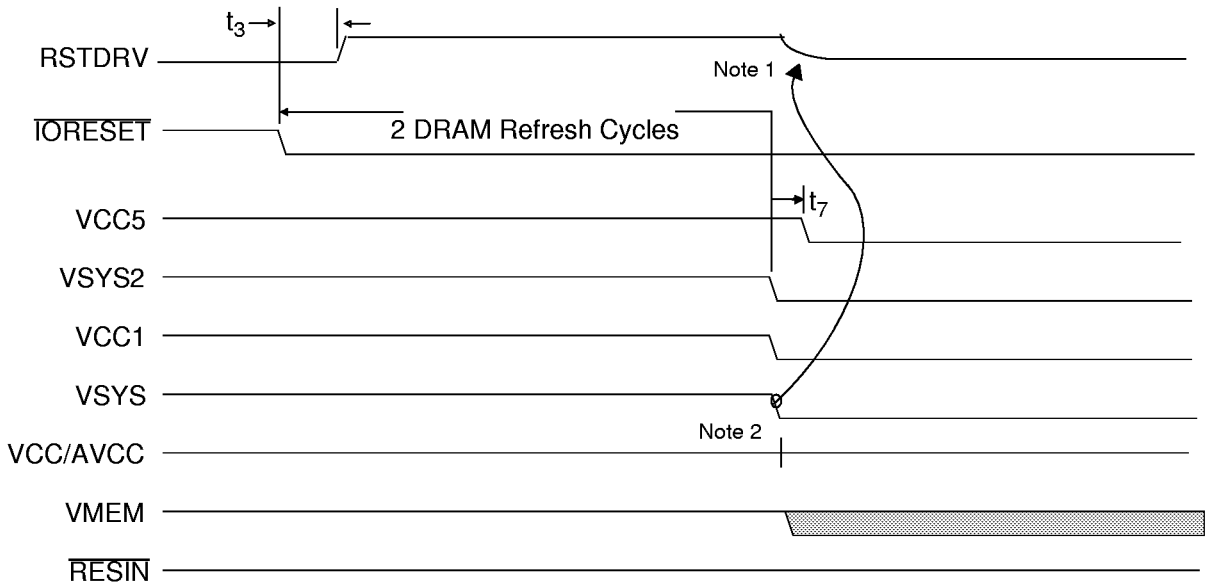
Figure 33. Micro Power Off Mode Exit



Notes:

1. *RSTDRV external driver is powered by: VCCIO = VSYS and VCC Clamp = VCC5.*
2. *A secondary power source could be applied at this time*

Figure 34. Entering Micro Power Off Mode (DRAM Refresh Disabled)



Notes:

1. *RSTDRV external driver is powered by: VCCIO = VSYS and VCC Clamp = VCC5.*
2. *A secondary power source could be applied at this time*

Figure 35. Entering Micro Power Off Mode (DRAM Refresh Enabled)

Table 52. DRAM Memory Interface, Page Hit and Refresh Cycle (See Figures 36 and 37)

Symbol	Parameter Description	Notes	Preliminary		Unit
			Min	Max	
t30	MA valid setup to $\overline{RAS}$ Low		0		ns
t31	MA hold from $\overline{RAS}$ Low		10		ns
t32	MA setup to $\overline{CAS}$ Low		0		ns
t37	$\overline{CAS}$ precharge (Page mode)		10		ns
t38	MA hold from $\overline{CAS}$ active		15		ns
t39	$\overline{RAS}$ to $\overline{CAS}$ delay		20		ns
t41	$\overline{CAS}$ pulse width (page hit)		20	10,000	ns
t42	$\overline{MWE}$ setup to $\overline{CAS}$ Low (page hit)		0		ns
t43	$\overline{MWE}$ hold from $\overline{CAS}$ Low		15		ns
t45	$\overline{CAS}$ cycle time (Page mode)		45		ns
t46	$\overline{CAS}$ Low to D15–D0 valid (read access time)			20	ns
t47	D15–D0 hold from $\overline{CAS}$ High (read)		0		ns
t48	D15–D0 setup to $\overline{CAS}$ Low (write)		0		ns
t49	D15–D0 hold from $\overline{CAS}$ Low (write)		15		ns
t50	$\overline{CAS}$ Low to $\overline{RAS}$ Low (refresh)		10		ns
t51	$\overline{CAS}$ hold from $\overline{RAS}$ Low (refresh)		70		ns
t53	$\overline{RAS}$ pulse width (suspend refresh)		80		ns

Notes:

These timings are based on 33-MHz operation (70 ns or faster DRAM recommended).

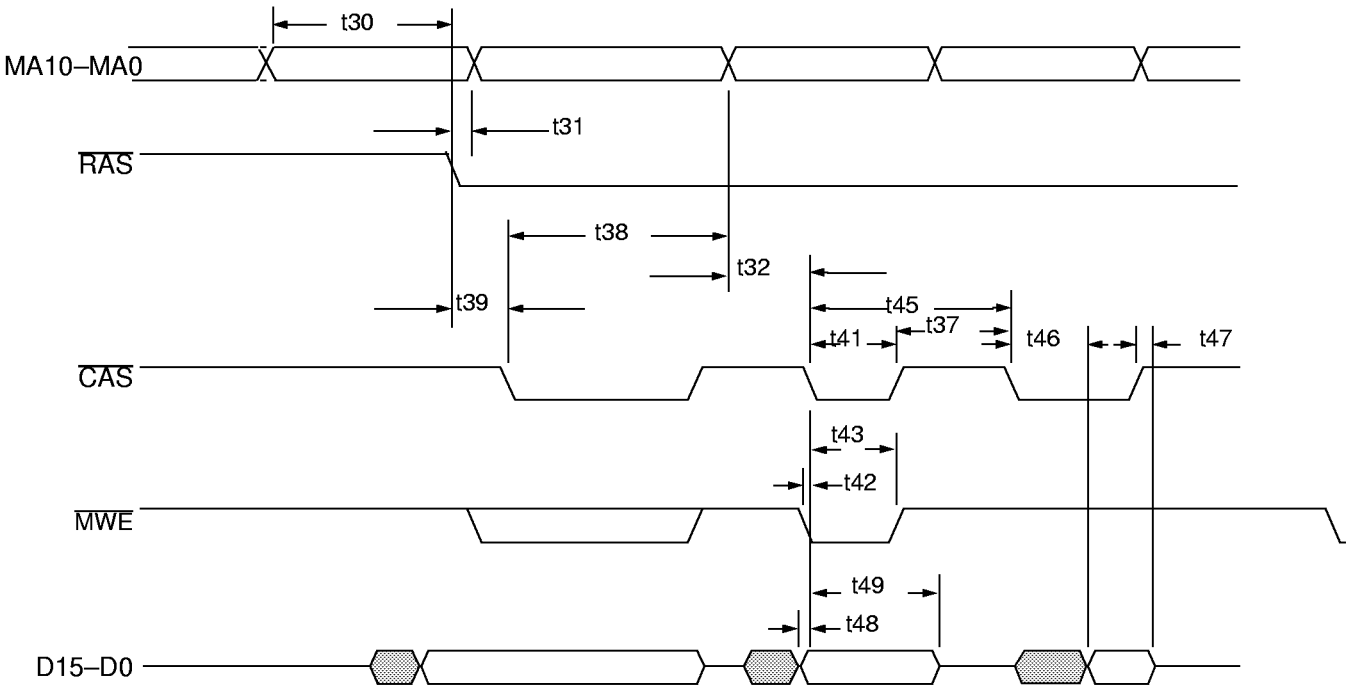


Figure 36. DRAM Timings, Page Hit

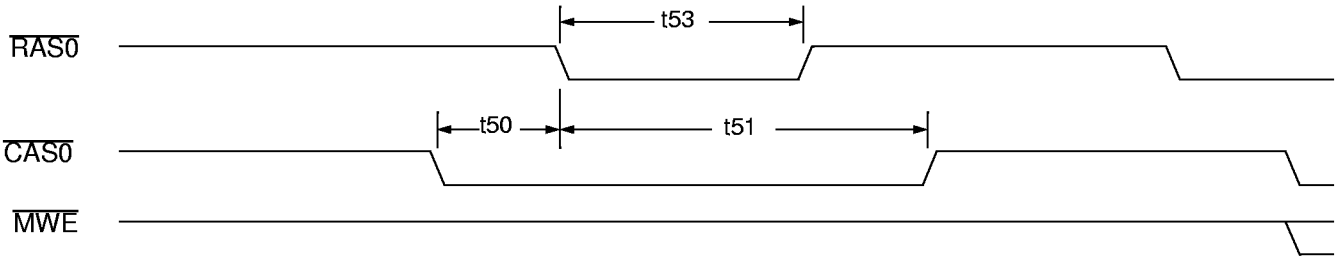


Figure 37. DRAM Timings, Refresh Cycle

Table 53. DRAM First Cycle Read Access (See Figure 38)

Symbol	Parameter Description	Wait States	Min	Max	Unit
t5a	$\overline{CAS}$ Low to data valid (read access time)	1	20		ns
		2	50		ns
		3	80		ns
t28a	$\overline{RAS}$ Low to data valid (read access time)	1	50		ns
		2	80		ns
		3	110		ns
t30	MA valid setup to $\overline{RAS}$ Low	N/A	0		ns
t31	MA hold from $\overline{RAS}$ Low	N/A	10		ns
t32	MA setup to $\overline{CAS}$ Low	N/A	0		ns
t33	$\overline{RAS}$ hold from $\overline{CAS}$ Low	N/A	20		ns
t34	$\overline{RAS}$ precharge from $\overline{CAS}$ High	N/A	10		ns
t38	MA hold from $\overline{CAS}$ active	N/A	15		ns
t39	$\overline{RAS}$ to $\overline{CAS}$ delay	N/A	20		ns
t40	$\overline{RAS}$ pulse width	N/A	70	10,000	ns
t41a	$\overline{CAS}$ pulse width (read, first cycle)	1	30		ns
		2	60		ns
		3	90		ns
t44a	$\overline{CAS}$ hold from $\overline{RAS}$ Low	1	60		ns
		2	90		ns
		3	120		ns

Notes:

For more information about DRAM first cycle read wait states, see the DRAM First Cycle Wait State Select Logic table in Chapter 5 of the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.*

Table 54. DRAM Bank/Page Miss Read Cycles (See Figure 38)

Symbol	Parameter Description	Wait State	Min	Max	Unit
t5b	$\overline{CAS}$ Low to data valid (read access time)	3	35		ns
		4	65		ns
		5	80		ns
t28b	$\overline{RAS}$ Low to data valid (read access time)	3	65		ns
		4	95		ns
		5	110		ns
t29a	$\overline{CAS}$ precharge (page miss read)	N/A	30		ns
t33	$\overline{RAS}$ hold from $\overline{CAS}$ Low	N/A	20		ns
t34	$\overline{RAS}$ precharge from $\overline{CAS}$ High	N/A	10		ns
t36	$\overline{RAS}$ precharge (page miss)	3	38		ns
		4	38		ns
		5	53		ns
t39	$\overline{RAS}$ to $\overline{CAS}$ delay	N/A	30		ns
t40	$\overline{RAS}$ pulse width		70	10,000	ns

Table 54. DRAM Bank/Page Miss Read Cycles (See Figure 38) (Continued)

Symbol	Parameter Description	Wait State	Min	Max	Unit
t41b	$\overline{CAS}$ pulse width (read, page miss)	3	45		ns
		4	75		ns
		5	90		ns
t44b	$\overline{CAS}$ hold from $\overline{RAS}$ Low	3	75		ns
		4	105		ns
		5	120		ns
t47	D15–D0 hold from $\overline{CAS}$ High (read)	N/A	0		ns

Notes:

For more information about DRAM bank miss read wait states, see the DRAM Bank Miss Wait State Select Logic table in Chapter 5 of the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.*

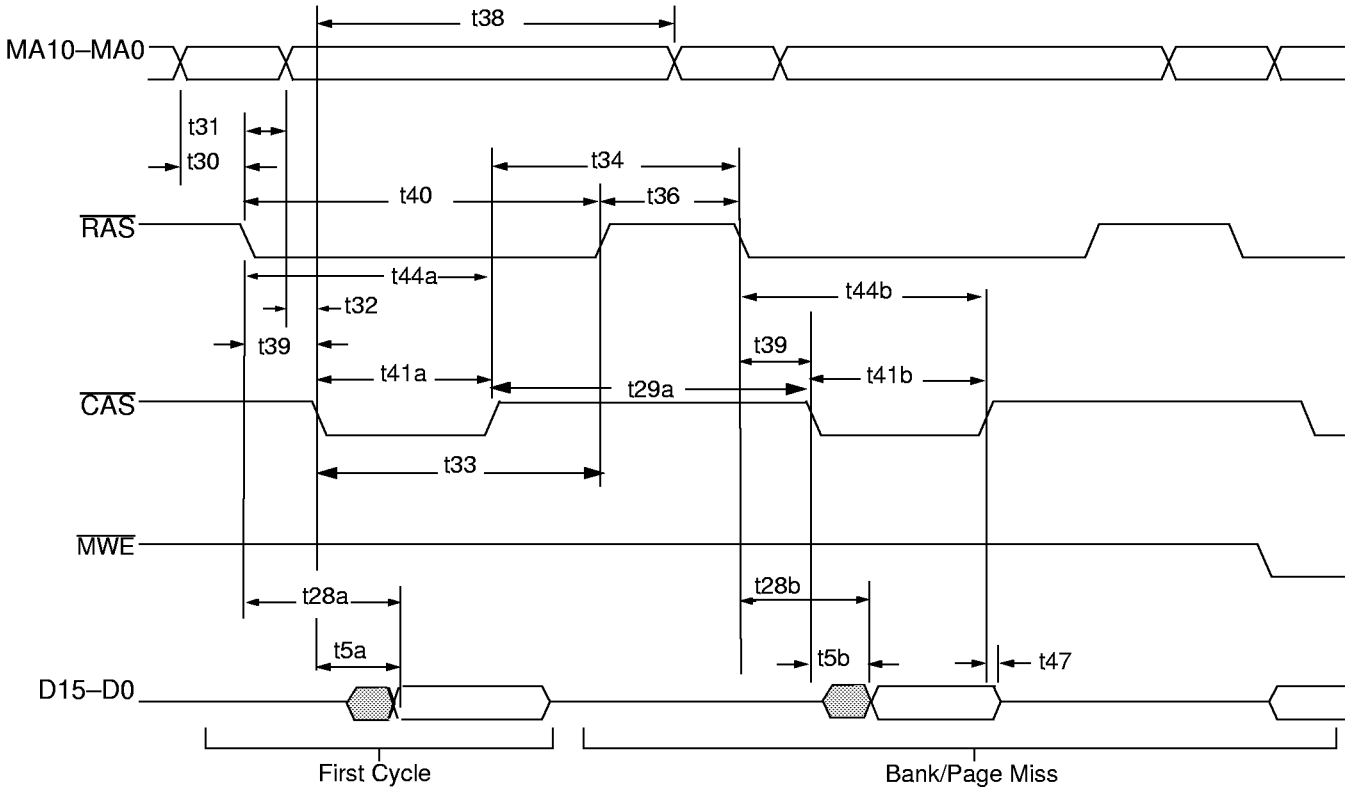


Figure 38. DRAM First Cycle and Bank/Page Miss (Read Cycles)

Table 55. DRAM First Cycle Write Access (See Figure 39)

Symbol	Parameter Description	Wait State	Min	Max	Unit
t5c	D15–D0 setup to $\overline{CAS}$ Low (write)	N/A	5		ns
t27d	$\overline{MWE}$ setup to $\overline{CAS}$ Low (first cycle)	N/A	20		ns
t30	MA valid setup to $\overline{RAS}$ Low	N/A	0		ns
t31	MA hold from $\overline{RAS}$ Low	N/A	10		ns
t32	MA setup to $\overline{CAS}$ Low	N/A	0		ns
t33	$\overline{RAS}$ hold from $\overline{CAS}$ Low	N/A	20		ns
t34	$\overline{RAS}$ precharge from $\overline{CAS}$ High	N/A	10		ns
t38	MA hold from $\overline{CAS}$ active	N/A	15		ns
t39	$\overline{RAS}$ to $\overline{CAS}$ delay	N/A	20		ns
t40	$\overline{RAS}$ pulse width	N/A	70	10,000	ns
t41d	$\overline{CAS}$ pulse width (first cycle, write)	1	15		ns
		2	45		
		3	75		ns
t43	$\overline{MWE}$ hold from $\overline{CAS}$ Low	N/A	15		ns
t44d	$\overline{CAS}$ hold from $\overline{RAS}$ Low (first cycle, write)	1	45		ns
		2	75		ns
		3	105		ns
t49	D15–D0 hold from $\overline{CAS}$ Low (write)	N/A	15		ns

Notes:

For more information about DRAM first cycle write wait states, see the DRAM First Cycle Wait State Select Logic table in Chapter 5 of the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.*

Table 56. DRAM Bank/Page Miss Write Cycles (See Figure 39)

Symbol	Parameter Description	Wait State	Min	Max	Unit
t5c	D15–D0 setup to $\overline{CAS}$ Low (write)	N/A	5		ns
t27c	$\overline{MWE}$ to $\overline{CAS}$ Low	3	65		ns
		4	65		ns
		5	80		ns
t29b	$\overline{CAS}$ precharge (page miss write)	N/A	60		ns
t33	$\overline{RAS}$ hold from $\overline{CAS}$ Low	N/A	20		ns
t34	$\overline{RAS}$ precharge from $\overline{CAS}$ High	N/A	10		ns
t36	$\overline{RAS}$ precharge	3	38		ns
		4	38		ns
		5	53		ns
t39	$\overline{RAS}$ to $\overline{CAS}$ delay	N/A	30		ns
t40	$\overline{RAS}$ pulse width	N/A	70	10,000	ns
t41c	$\overline{CAS}$ pulse width (page miss write)	3	30		ns
		4	60		ns
		5	75		ns
t44c	$\overline{CAS}$ hold from $\overline{RAS}$ Low (page miss write)	3	60		ns
		4	90		ns
		5	105		ns
t49	D15–D0 hold from $\overline{CAS}$ Low (write)	N/A	15		ns

Notes:

For more information about DRAM bank miss wait states, see the DRAM Bank Miss Wait State Select Logic table in Chapter 5 of the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.*

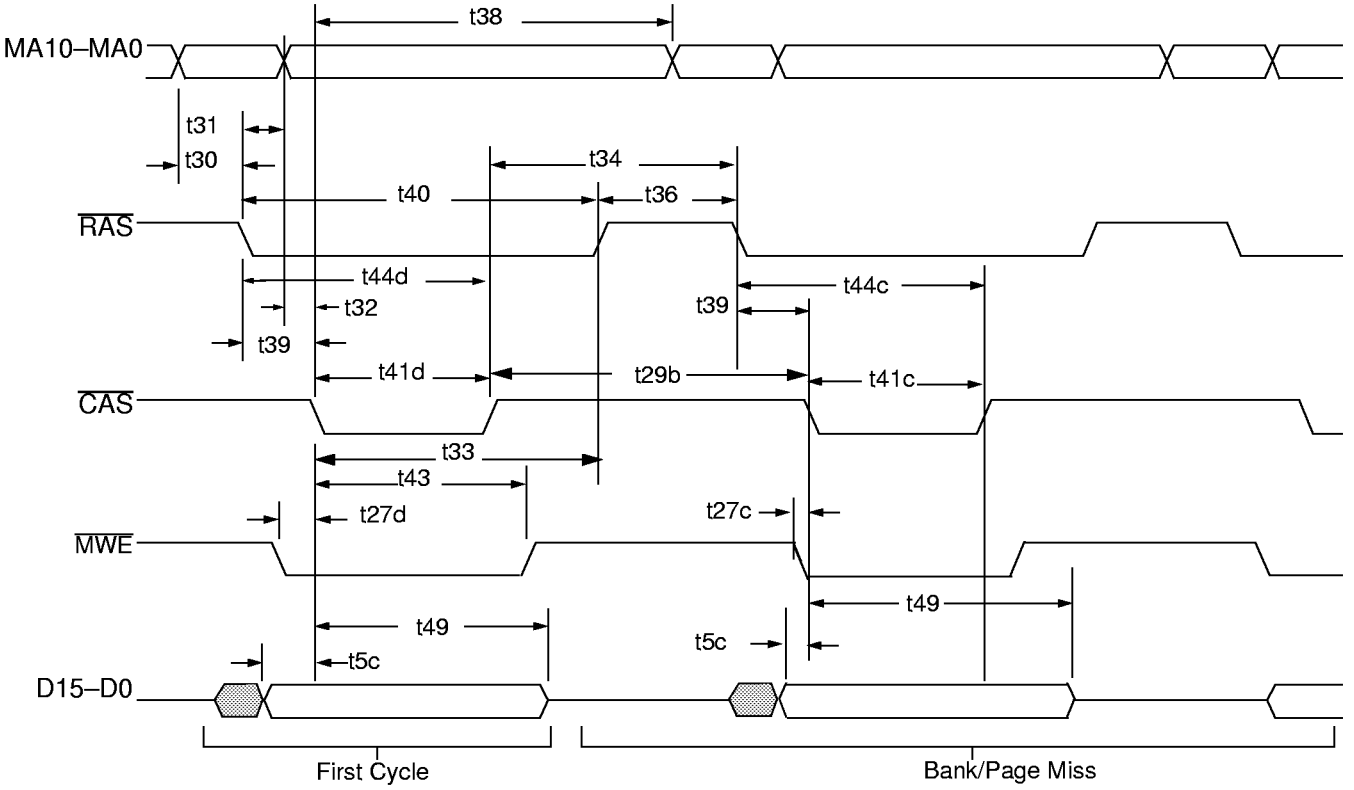


Figure 39. DRAM First Cycle and Bank/Page Miss (Write Cycles)

Table 57. Local Bus Interface (See Figure 40)

Symbol	Parameter Description	Notes	Preliminary		Unit
			Min	Max	
t1	CPUCLK period		14		ns
t2	CPUCLK pulse width low		7		ns
t3	CPUCLK pulse width high		7		ns
t4	$\overline{ADS}$ delay from CPUCLK		3	15	ns
t5	A[23–1] $\overline{BLE}$, $\overline{BHE}$, W/$\overline{R}$,D/$\overline{C}$, M/$\overline{IO}$ delay from CPUCLK		5	23	ns
t6a	$\overline{LDEV}$ valid from address or control (non-zero wait state)		2	20	ns
t6b	$\overline{LDEV}$ valid from address or control (zero wait state)		2	18	ns
t7	$\overline{LRDY}$ valid from CPUCLK		2	12	ns
t8	$\overline{LRDY}$ high impedance from CPUCLK		0	5	ns
t9	$\overline{CPURDY}$ delay from CPUCLK		5	26	ns
t10	$\overline{CPURDY}$ high impedance from CPUCLK		0	5	ns
t11	D15–D0 setup to CPUCLK (read)		7		ns
t12	D15–D0 hold from CPUCLK (read)		0	0	ns
t13	D15–D0 valid from CPUCLK (write)		5	20	ns

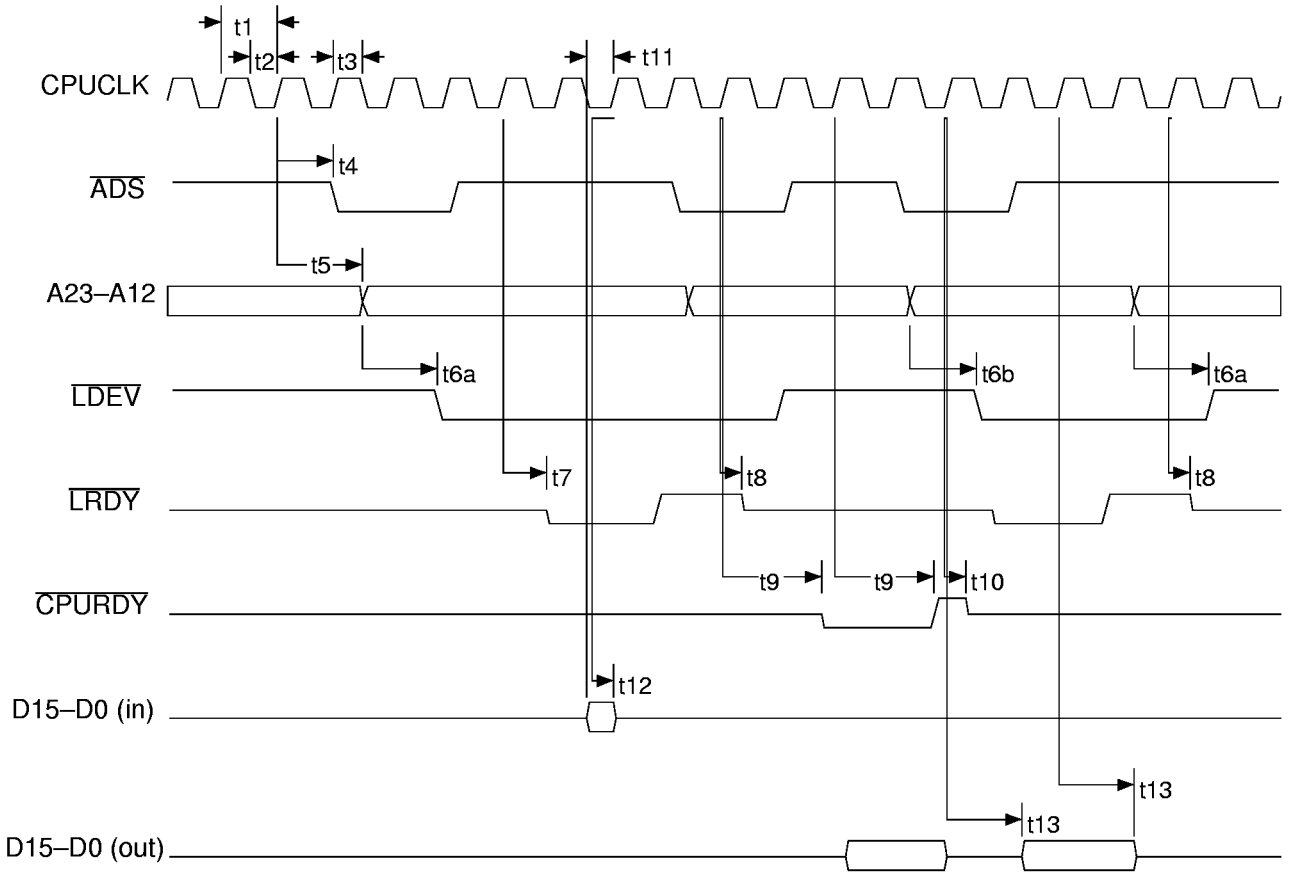


Figure 40. Local Bus Interface

Table 58. Video RAM/LCD Interface (See Figures 41 and 42)

Symbol	Parameter Description	Notes	Preliminary		Unit
			Min	Max	
t81	DSMD hold from DSMA change		5		ns
t82	Display RAM read cycle pulse width		85		ns
t83	DSMD active from $\overline{\text{DSWE}}$ active			50	ns
t84	DSMD setup to $\overline{\text{DSWE}}$ inactive		15		ns
t85	DSMA hold from $\overline{\text{DSWE}}$ inactive		5		ns
t86	DSMD hold from $\overline{\text{DSWE}}$ inactive		0		ns
t87	Display RAM write cycle pulse width		65		ns
t88	DSMD tri-state delay from $\overline{\text{DSOE}}$ High		5	30	ns
t89	DSMD delay from $\overline{\text{DSOE}}$ active		5	30	ns
t90	Panel data setup to CP2 (data clock)		5		ns
t91	Panel data hold from CP2 (data clock)		10		ns
t92	Panel data delay from CP2 (data clock)			10	ns
t93	CP2 allowance time from CP1 (latch pulse)		65		ns
t94	CP1 allowance time from CP2		65		ns
t95	FRM setup time		520		ns
t96	FRM hold time		520		ns
t97	DSMA setup to $\overline{\text{DSWE}}$ active		0		ns

Table 59. Power Management Control Signals (Not Shown)

No.	Parameter Description	Notes	Preliminary		Units
			Min	Max	
	EXTSMI pulse width		10		ns
	$\overline{\text{SUS}}/\overline{\text{RES}}$ pulse width		100		ns
	$\overline{\text{LVDD}}$ active Low to $\overline{\text{LVEE}}$ active Low	1, 3			
	$\overline{\text{LVEE}}$ inactive to $\overline{\text{LVDD}}$ inactive	2, 3			

Notes:

1. *These timings are always controlled via refresh cycle generation and are therefore based on the programmed refresh rate for the system. $\overline{\text{LVEE}}$ active always follows $\overline{\text{LVDD}}$ active by one refresh cycle. This sequence will always occur when the system exits reset or when the system transitions from the Suspend mode to High-Speed PLL mode. The default refresh rate after reset is 15.0 µs. See the* Élan™SC300 Microcontroller Programmer's Reference Manual, *order #18470, for a full description of the power management unit and the refresh control mechanisms.*
2. *$\overline{\text{LVEE}}$ will always be forced to inactive whenever the device enters the Sleep mode, or whenever the Video PLL is forced off in Doze mode. $\overline{\text{LVEE}}$ will remain inactive in Suspend mode. $\overline{\text{LVDD}}$ will remain active until the device enters the Suspend mode, at which point it will be forced inactive.*
3. *The LCD panel data and control signals are all forced to a logical 0 in the power management modes that are programmed to disable the video PLL (i.e., the video PLL may be disabled in Doze, Sleep, and Suspend modes). These signals will be re-driven whenever $\overline{\text{LVDD}}$ is driven active.*

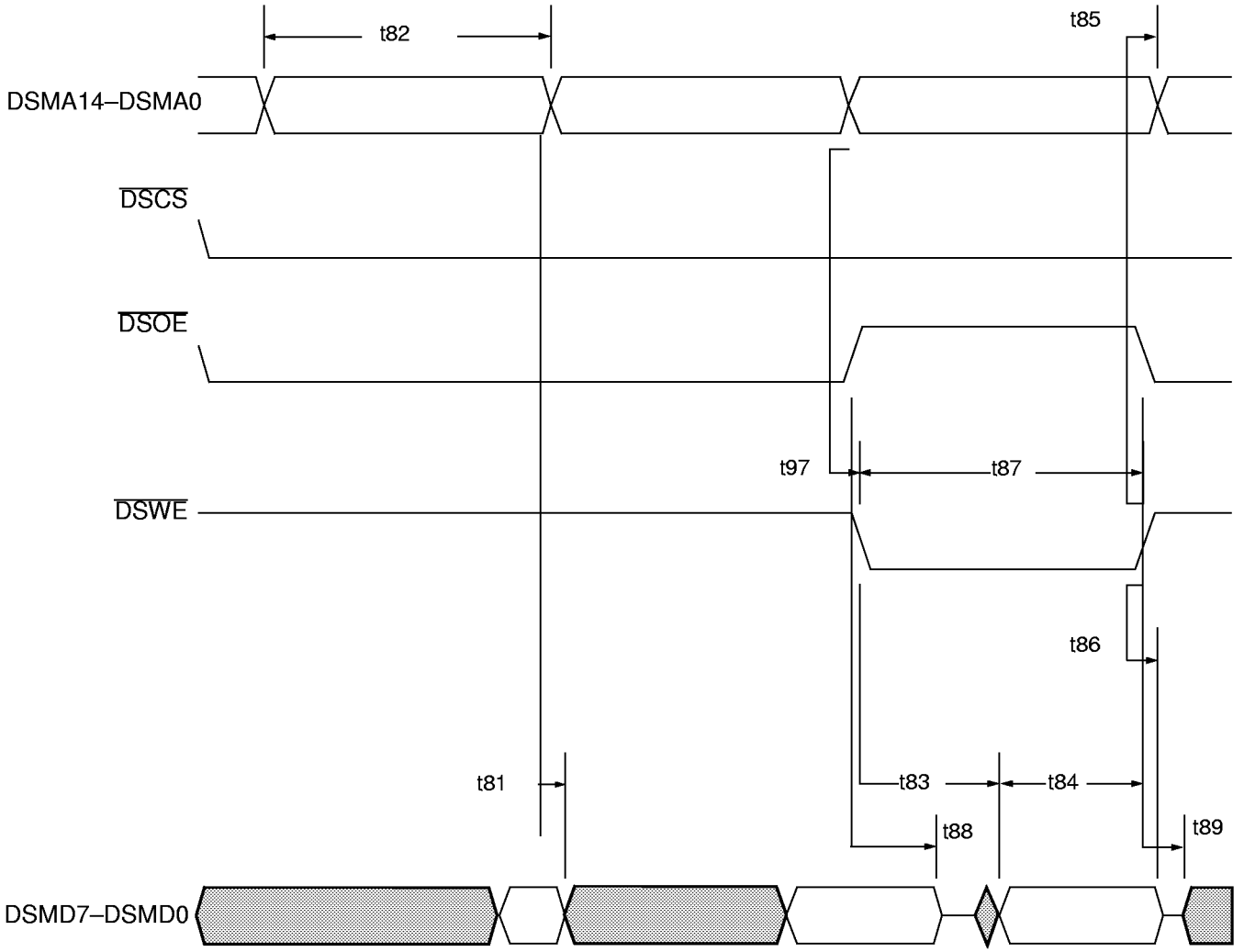


Figure 41. Display SRAM Timings

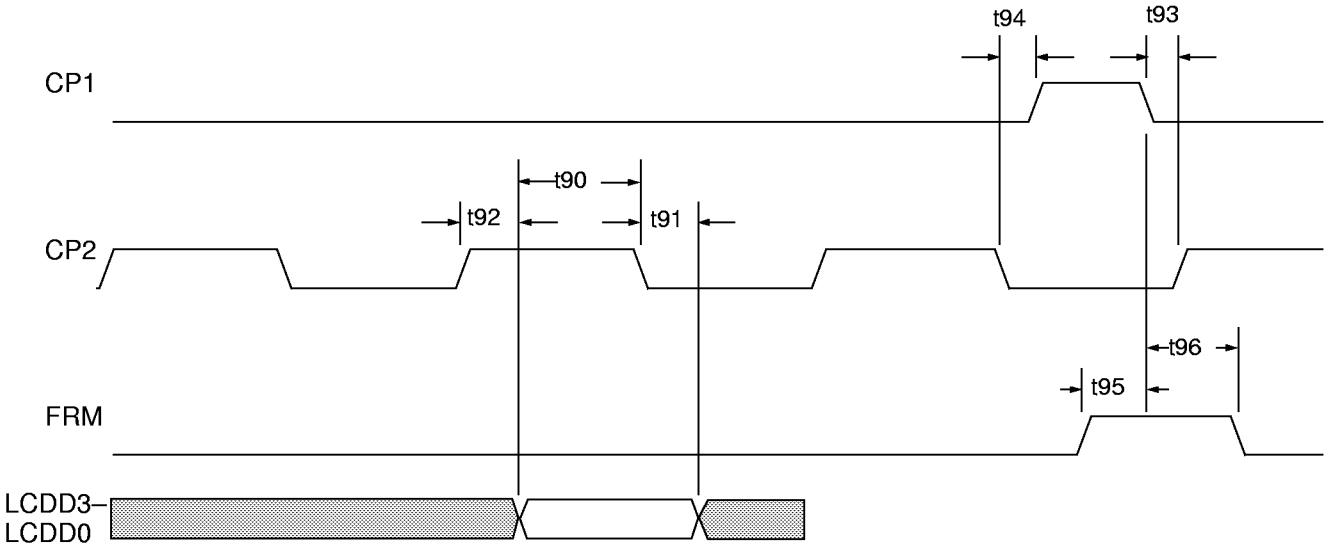


Figure 42. LCD Interface Timings

Table 60. PCMCIA Memory Read Cycle (See Figure 43)

Symbol	Parameter Description	Notes	Preliminary		Unit
			Min	Max	
t1a	Data setup before $\overline{\text{MEMR}}$ inactive (8 bit)		40		ns
t1b	Data setup before $\overline{\text{MEMR}}$ inactive (16 bit)		25		ns
t2	Data hold following $\overline{\text{MEMR}}$		0		ns
t3	$\overline{\text{MEMR}}$ width time		550		ns
t4a	Address setup before $\overline{\text{MEMR}}$ (8 bit)	1	155		ns
t4b	Address setup before $\overline{\text{MEMR}}$ (16 bit)		60		ns
t5	Address hold following $\overline{\text{MEMR}}$	2, 3	0		ns
t6a	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMR}}$ (8 bit)	4	175		ns
t6b	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMR}}$ (16 bit)	4	45		ns
t7	$\overline{\text{MCE}}$ hold after $\overline{\text{MEMR}}$	2, 4	0		ns
t8	$\overline{\text{MEMR}}$ inactive from $\overline{\text{WAIT\_AB}}$ inactive		120		ns
t9	$\overline{\text{WAIT\_AB}}$ delay falling from $\overline{\text{MEMR}}$			35	ns
t10	$\overline{\text{WAIT\_AB}}$ pulse width time	5		12,000	ns
t11	ICDIR setup before $\overline{\text{MEMR}}$		–1		ns
t12	ICDIR hold after $\overline{\text{MEMR}}$		0		ns
t13	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{MEMR}}$		–2		ns
t14	$\overline{\text{DBUFOE}}$ hold after $\overline{\text{MEMR}}$		–2		ns
t15a	ENDIRH, ENDIRL setup before $\overline{\text{MEMR}}$ (8 bit)		170		ns
t15b	ENDIRH, ENDIRL setup before $\overline{\text{MEMR}}$ (16 bit)		45		ns
t16	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4		ns

Notes:

1. *Violates for 600 ns (3.3 V) PCMCIA read cycle only.*
2. *PCMCIA specifies 35 ns for a 600 ns cycle, 20 ns for 250 and 200 ns cycles, and 15 ns for a 100 ns cycle.*
3. *If PCMCIA is buffered, this hold time may be increased by propagation delay through the buffer.*
4. *If the PCMCIA address buffer is controlled via the MCE signals, the output disable/enable delay of the buffer will affect the address setup and hold from $\overline{\text{MEMR}}$.*
5. *$\overline{\text{WAIT\_AB}}$ asserted for longer that 10 µs may cause a DRAM $\overline{\text{RAS}}$ low (max) to be violated if the "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The $\overline{\text{RAS}}$ active timer (10 µs) will not force $\overline{\text{RAS}}$ inactive while the "extended" $\overline{\text{PCMCIA}}$ cycle is occurring.*

These timings are based on default device settings and required initial programming. These timings may be modified via the MMS Memory Wait State 1 and 2 Registers, Index 62h and Index 50h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

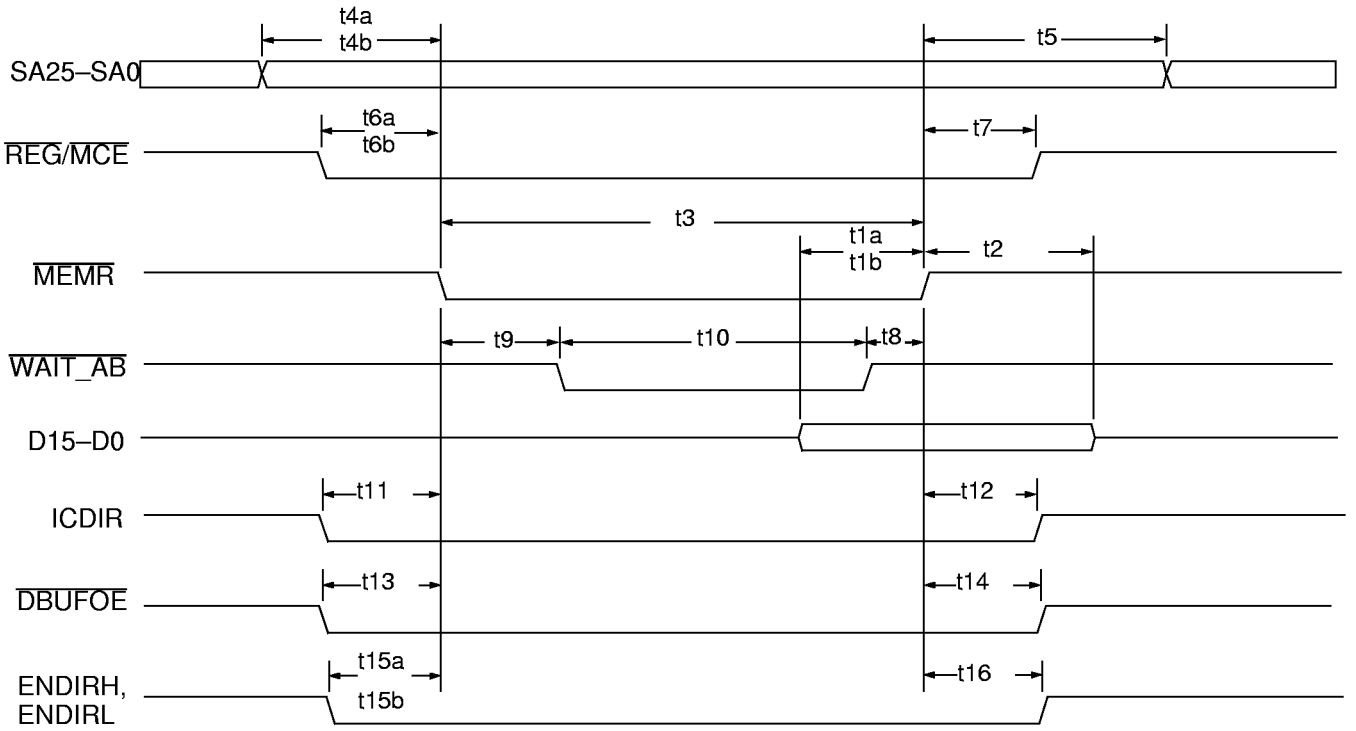


Figure 43. PCMCIA Memory Read Cycle

Table 61. PCMCIA Memory Write Cycle (See Figure 44)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t2	Data hold following $\overline{\text{MEMW}}$		50		ns
t3	$\overline{\text{MEMW}}$ width time		500		ns
t4a	Address setup before $\overline{\text{MEMW}}$ (8 bit)		150		ns
t4b	Address setup before $\overline{\text{MEMW}}$ (16 bit)		60		ns
t5	Address hold following $\overline{\text{MEMW}}$		50		ns
t6a	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMW}}$ (8 bit)		175		ns
t6b	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMW}}$ (16 bit)		45		ns
t7	$\overline{\text{MCE}}$ hold after $\overline{\text{MEMW}}$		40		ns
t8a	Output Enable ($\overline{\text{MEMR}}$) setup before $\overline{\text{MEMW}}$ (8 bit)		200		ns
t8b	Output Enable ($\overline{\text{MEMR}}$) setup before $\overline{\text{MEMW}}$ (16 bit)		100		ns
t9a	Output Enable ($\overline{\text{MEMR}}$) hold after $\overline{\text{MEMW}}$ (8 bit)		250		ns
t9b	Output Enable ($\overline{\text{MEMR}}$) hold after $\overline{\text{MEMW}}$ (16 bit)		150		ns
t10	$\overline{\text{MEMW}}$ inactive from $\overline{\text{WAIT\_AB}}$ inactive		100		ns
t11	$\overline{\text{WAIT\_AB}}$ delay falling from $\overline{\text{MEMW}}$			35	ns
t12	$\overline{\text{WAIT\_AB}}$ pulse width time	1		12,000	ns
t13a	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{MEMW}}$ (8 bit)		150		ns
t13b	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{MEMW}}$ (16 bit)		50		ns
t14	$\overline{\text{DBUFOE}}$ hold after $\overline{\text{MEMW}}$		50		ns

Notes:

1. *$\overline{\text{WAIT\_AB}}$ asserted for longer that 10 µs may cause a DRAM $\overline{\text{RAS}}$ Low (max) to be violated if this "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The $\overline{\text{RAS}}$ active timer (10 µs) will not force $\overline{\text{RAS}}$ inactive while the "extended" PCMCIA cycle is occurring.*

These timings are based on default device settings and required initial programming. These timings may be modified via the MMS Memory Wait State Registers 1 and 2, Index 62h and Index 50h, and Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual, order #18470.)

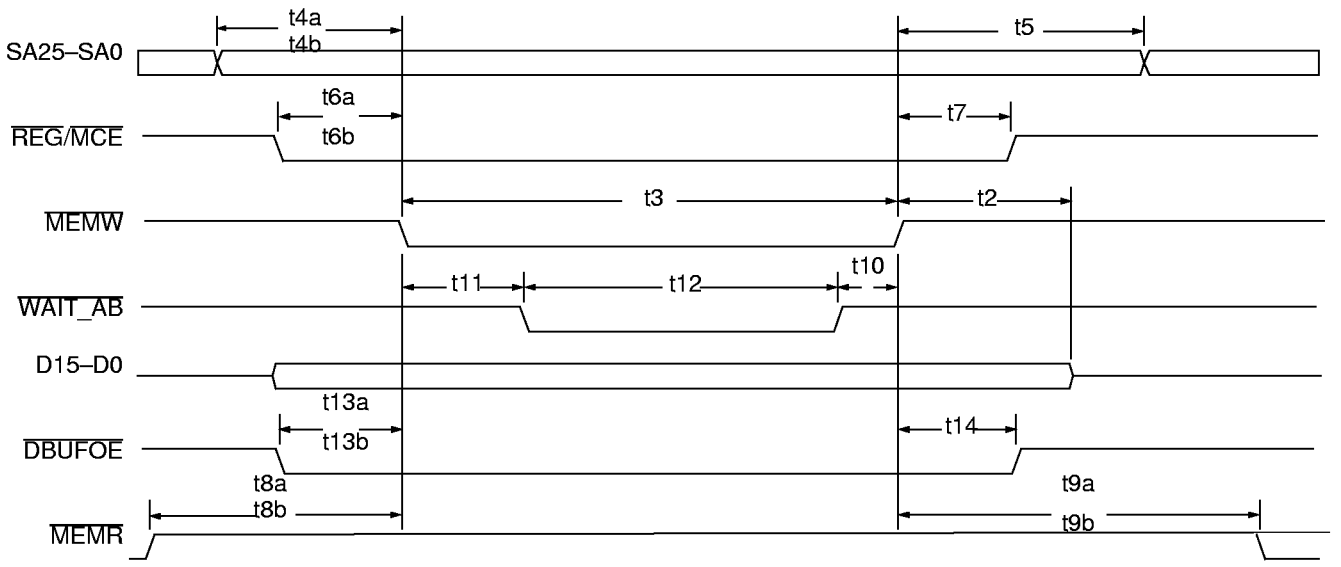


Figure 44. PCMCIA Memory Write Cycle

Table 62. PCMCIA I/O Read Cycle (See Figure 45)

Symbol	Parameter Description	Notes	Version B3 Preliminary		Version B4 Preliminary		Units
			Min	Max	Min	Max	
t1	Data setup before $\overline{IOR}$		40		40		ns
t2	Data hold following $\overline{IOR}$		0		0		ns
t3a	$\overline{IOR}$ width time (8 bit)		560		490		ns
t3b	$\overline{IOR}$ width time (16 bit)		280		225		ns
t4a	Address setup before $\overline{IOR}$ (8 bit)		150		150		ns
t4b	Address setup before $\overline{IOR}$ (16 bit)		115		115		ns
t5	Address hold following $\overline{IOR}$	1	–1		50		ns
t6a	$\overline{MCEL}$ setup before $\overline{IOR}$ (8 bit)	2	160		160		ns
t6b	$\overline{MCEL}$ setup before $\overline{IOR}$ (16 bit)		100		100		ns
t7	$\overline{MCE}$ hold after $\overline{IOR}$	1, 2	5		65		ns
t8	$\overline{REG}$ setup before $\overline{IOR}$		5		5		ns
t9	$\overline{REG}$ hold after $\overline{IOR}$		0		65		ns
t10	$\overline{IOIS16}$ delay falling from Address			35		35	ns
t11	$\overline{IOIS16}$ delay rising from Address			35		35	ns
t12	$\overline{WAIT\_AB}$ delay falling from $\overline{IOR}$			35		35	ns
t13	$\overline{WAIT\_AB}$ pulse width time	3		12,000		12,000	ns
t14	ICDIR setup before $\overline{IOR}$		–5		–5		ns
t15	ICDIR hold after $\overline{IOR}$		0		5		ns
t16	$\overline{DBUFOE}$ setup before $\overline{IOR}$		–3		–3		ns
t17	$\overline{DBUFOE}$ hold after $\overline{IOR}$		–3		45		ns
t18a	ENDIRH, ENDIRL setup before $\overline{IOR}$ (8 bit)		170		170		ns
t18b	ENDIRH, ENDIRL setup before $\overline{IOR}$ (16 bit)		110		110		ns
t19	ENDIRH, ENDIRL hold from $\overline{IOR}$		–6		45		ns
t20	$\overline{MCEH}$ delay from $\overline{IOIS16}$ active			50		50	ns
t21	$\overline{IOR}$ inactive from $\overline{WAIT\_AB}$ inactive		100		100		ns

Notes:

1. *PCMCIA specifies 20 ns (min) for 5 V I/O cards.*
2. *If the PCMCIA address buffer is controlled via the MCE signals, the output disable/enable delay of the buffer will affect the address setup and hold from $\overline{MEMR}$.*
3. *$\overline{WAIT\_AB}$ asserted for greater that 10 µs may cause a DRAM $\overline{RAS}$ low (max) to be violated if the "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The $\overline{RAS}$ active timer (10 µs) will not force $\overline{RAS}$ inactive while the "extended" $\overline{PCMCIA}$ cycle is occurring.*

These timings are based on default device settings and required initial programming. These timings may be modified via the Wait State Control and Command Delay Register. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

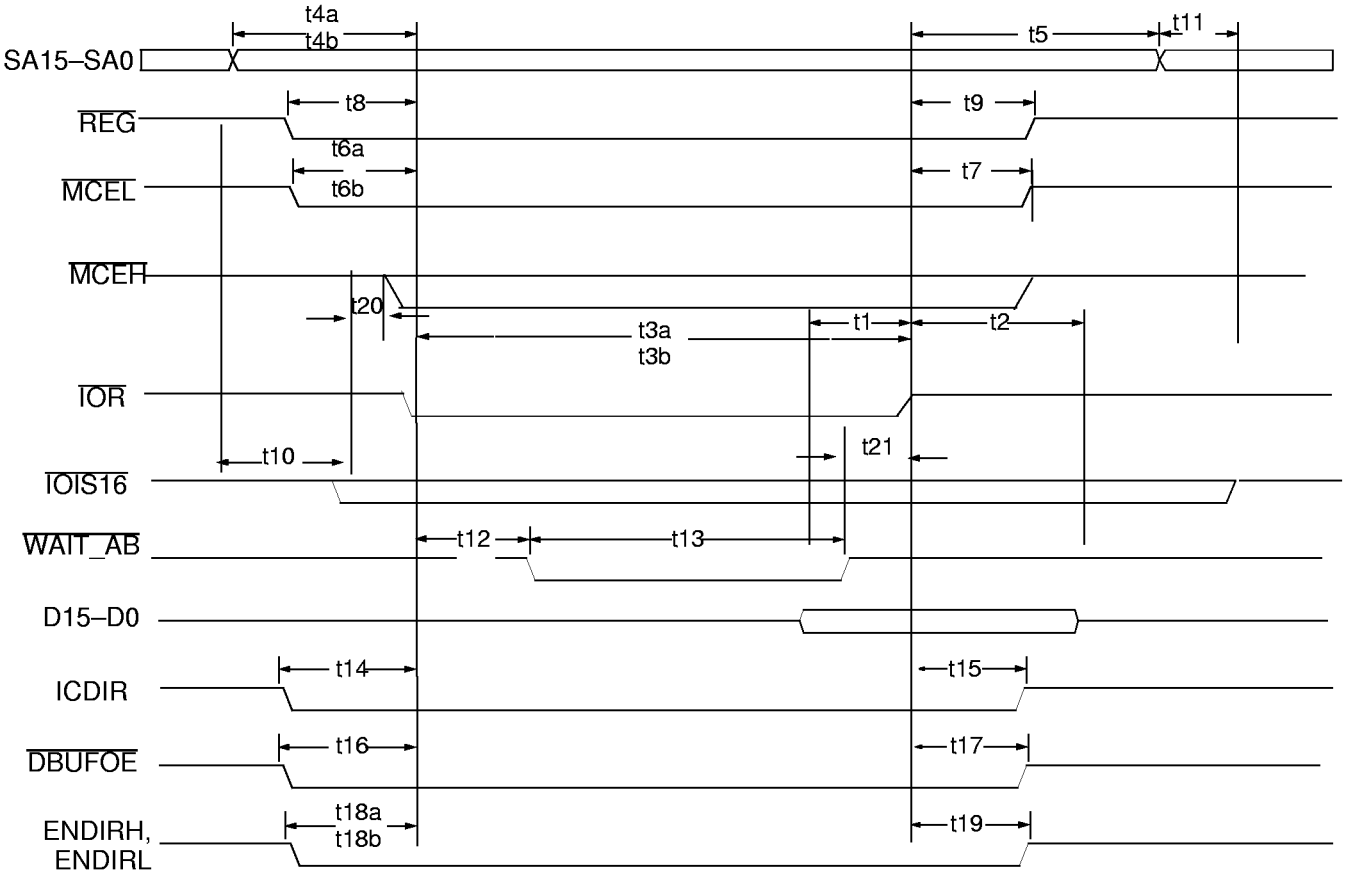


Figure 45. PCMCIA I/O Read Cycle

Table 63. PCMCIA I/O Write Cycle (See Figure 46)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1	Data setup before $\overline{IOW}$ active	2	25		ns
t2	Data hold following $\overline{IOW}$		50		ns
t3a	$\overline{IOW}$ width time (8 bit)		440		ns
t3b	$\overline{IOW}$ width time (16 bit)		165		ns
t4a	Address setup before $\overline{IOW}$ (8 bit)		175		ns
t4b	Address setup before $\overline{IOW}$ (16 bit)		165		ns
t5	Address hold following $\overline{IOW}$		50		ns
t6a	$\overline{MCEL}$ setup before $\overline{IOW}$ (8 bit)		215		ns
t6b	$\overline{MCEL}$ setup before $\overline{IOW}$ (16 bit)		160		ns
t7	$\overline{MCE}$ hold after $\overline{IOW}$		50		ns
t8a	$\overline{REG}$ setup before $\overline{IOW}$ (8 bit)		230		ns
t8b	$\overline{REG}$ setup before $\overline{IOW}$ (16 bit)		170		ns
t9	$\overline{REG}$ hold after $\overline{IOW}$		50		ns
t10	$\overline{IOIS16}$ delay falling from Address			35	ns
t11	$\overline{IOIS16}$ delay rising from Address			35	ns
t12	$\overline{WAIT\_AB}$ delay falling from $\overline{IOW}$			35	ns
t13	$\overline{WAIT\_AB}$ pulse width time	1		12,000	ns
t14a	$\overline{DBUFOE}$ setup before $\overline{IOW}$ (8 bit)		230		ns
t14b	$\overline{DBUFOE}$ setup before $\overline{IOW}$ (16 bit)		165		ns
t15	$\overline{DBUFOE}$ hold after $\overline{IOW}$		50		ns
t16	$\overline{MCEH}$ delay from $\overline{IOIS16}$ active			50	ns
t17	$\overline{IOW}$ inactive from $\overline{WAIT\_AB}$ inactive		100		ns

Notes:

1. *$\overline{WAIT\_AB}$ asserted for longer than 10 µs may cause a DRAM $\overline{RAS}$ Low (max) to be violated if this "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The $\overline{RAS}$ active timer (10 µs) will not force $\overline{RAS}$ inactive while the "extended" PCMCIA cycle is occurring.*
2. *PCMCIA specifies 60 ns minimum for data setup to I/O write active.*

These timings are based on default device settings and required initial programming. These timings may be modified via the Wait State Control and Command Delay Registers. (See the Élan™SC300 Microcontroller Programmer's Reference Manual, *order #18470.)*

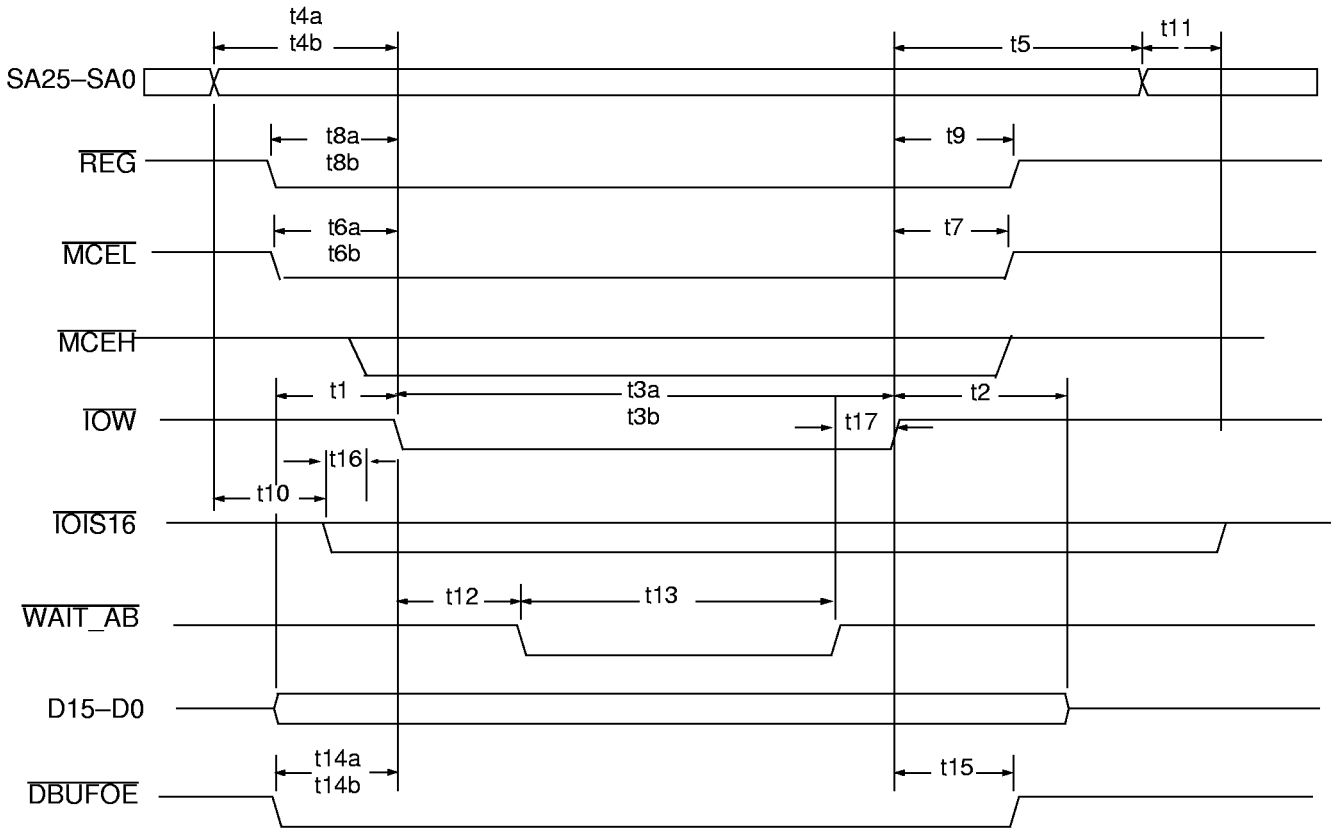


Figure 46. PCMCIA I/O Write Cycle

Table 64. BIOS ROM Read/Write 8-Bit Cycle (See Figure 47)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1a	SA stable to $\overline{\text{ROMCS}}$ active	1	55		ns
t1b	SA stable to $\overline{\text{ROMCS}}$ active	2		5	ns
t2a	SA hold from $\overline{\text{ROMCS}}$ inactive (write)	1	50		ns
t2b	SA hold from $\overline{\text{ROMCS}}$ inactive (read)	1	0		ns
t3a	$\overline{\text{ROMCS}}$ pulse width (read)	1	390		ns
t3b	$\overline{\text{ROMCS}}$ pulse width (write)	1	335		ns
t4a	$\overline{\text{MEMW}}$ active to $\overline{\text{ROMCS}}$ active	1		2	ns
t4b	$\overline{\text{MEMR}}$ active to $\overline{\text{ROMCS}}$ active	1		1	ns
t5a	$\overline{\text{ROMCS}}$ hold from $\overline{\text{MEMW}}$ inactive	1	0		ns
t5b	$\overline{\text{ROMCS}}$ hold from $\overline{\text{MEMR}}$ inactive	1	0		ns
t6	RDDATA setup to command inactive		40		ns
t7	RDDATA hold from command inactive		0		ns
t8	WRDATA setup to command inactive		200		ns
t9	WRDATA hold from command inactive		50		ns
t10	$\overline{\text{DBUFOE}}$ active from command			5	ns
t11a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50		ns
t11b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2		ns
t12	ENDIRH, ENDIRL setup before $\overline{\text{MEMR}}$			50	ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4		ns
t14	$\overline{\text{ROMCS}}$ active to command active	2	65		ns
t15	$\overline{\text{ROMCS}}$ hold from SA	2	5		ns

Notes:

1. *This is the timing when $\overline{\text{ROMCS}}$ is qualified with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$, (Bit 2 of the Miscellaneous 5 Register, Index B3h, = 0.)*
2. *This is the timing when $\overline{\text{ROMCS}}$ is configured as an address decode, (Bit 2 of the Miscellaneous 5 Register, Index B3h, = 1.)*

These timings are based on default wait state settings, set for three wait states in bits 4 and 7 of the Command Delay Register, Index 60h, and required initial programming. These timings may be modified via the MMS Memory Wait State 1 Register, Index 62h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual, *order #18470.) For fast $\overline{\text{ROMCS}}$ (BIOS ROM) accesses, set bit 6 of Miscellaneous 5 Register, Index B3h. Bits 4 and 5 control wait states when fast $\overline{\text{ROMCS}}$ is enabled. For more information, see Table 66, "DOS ROM and Fast DOS ROM Read/Write 16-Bit Cycles (See Figure 49)," on page 124. Also see the* Élan™SC300 and Élan™SC310 Devices' ISA Bus Anomalies Application Note, *order #20747.*

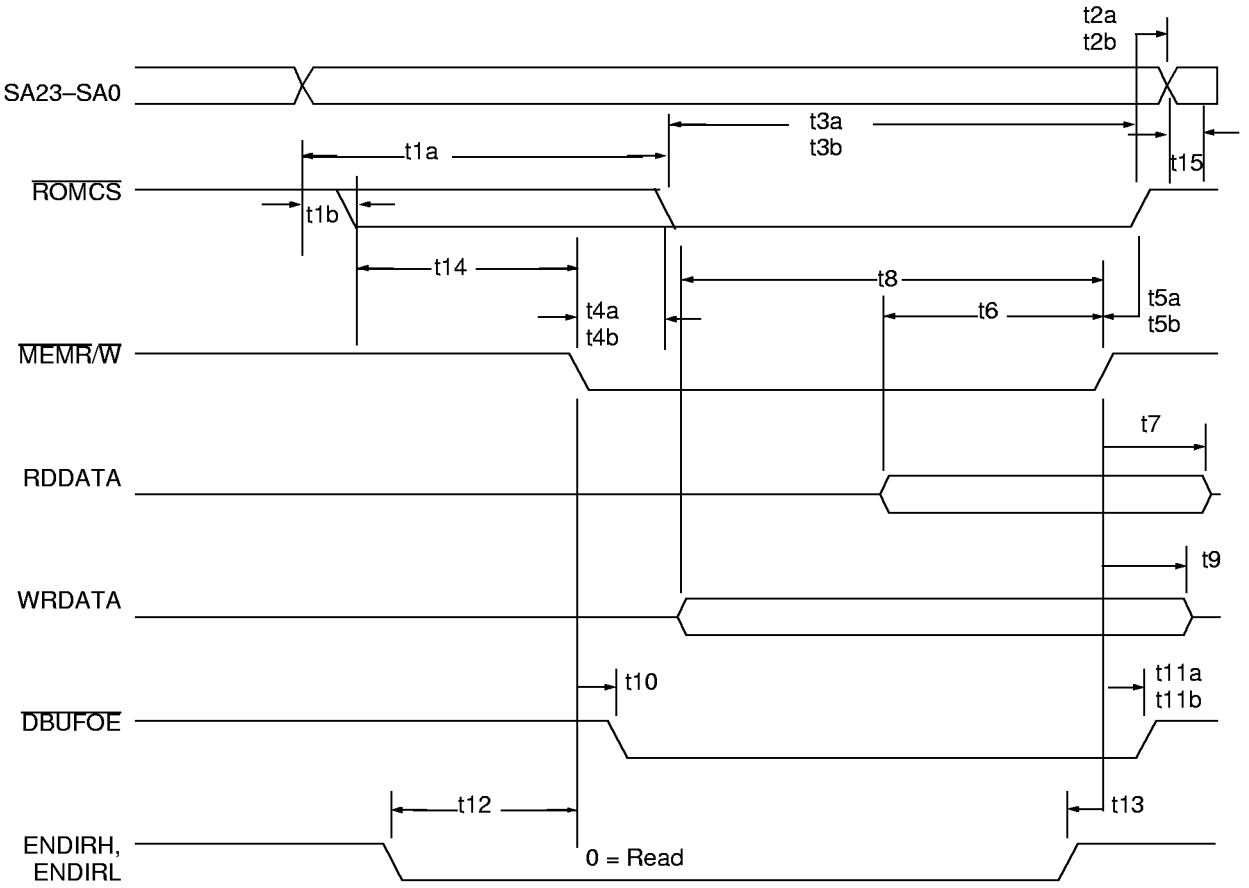


Figure 47. BIOS ROM Read/Write 8-Bit Cycle

Table 65. DOS ROM Read/Write 8-Bit Cycle (See Figure 48)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1a	SA stable to $\overline{\text{DOSCS}}$ active	1	160		ns
t1b	SA stable to $\overline{\text{DOSCS}}$ active	2		5	ns
t2a	SA hold from $\overline{\text{DOSCS}}$ inactive (write)	1	50		ns
t2b	SA hold from $\overline{\text{DOSCS}}$ inactive (read)	1	0		ns
t3a	$\overline{\text{DOSCS}}$ pulse width (read)	1	550		ns
t3b	$\overline{\text{DOSCS}}$ pulse width (write)	1	500		ns
t4a	$\overline{\text{MEMW}}$ active to $\overline{\text{DOSCS}}$ active	1		4	ns
t4b	$\overline{\text{MEMR}}$ active to $\overline{\text{DOSCS}}$ active	1		4	ns
t5a	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMW}}$ inactive	1		0	ns
t5b	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMR}}$ inactive	1		0	ns
t6	RDDATA setup to command inactive		40		ns
t7	RDDATA hold from command inactive		0		ns
t8	WRDATA setup to command inactive		90		ns
t9	WRDATA hold from command inactive		50		ns
t10	$\overline{\text{DBUFOE}}$ active from command			5	ns
t11a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50		ns
t11b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2		ns
t12	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$			50	ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–3		ns
t14	$\overline{\text{DOSCS}}$ active to command active	2	170		ns
t15	$\overline{\text{DOSCS}}$ hold from SA	2	5		ns

Notes:

1. *This is the timing when $\overline{\text{DOSCS}}$ is qualified with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$, (Bit 4 of ROM Configuration 3 Register, Index B8h, = 0).*
2. *This is the timing when $\overline{\text{DOSCS}}$ is configured as an address decode, (Bit 4 of ROM Configuration 3 Register, Index B8h, = 1).*

These timings are based on default settings with bit 2 in Index 50h set to 0 and bits 0 and 1 in Index 62h equal to 0 for 5 wait states, and required initial programming. These timings may be modified via the MMS Memory Wait State 1 Register, Index 62h, the Command Delay Register, Index 60h, and the MMS Memory Wait State 2 Register Index 50h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

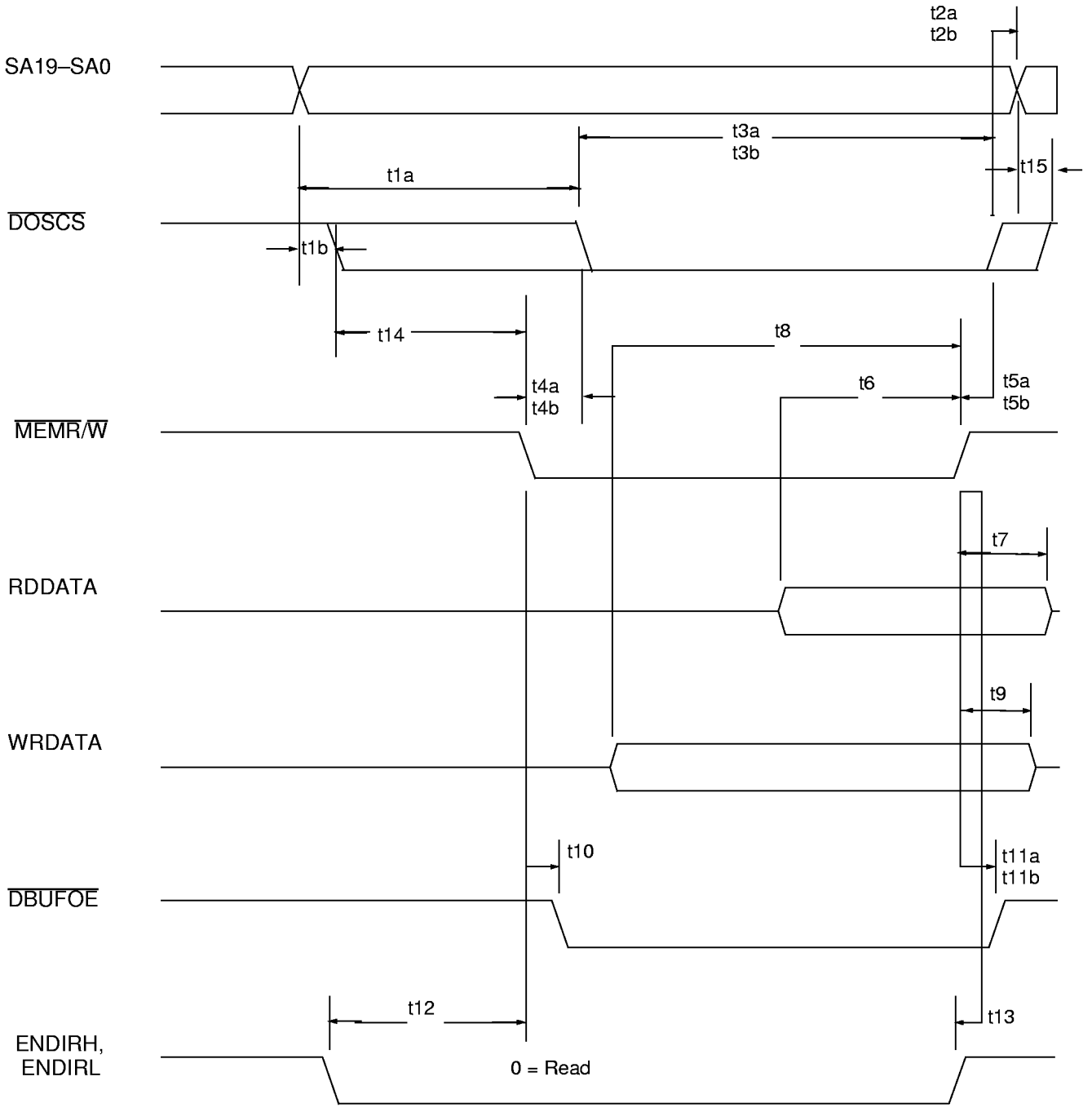


Figure 48. DOS ROM Read/Write 8-Bit Cycle

Table 66. DOS ROM and Fast DOS ROM Read/Write 16-Bit Cycles (See Figure 49)

Symbol	Parameter Description	Notes	Standard DOS ROM Preliminary		Fast DOS 33 MHz Preliminary		Fast DOS 25 MHz Preliminary		Units
			Min	Max	Min	Max	Min	Max	
t1a	SA stable to $\overline{\text{DOSCS}}$ active	1	65		25		25		ns
t1b	SA stable to $\overline{\text{DOSCS}}$ active	2		5		5		8	ns
t2a	SA hold from $\overline{\text{DOSCS}}$ inactive (write)	1	50		15		20		ns
t2b	SA hold from $\overline{\text{DOSCS}}$ inactive (read)	1	0		0		0		ns
t3a	$\overline{\text{DOSCS}}$ pulse width (read)	1	550		130		250		ns
t3b	$\overline{\text{DOSCS}}$ pulse width(write)	1	500		100		175		ns
t4a	$\overline{\text{MEMW}}$ active to $\overline{\text{DOSCS}}$ active	1		3		3		3	ns
t4b	$\overline{\text{MEMR}}$ active to $\overline{\text{DOSCS}}$ active	1		4		4		4	ns
t5a	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMW}}$ inactive	1	0		0		0		ns
t5b	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMR}}$ inactive	1	0		0		0		ns
t6	RDDATA setup to command inactive		25		25		33		ns
t7	RDDATA hold from command inactive		0		0		0		ns
t8	WRDATA setup to command inactive		400		120		160		ns
t9	WRDATA hold from command inactive		45		15		20		ns
t10	$\overline{\text{DBUFOE}}$ active from command			5		5		0	ns
t11a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50		15		20		ns
t11b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2		–2		0		ns
t12	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$		50		15		20		ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4		–4		–4		ns
t14	$\overline{\text{DOSCS}}$ active to command active	2	65		15		20		ns
t15	$\overline{\text{DOSCS}}$ hold from $\overline{\text{SA}}$	2	5		5		5		ns
t16a	$\overline{\text{MEMR}}$ pulse width		550		130		250		ns
t16b	$\overline{\text{MEMW}}$ pulse width		500		100		175		ns

Notes:

1. *This is the timing when $\overline{\text{DOSCS}}$ is qualified with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$, (Bit 4 of ROM Configuration 3 Register, Index B8h, = 0).*
2. *This is the timing when $\overline{\text{DOSCS}}$ is configured as an address decode, (Bit 4 of ROM Configuration 3 Register, Index B8h, = 1).*

These timings are based on Index 51h, bit 1 set for 16-bit $\overline{\text{DOSCS}}$ cycles, and required initial programming. The standard DOS ROM timings are based on the default wait state settings in bits 2 and 3 of the MMS Memory Wait State Register, Index 62h, set to 4 wait states. The fast DOS ROM timings are based on Index B8h, bit 7 set for $\overline{\text{DOSCS}}$ cycles to run at high-speed with the default setting in bits 5 and 6 for 4-wait states.

These timings may be modified via the Command Delay Register, Index 60h. (See the Élan™SC310 Microcontroller Programmer's Reference Manual*, order #18470.)*

For more information about fast DOS ROM cycles, see the Élan™SC300 and Élan™SC310 Devices' ISA Bus Anomalies Application Note*, order #20747. The fast DOS ROM timings shown here also apply to fast BIOS ROM (ROMCS) accesses controlled by Miscellaneous 5 Register, Index B3h.*

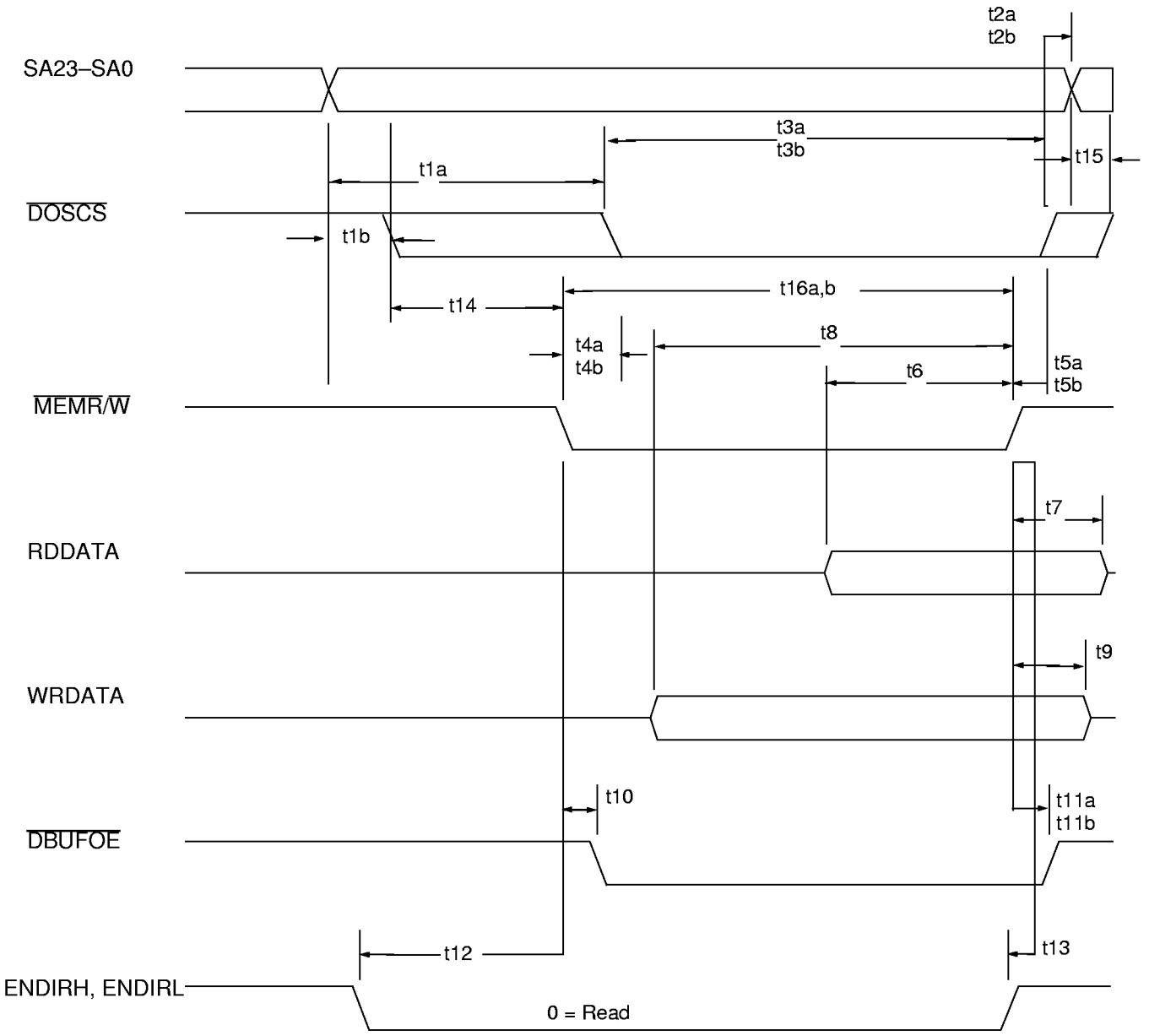


Figure 49. DOS ROM Read/Write 16-Bit Cycle

Table 67. ISA Memory Read/Write 8-Bit Cycle (See Figure 50)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1	LA stable to BALE inactive		60		ns
t2	SA stable to command active		160		ns
t3	BALE pulse width		35		ns
t4	LA hold from BALE inactive		40		ns
t5a	SA hold from command inactive write		50		ns
t5b	SA hold from command inactive read		0		ns
t6	BALE inactive to command active			140	ns
t7a	$\overline{\text{MEMW}}$ command pulse width		500		ns
t7b	$\overline{\text{MEMR}}$ command pulse width		550		ns
t8a	$\overline{\text{MEMW}}$ active to IOCHRDY inactive			340	ns
t8b	$\overline{\text{MEMR}}$ active to IOCHRDY inactive			340	ns
t9a	$\overline{\text{MEMW}}$ hold from IOCHRDY active			110	ns
t9b	$\overline{\text{MEMR}}$ hold from IOCHRDY active			160	ns
t10	RDDATA setup to command inactive		40		ns
t11	RDDATA hold from command inactive		0		ns
t12	WRDATA setup to command inactive		300		ns
t13	WRDATA hold from command inactive		50		ns
t14	$\overline{\text{DBUFOE}}$ active from command			5	ns
t15a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50		ns
t15b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2		ns
t16	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$		170		ns
t17	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4		ns
t18	LA stable to SA stable		15		ns
t19	SA stable to BALE inactive		45		ns

Notes:

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State1 Register, Index 62h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

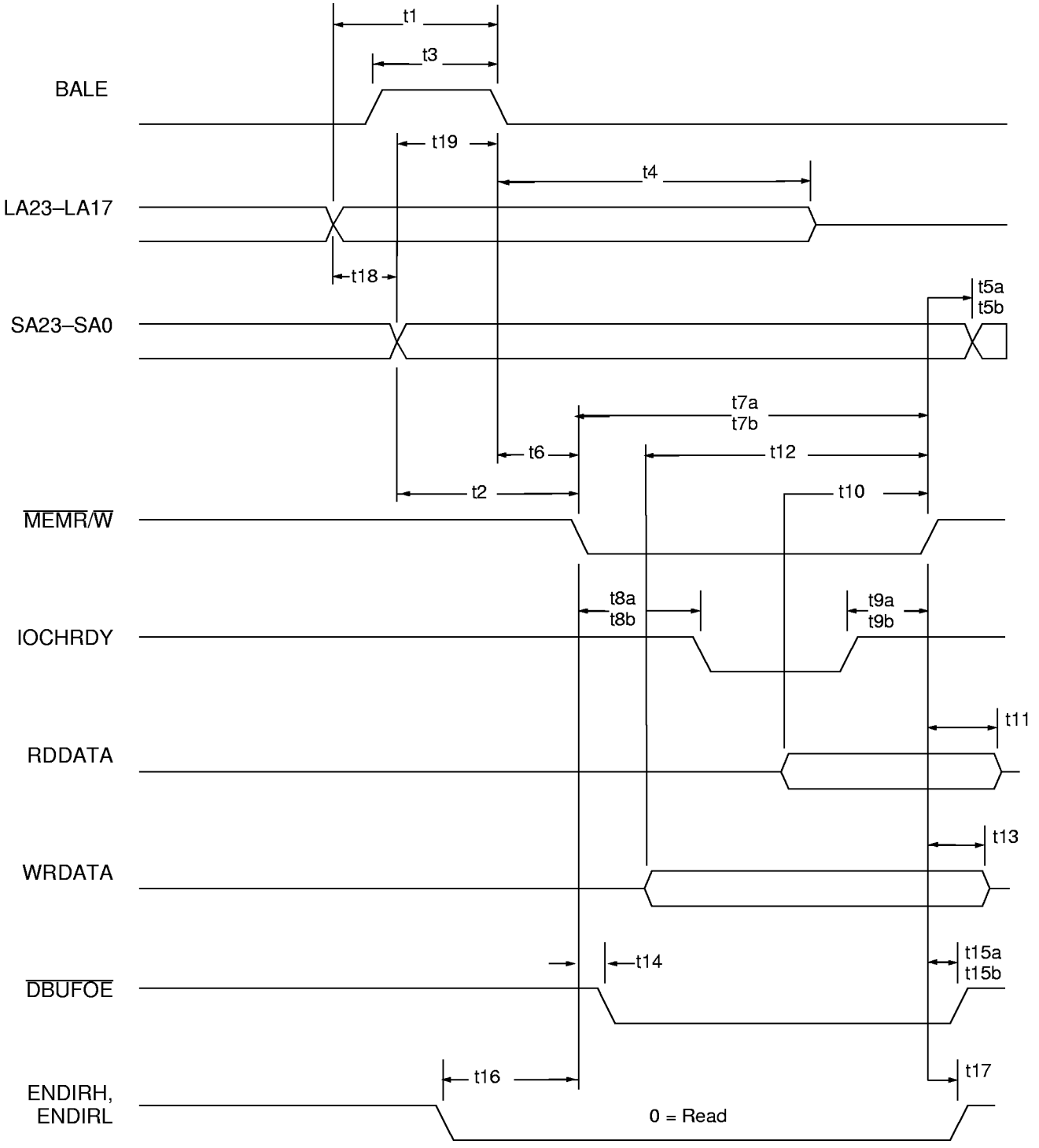


Figure 50. ISA Memory Read/Write 8-Bit Cycle

Table 68. ISA Memory Read/Write 16-Bit Cycle (See Figure 51)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1	LA stable to BALE inactive		60		ns
t2	SA stable to command active		70		ns
t3	BALE pulse width		35		ns
t4	LA hold from BALE inactive		40		ns
t5a	SA hold from command inactive write		50		ns
t5b	SA hold from command inactive read		0		ns
t6	BALE inactive to command active			30	ns
t7a	LA stable to $\overline{\text{MCS16}}$ valid			35	ns
t7b	$\overline{\text{MCS16}}$ hold from LA change		0		ns
t8a	$\overline{\text{MEMW}}$ command pulse width		500		ns
t8b	$\overline{\text{MEMR}}$ command pulse width		550		ns
t9a	$\overline{\text{MEMW}}$ active to IOCHRDY inactive			340	ns
t9b	$\overline{\text{MEMR}}$ active to IOCHRDY inactive			340	ns
t10a	$\overline{\text{MEMW}}$ hold from IOCHRDY active			110	ns
t10b	$\overline{\text{MEMR}}$ hold from IOCHRDY active			160	ns
t11	RDDATA setup to command inactive		25		ns
t12	RDDATA hold from command inactive		0		ns
t13	WRDATA setup to command inactive		330		ns
t14	WRDATA hold from command inactive		50		ns
t15	$\overline{\text{DBUFOE}}$ active from command			5	ns
t16a	$\overline{\text{DBUFOE}}$ hold from command write		50		ns
t16b	$\overline{\text{DBUFOE}}$ hold from command read		–2		ns
t17	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$		50		ns
t18	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4		ns
t19	SA (23:13) stable to $\overline{\text{MCS16}}$ valid			25	ns
t20	LA stable to SA stable		15		ns
t21	SA stable to BALE inactive		45		ns

Notes:

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State 1 Register, Index 62h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

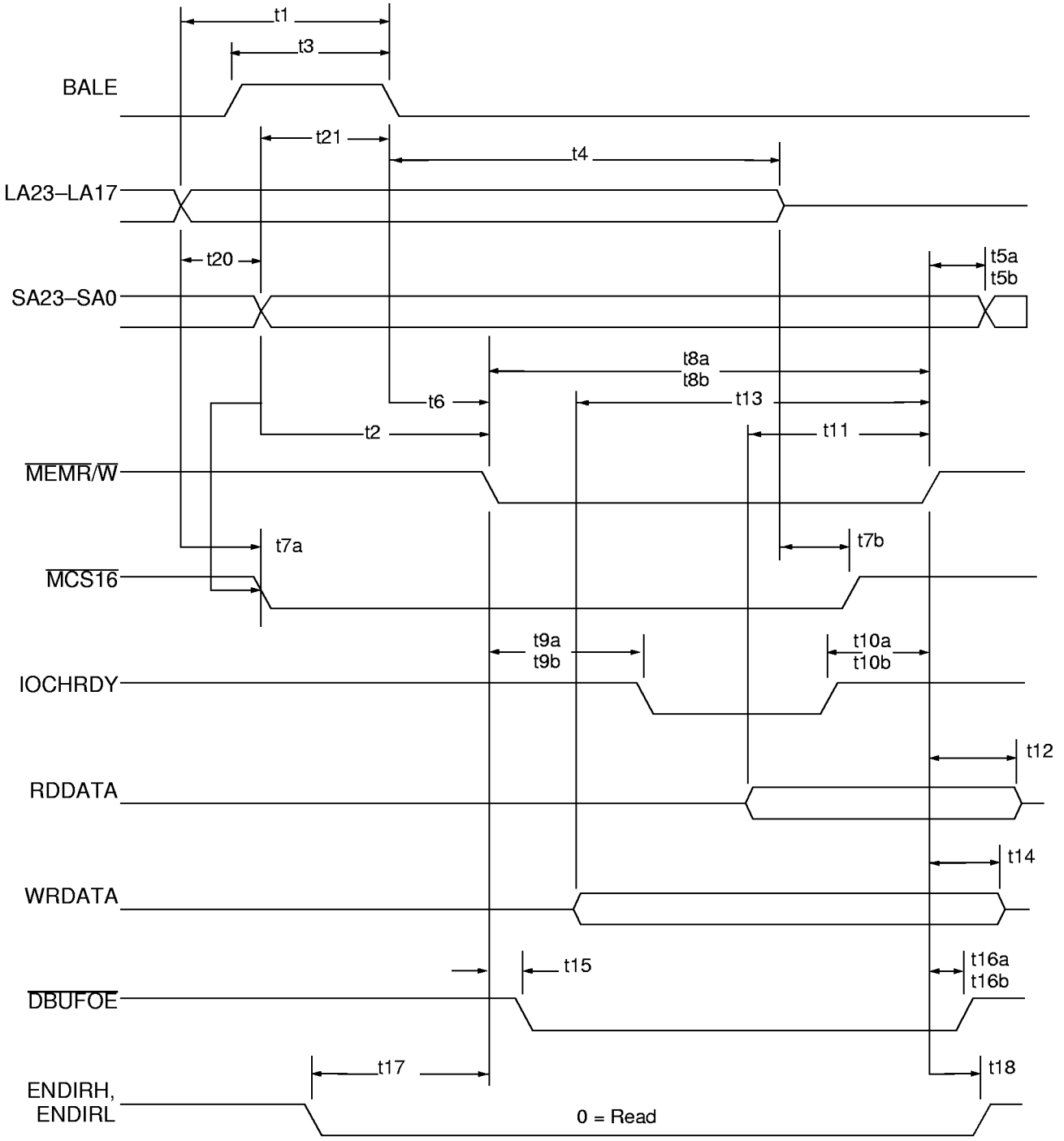


Figure 51. ISA Memory Read/Write 16-Bit Cycle

Table 69. ISA Memory Read/Write 0 Wait State Cycle (See Figure 52)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1	LA stable to BALE inactive		60		ns
t2	SA stable to command active		70		ns
t3	BALE pulse width		35		ns
t4	LA hold from BALE inactive		40		ns
t5a	SA hold from command inactive write		0		ns
t5b	SA hold from command inactive read		0		ns
t6	BALE inactive to command active			30	ns
t7	LA stable to $\overline{\text{MCS16}}$ active			35	ns
t8	Command pulse width		100		ns
t9	Command active to $\overline{\text{0WS}}$ active		0	20	ns
t10	$\overline{\text{0WS}}$ hold from command inactive			40	ns
t11	$\overline{\text{MCS16}}$ hold from LA change		0		ns
t12	RDDATA setup to command inactive		25		ns
t13	RDDATA hold from command inactive		0		ns
t14	WRDATA setup to command inactive		100		ns
t15	WRDATA hold from command inactive	1	–1		ns

Notes:

1. *If the data bus is externally buffered and/or level translated, this write data hold time will be increased by the propagation delay through the buffer and/or the output disable delay of the buffer.*

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State 1 Register, Index 62h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

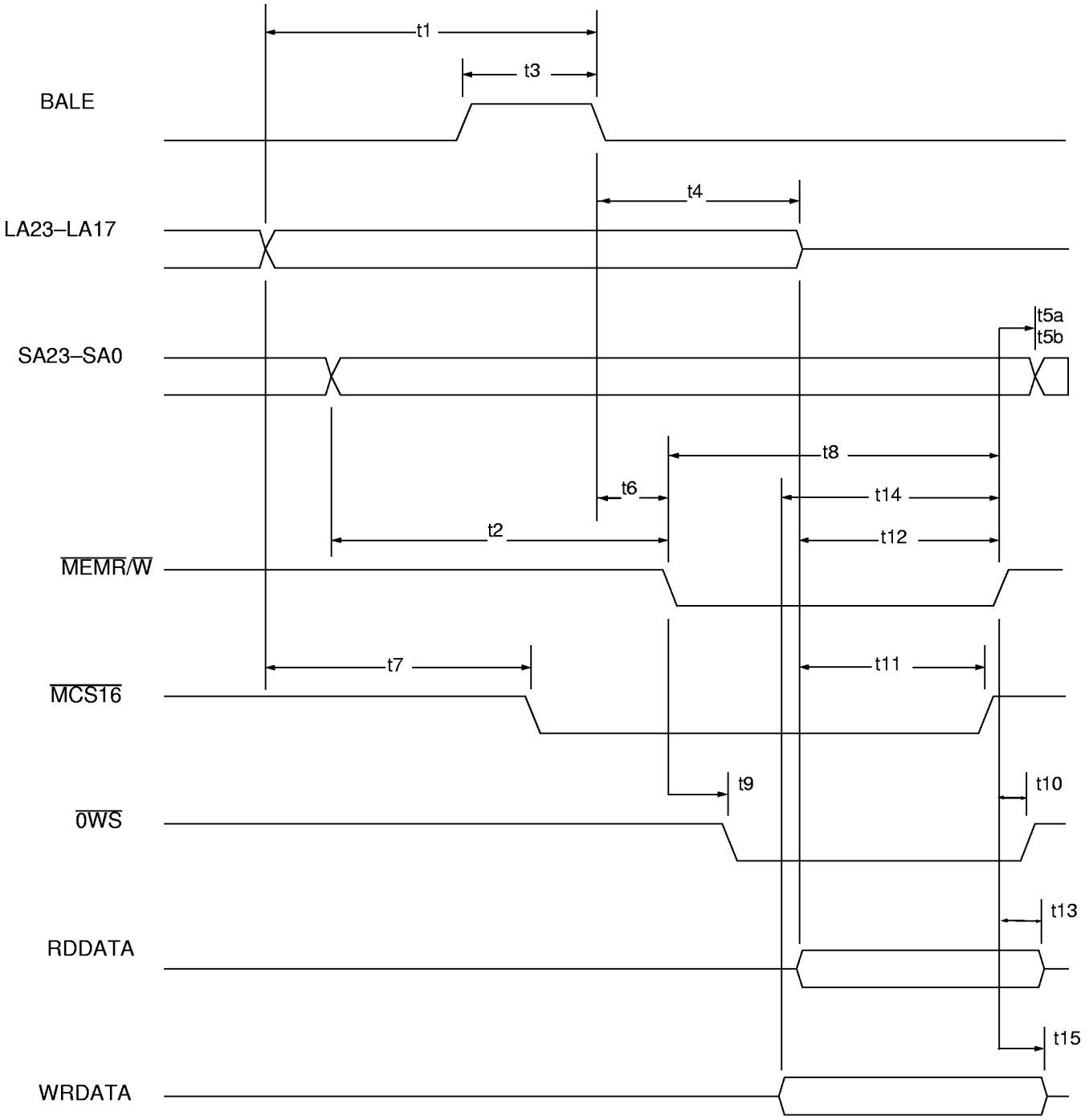


Figure 52. ISA Memory Read/Write 0 Wait State Cycle

Table 70. ISA I/O 8-Bit Read/Write Cycle (See Figure 53)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1a	SA stable to $\overline{IOW}$ active		200		ns
t1b	SA stable to $\overline{IOR}$ active		150		ns
t2a	SA hold from $\overline{IOW}$ inactive		50		ns
t2b	SA hold from $\overline{IOR}$ inactive	1	50		ns
t3a	$\overline{IOW}$ pulse width		450		ns
t3b	$\overline{IOR}$ pulse width	1	505		ns
t4a	$\overline{IOW}$ active to IOCHRDY inactive			300	ns
t4b	$\overline{IOR}$ active to IOCHRDY inactive			350	ns
t5a	$\overline{IOW}$ hold from IOCHRDY active		110		ns
t5b	$\overline{IOR}$ hold from IOCHRDY active		160		ns
t6	RDDATA setup to command inactive		40		ns
t7	RDDATA hold from command inactive		0		ns
t8	WRDATA setup to command inactive		400		ns
t9	WRDATA hold from command inactive		50		ns
t10	$\overline{DBUFOE}$ active from command			5	ns
t11a	$\overline{DBUFOE}$ hold from command write		50		ns
t11b	$\overline{DBUFOE}$ hold from command read	1	50		ns
t12	ENDIRH, ENDIRL setup to $\overline{IOR}$		150		ns
t13	ENDIRH, ENDIRL hold from $\overline{IOR}$	1	50		ns
t14	BALE pulse width		50		ns

Notes:

1. *These timings apply only to the B4 version of the ÉlanSC300 microcontroller. The timings for the B3 version are t2b = 0 ns, t3b = 550 ns, t11b = -2 ns, and t13 = -4 ns.*

These timings may be modified via the MMS Memory Wait State 1 Register, Index 62h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual*, order #18470.)*

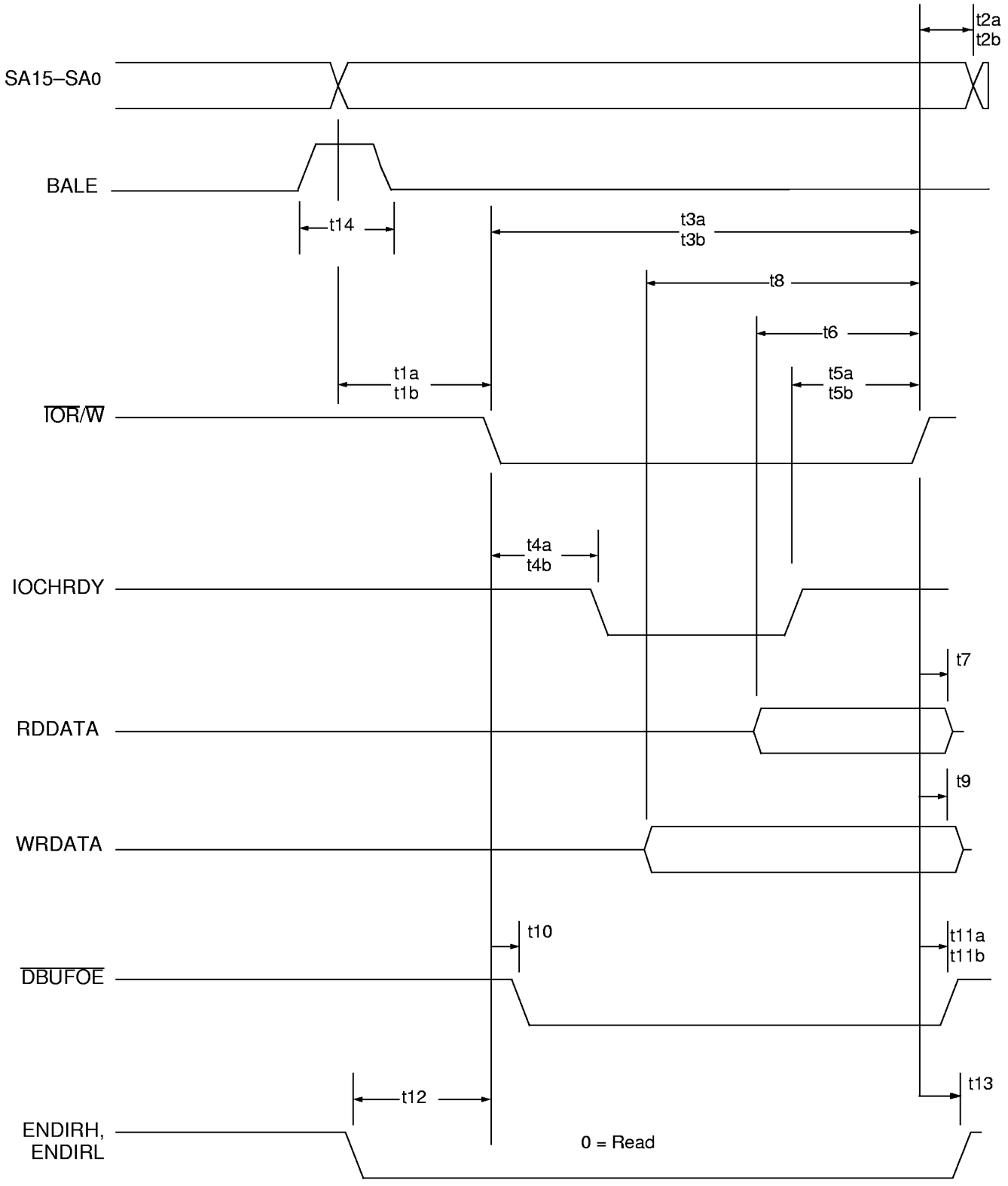


Figure 53. ISA I/O 8-Bit Read/Write Cycle

Table 71. ISA I/O 16-Bit Read/Write Cycle (See Figure 54)

Symbol	Parameter Description	Notes	Preliminary		Units
			Min	Max	
t1a	SA stable to $\overline{IOW}$ active		200		ns
t1b	SA stable to $\overline{IOR}$ active		150		ns
t2	SA stable to $\overline{IOCS16}$ active			95	ns
t3a	$\overline{IOW}$ active to IOCHRDY inactive			30	ns
t3b	$\overline{IOR}$ active to IOCHRDY inactive			80	ns
t4a	$\overline{IOW}$ hold from IOCHRDY active		110		ns
t4b	$\overline{IOR}$ hold from IOCHRDY active		160		ns
t5a	$\overline{IOW}$ pulse width		160		ns
t5b	$\overline{IOR}$ pulse width	1	225		ns
t6a	SA hold from $\overline{IOW}$ inactive		50		ns
t6b	SA hold from $\overline{IOR}$ inactive	1	50		ns
t7	RDDATA setup to command inactive		40		ns
t8	RDDATA hold from command inactive		0		ns
t9	WRDATA setup to command inactive		250		ns
t10	WRDATA hold from command inactive		50		ns
t11	$\overline{DBUFOE}$ active from command			5	ns
t12a	$\overline{DBUFOE}$ hold from command write		50		ns
t12b	$\overline{DBUFOE}$ hold from command read	1	50		ns
t13	ENDRIH, ENDIRL setup to $\overline{IOR}$		100		ns
t14	ENDIRH, ENDIRL hold from $\overline{IOR}$	1	50		ns
t15	BALE pulse width		50		ns

Notes:

1. *These timings apply to the B4 version of the ÉlanSC300 microcontroller only. The timings for the B3 version are t5b = 260, t6b = 0, t12b = -2 ns, and t14 = -4 ns.*

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State1 Register, Index 62h, and the Command Delay Register, Index 60h. (See the Élan™SC300 Microcontroller Programmer's Reference Manual, *order #18470.)*

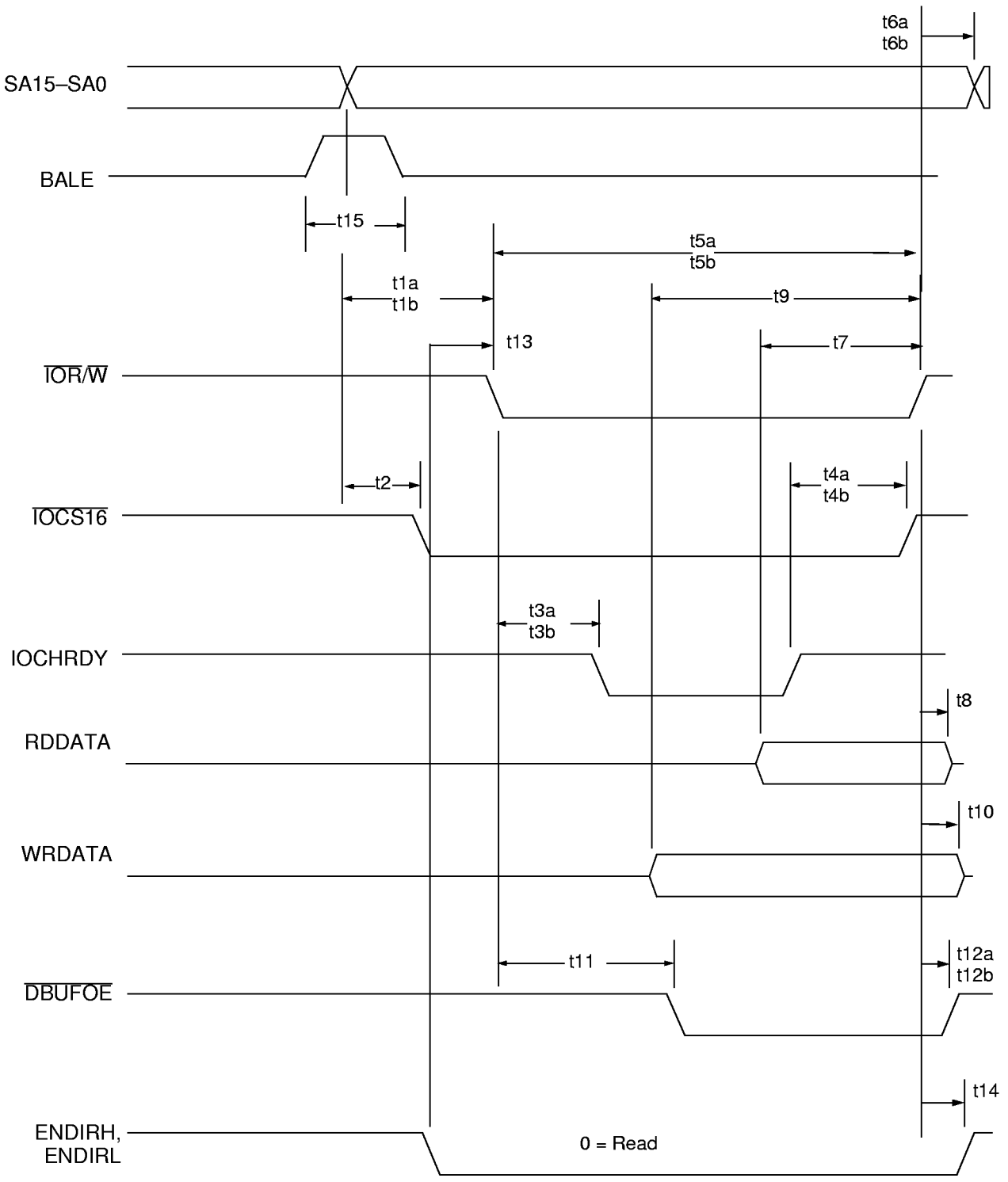


Figure 54. ISA I/O 16-Bit Read/Write Cycle

Table 72. EPP Data Register Write Cycle (See Figure 55)

Symbol	Parameter Description	Max	Min	Unit
t0	$\overline{AFDT}$ delay from $\overline{IOW}$ active	8.4	4.9	ns
t1	$\overline{AFDT}$ delay from $\overline{PPDCS}$ active	1.8	1.1	ns
t2	$\overline{AFDT}$ delay from $\overline{PPOEN}$ active	1.0	0.8	ns
t3	$\overline{AFDT}$ active pulse width (no wait states added)	450	448	ns
t4	$\overline{AFDT}$ High to Low recovery	1000		ns
t5	$\overline{AFDT}$ Low to $\overline{STRB}$ Low	–0.2		ns
t6	$\overline{STRB}$ delay from $\overline{PPDCS}$ active	1.6	0.9	ns
t7	$\overline{STRB}$ delay from $\overline{PPOEN}$ active	0.8	0.6	ns
t8	$\overline{AFDT}$ High to $\overline{STRB}$ High delay	–2.4	–1.4	ns
t9	$\overline{STRB}$ Low to data valid delay	3.7		ns
t10	$\overline{STRB}$ High to data valid hold		4.0	ns
t11	$\overline{PPOEN}$ delay from $\overline{IOW}$ active	7.4		ns
t12	$\overline{PPOEN}$ delay from $\overline{IOW}$ inactive		1.1	ns
t13	$\overline{PPDCS}$ delay from $\overline{IOW}$ active	6.6		ns
t14	$\overline{PPDCS}$ delay from $\overline{IOW}$ inactive		4.3	ns
t15	$\overline{AFDT}$ hold from BUSY High	139	129	ns
t16	BUSY Low delay from $\overline{AFDT}$ active	307		ns

Notes:

The appropriate timings above are valid for the Bidirectional Parallel Port mode also. Timings t13 and t14 are also valid for the Unidirectional Parallel Port mode. ($\overline{PPDCS}$ is $\overline{PPWDE}$ in Unidirectional mode.)

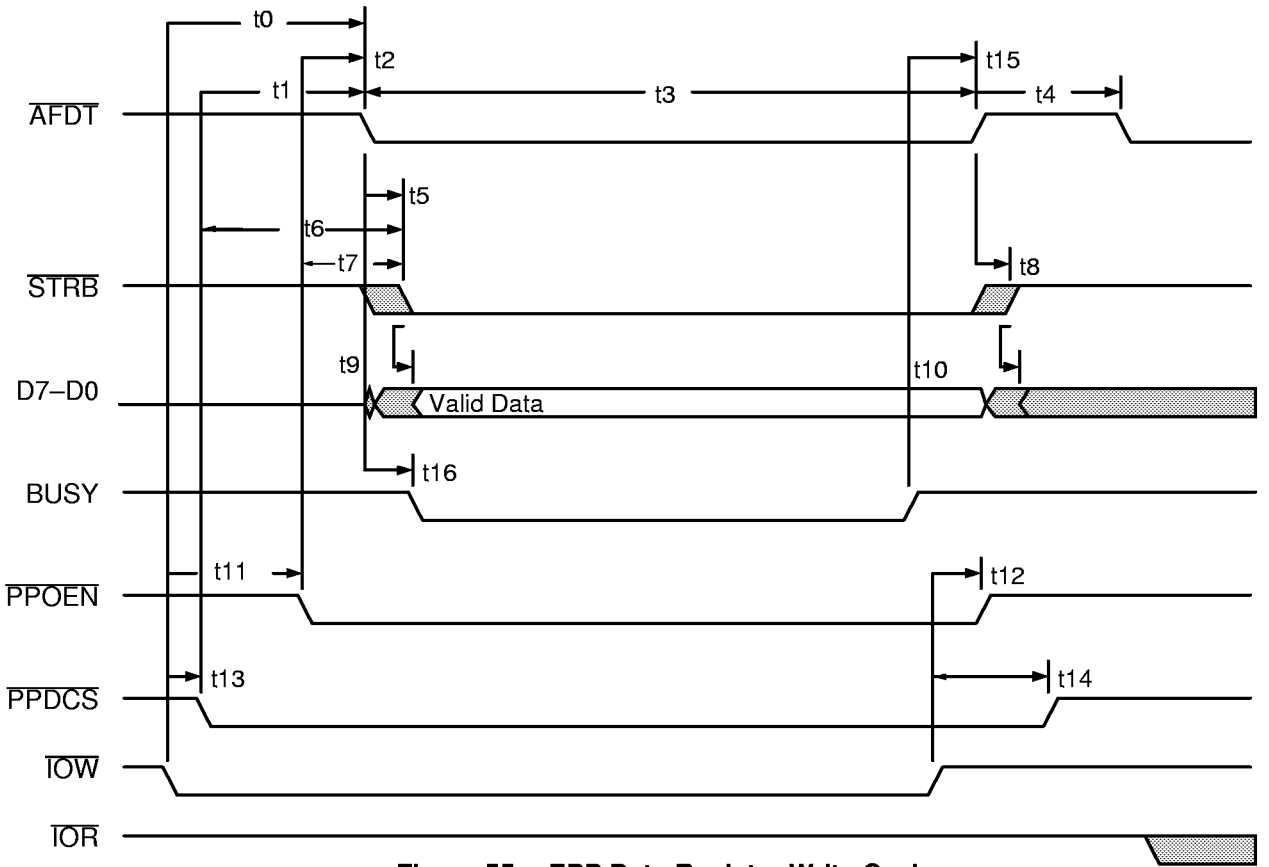


Figure 55. EPP Data Register Write Cycle

Table 73. EPP Data Register Read Cycle (See Figure 56)

Symbol	Parameter Description	Max	Min	Unit
t1	$\overline{AFDT}$ delay from $\overline{PPDCS}$ active	1.8	1.1	ns
t2	$\overline{AFDT}$ active pulse width (no wait states)	450	448	ns
t3	$\overline{AFDT}$ High to Low recovery	1000		ns
t4	Read data valid delay	25.3		ns
t5	Read data hold time		2.3	ns
t6	$\overline{PPDCS}$ delay from $\overline{IOR}$ active	6.8		ns
t7	$\overline{PPDCS}$ delay from $\overline{AFDT}$ inactive	3.7	1.8	ns
t8	$\overline{PPDCS}$ delay from $\overline{IOR}$ inactive		4.2	ns
t9	BUSY (inactive) hold from $\overline{AFDT}$ High		0	ns

Notes:
The appropriate timings above are also valid for the Bidirectional Parallel Port mode.

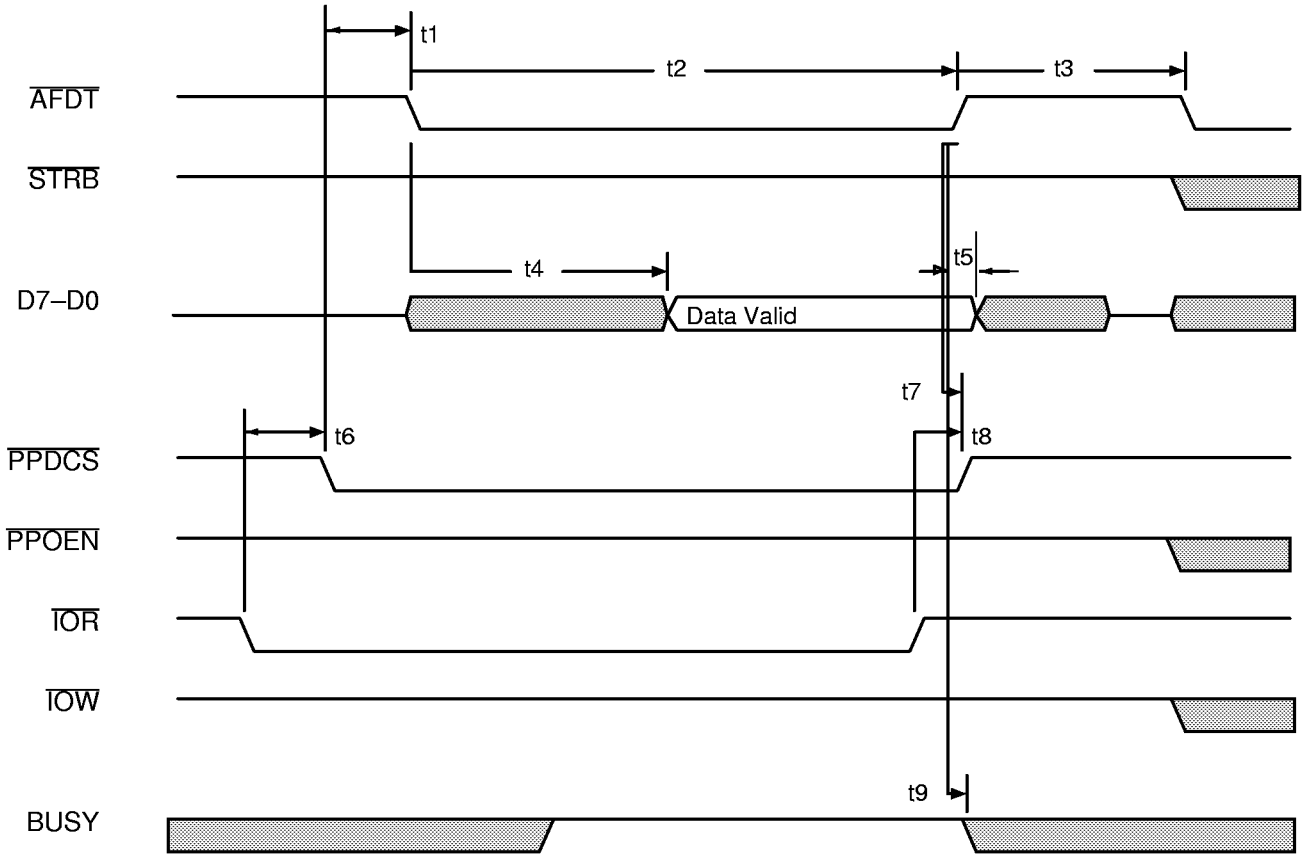
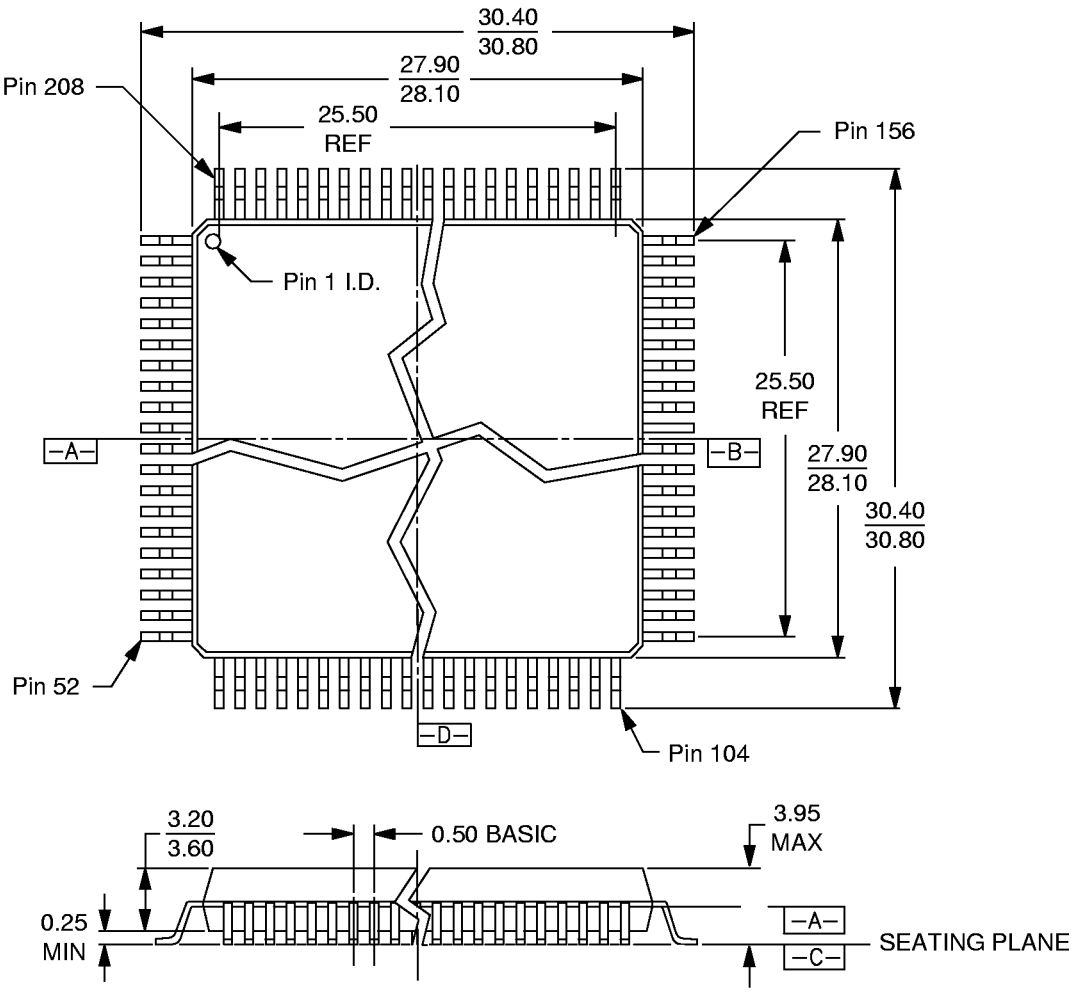


Figure 56. EPP Data Register Read Cycle

PHYSICAL DIMENSIONS

PQR 208, Trimmed and Formed

Plastic Shrink Quad Flat Pack (QFP)

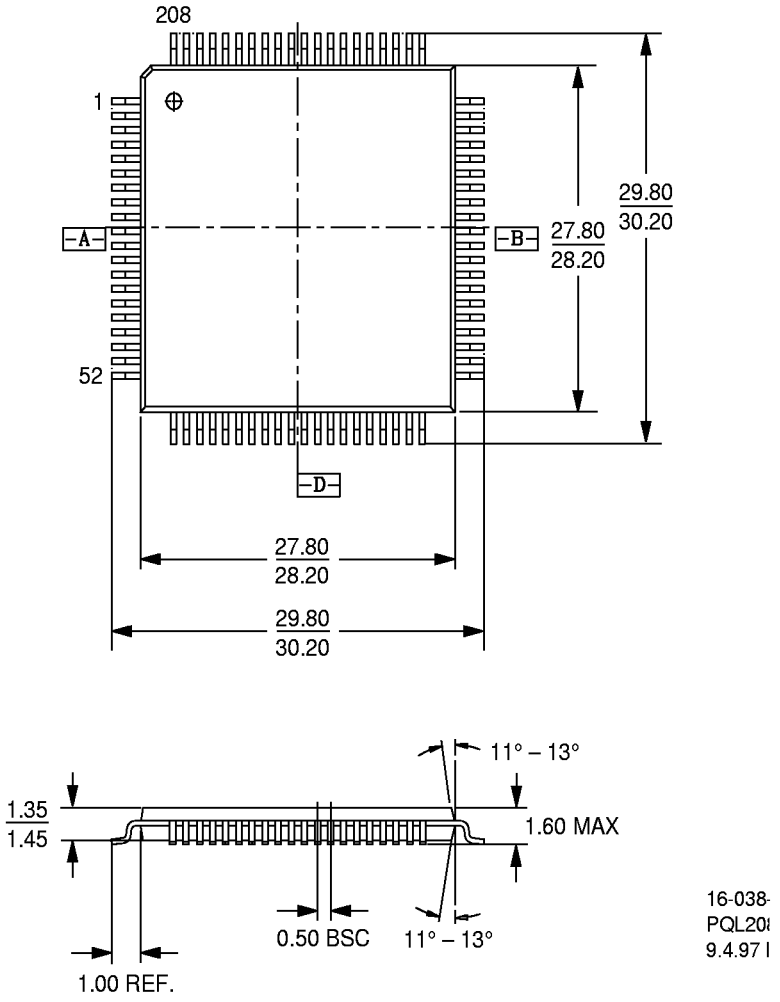


Notes:

1. *All measurements are in millimeters unless otherwise noted.*
2. *Not to scale. For reference only.*

PHYSICAL DIMENSIONS (CONTINUED)

PQL 208, Trimmed and Formed
Thin Quad Flat Pack (TQFP)



Notes:

1. *All measurements are in millimeters unless otherwise noted.*
2. *Not to scale. For reference only.*