

74AC/ACT11819

8-Bit Diagnostic/Pipe-Line Register with Parity Even Output

Objective Specification

ACL Products

FEATURES

- High-speed 8-bit parallel Output Register
- Serial shadow register with right-shift only
- Provides even-parity output
- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11819 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11819 is a high-speed, general purpose pipeline register with a parity even output and an on-board diagnostic register for performing serial register diagnostics and write control store applications.

The D_n to Q_n path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V}$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay PCP to Q_n	$C_L = 50\text{pF}$	5.4	5.6	ns
C_{PD}	Power dissipation capacitance ¹	$f = 1\text{MHz};$ Enabled	17	17	pF
		$C_L = 50\text{pF};$ Disabled	6	6	
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4.5	4.5	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; Disabled	10	10	pF
C_{IO}	I/O capacitance	$V_{IO} = 0\text{V}$ or V_{CC} ; Disabled	12	12	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	$C_L = 50\text{pF}; V_{CC} = 5.5\text{V}$	100	100	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

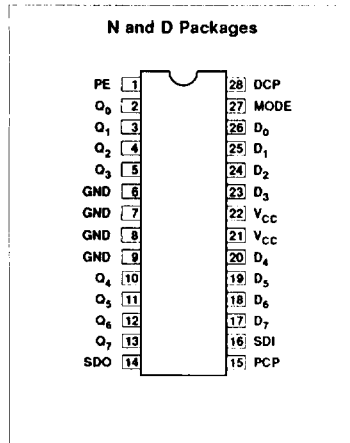
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

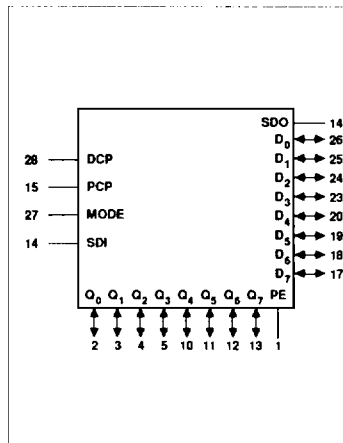
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11819N 74ACT11819N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11819D 74ACT11819D

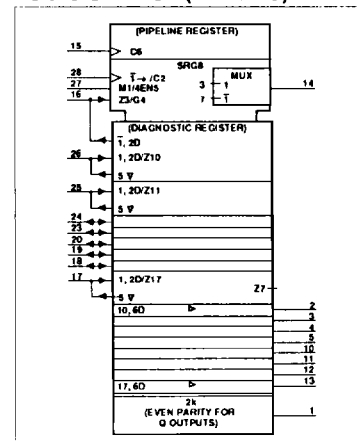
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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can load parallel data to the pipeline register and can output data through the D_n I/O port.

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Q_n port or adjacent bits in the diagnostic register to operate as a right-

shift-only shift register. This register can then participate in a serial loop throughout the system where normal data, address, status, and control registers are replaced with the 74AC/ACT11819 Diagnostic Pipe-Line Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then

after a specified number of clock cycles, the data clocked out can be compared to the expected results. Write control store loading can be accomplished using the same technique. An instruction word can be serially shifted into the diagnostic register and written into a write control store RAM by enabling the D_n outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	DCP	Data (diagnostic register) clock
15	PCP	Pipe-line (output register) clock
27	MODE	Mode control input
16	SDI	Serial data control input
14	SDO	Serial data output
1	PE	Parity Even output
26, 25, 24, 23, 20, 19, 18, 17	$D_0 - D_7$	Data inputs/outputs
2, 3, 4, 5, 10, 11, 12, 13	$Q_0 - Q_7$	Data outputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{cc}	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS			OUTPUT AND I/O			STATUS
	SDI	DCP	PCP	SDO	$D_0 - D_7$, PE	$Q_0 - Q_7$	
L	X	↑	X	DR7*	OUTPUT	Z	Serial input, shift right
H	L	↑	X	SDI (L)	OUTPUT	INPUT	Parallel load diagnostic register from $Q_0 - Q_7$
H	L	↑	↑	SDI (L)	OUTPUT	INPUT	Parallel load diagnostic register from pipeline register from $D_0 - D_7$
L X	X L	X X	↑ ↑	DR7*	OUTPUT	INPUT	Load pipeline register from $D_0 - D_7$
L	X	↑	↑	DR7*	OUTPUT	INPUT	Load pipeline register from $D_0 - D_7$ while shifting diagnostic register
H	H	No ↑	↑	SDI (H)	OUTPUT	OUTPUT	Load pipeline register from diagnostic register
H	X	X	X	SDI	OUTPUT	—	Serial data in to serial data out
H	H	X	X	SDI (H)	OUTPUT	OUTPUT HOLD	Hold diagnostic register, enable $D_0 - D_7$, transitions on DCP ignored
L X	X L	X X	X X	—	OUTPUT	Z	Disable $D_0 - D_7$ outputs

H = High voltage level

L = Low voltage level

↑ = Low-to-High clock transition

No ↑ = Don't allow Low-to-High clock transition

X = Don't care

Z = High-impedance state

* Internal node corresponding to the 8th bit of the Diagnostic Register

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11819			74ACT11819			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11819				74ACT11819				UNIT	
				T _A = +25°C		T _A = -40°C to +85°C		T _A = +25°C		T _A = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
				3.0	2.58		2.48						
													4.5
5.5	4.94		4.8		4.94		4.8						
								5.5			3.85		
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
				3.0	0.36		0.44						
													4.5
5.5		0.36		0.44		0.36		0.44					
									5.5			1.65	
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		±5.0		±0.5		±5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.