FAIRCHILD
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μA55107A • μA75107A
μA75107B • μA75108B
Dual Line Receivers

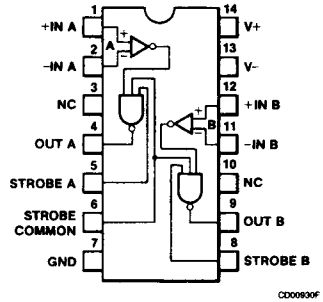
Linear Division Interface Products

Description

The devices in this series are high speed, two channel line receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3.0 V but can be increased to ±15 V by the use of input attenuators. Separate or common strobes are available. The μA55107A/μA75107A circuits feature an active pull-up (totem-pole output). The μA75108B circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the μA55110A/μA75110A line drivers. These line receivers are useful in high speed balanced, unbalanced and party-line transmission systems and as data comparators.

- **High Speed**
- **Standard Supply Voltages**
- **Dual Channels**
- **High Common Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Input Common Mode Voltage Range Of ±3.0 V**
- **Separate Or Common Strobes**
- **Wired-OR Output Capability**
- **High DC Noise Margins**
- **Strobe Input Clamp Diodes**
- **Input Is Diode Protected Against Power-Off Loading On B Version Devices**

Connection Diagram
14-Lead DIP and SO-14 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA55107ADM	6A	Ceramic DIP
μA75107ADC	6A	Ceramic DIP
μA75107APC	9A	Molded DIP
μA75107ASC	KD	Molded Surface Mount
μA75107BDC	6A	Ceramic DIP
μA75107BPC	9A	Molded DIP
μA75107BSC	KD	Molded Surface Mount
μA75108BPC	9A	Molded DIP
μA75108BSC	KD	Molded Surface Mount

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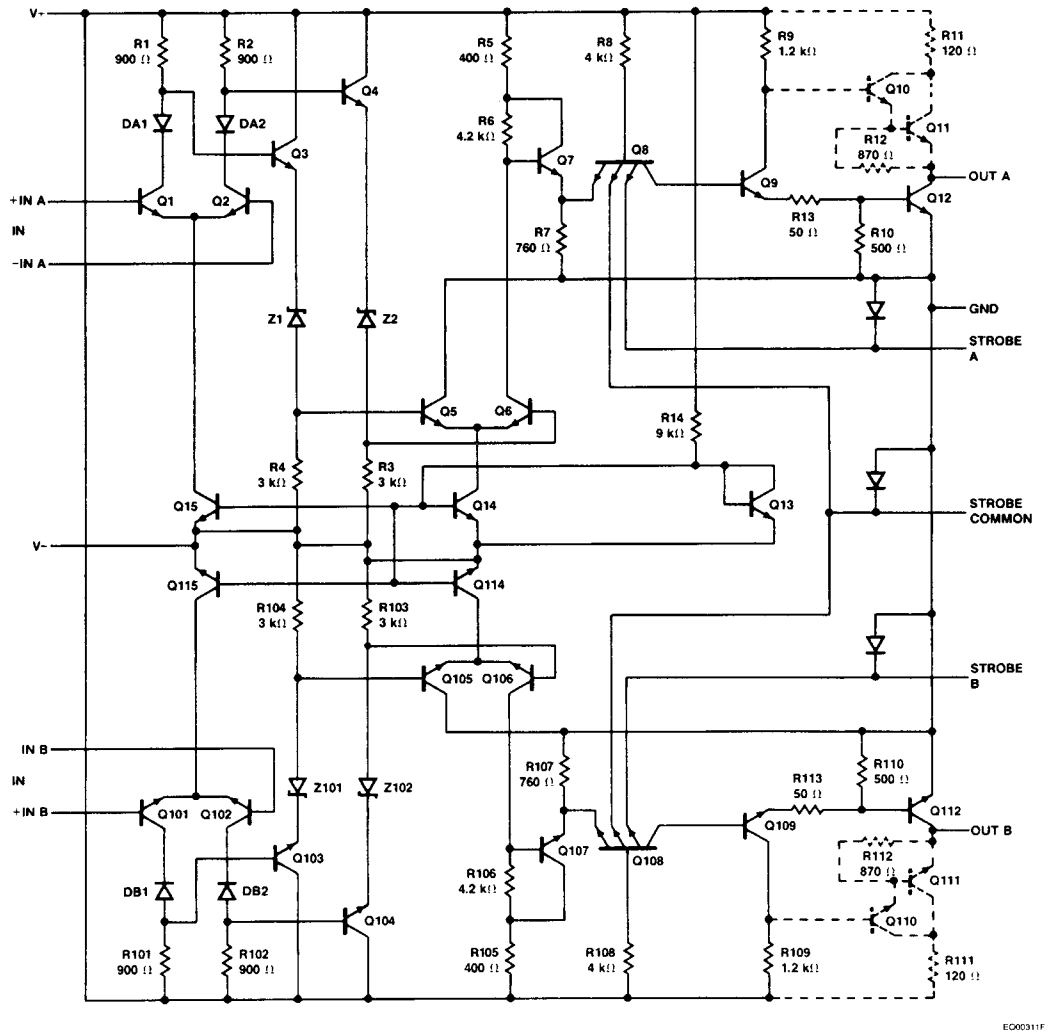
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	
Extended (μA55107A)	−55°C to +125°C
Commercial (μA75107A/B, μA75108B)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage[3]	±7.0 V
Differential Input Voltage[4]	±6.0 V
Common Mode Input Voltage[3]	±5.0 V
Strobe Input Voltage[3]	5.5 V

Notes

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP and SO-14.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. These voltages are with respect to network ground terminal.
4. These voltages are at the noninverting (+) terminal with respect to the inverting (−) terminal.

Equivalent Circuit

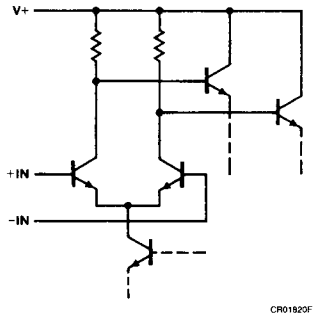


Note
Components shown with dashed lines are applicable to the μA55107A and μA75107B only. See description for differences between A and B versions.

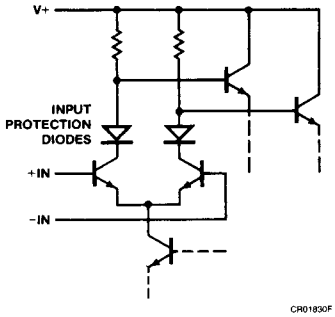
Circuit Differences Between A and B Versions

The essential difference between the μA55107A/μA75107A and μA75107B versions is shown in the following schematics of the input stage:

A Version

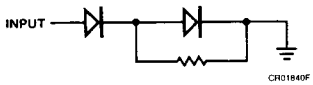


B Version

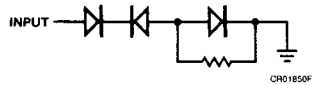


The input protection diodes are useful in certain party-line systems which may have multiple V + power supplies and, in which case, may be operated with some of the V + supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

A Version



B Version

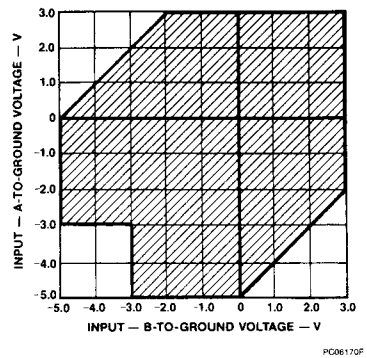


This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4 V. Since this is not a widespread application problem, both the A and B versions will be available. The ratings and characteristic specifications of the B versions are the same as those of the A versions.

Truth Table

Differential Inputs A-B	Strobes G	Strobes S	Output
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

Recommended Combinations of Input Voltage for Line Receivers



μA55107A, μA75107A, μA75107B
Electrical Characteristics Over recommended operating temperature range with V+ = Max and V– = Max, unless otherwise specified.[1, 3]

DC Characteristics

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
I_{IH}	Input Current HIGH	V_{DIFF} = 0.5 V, V_{CM} = −3.0 V to +3.0 V			30	75	μA
I_{IL}	Input Current LOW	V_{DIFF} = −2.0 V, V_{CM} = −3.0 V to +3.0 V				−10	μA
$I_{IH(G)}$	Gate Input Current HIGH	$V_{(G)}$ = 2.4 V				40	μA
		$V_{(G)}$ = V+				1.0	mA
$I_{IL(G)}$	Gate Input Current LOW	$V_{(G)}$ = 0.4 V				−1.6	mA
$I_{IH(ST)}$	Strobe Input Current HIGH	$V_{(ST)}$ = 2.4 V				80	μA
		$V_{(ST)}$ = V+				2.0	mA
$I_{IL(ST)}$	Strobe Input Current LOW	$V_{(ST)}$ = 0.4 V				−3.2	mA
V_{OH}	Output Voltage HIGH	I_{OH} = −400 μA, V_{CM} = −3.0 V to +3.0 V	V_{CC} = Min	2.4			V
V_{OL}	Output Voltage LOW	I_{OL} = 16 mA, V_{CM} = −3.0 V to +3.0 V	V_{CC} = Min			0.4	V
I_{OS}	Output Short Circuit Current[2]	V_O = 0 V		−18		−70	mA
I+	Positive Supply Current	$V_O = V_{OH}$, I_{OH} = 0 V, T_A = 25°C			18	30	mA
I–	Negative Supply Current	$V_O = V_{OH}$, I_{OH} = 0 V, T_A = 25°C			−8.4	−15	mA

AC Characteristics V_{CC} = ±5.0 V, R_L = 390 Ω, C_L = 50 pF, T_A = 25°C. (See Test Circuit)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$t_{PLH(D)}$	Propagation Delay Time			17	25	ns
$t_{PHL(D)}$				17	25	ns
$t_{PLH(S)}$				10	15	ns
$t_{PHL(S)}$				10	15	ns

μA75108B
DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input Current HIGH	V_{DIFF} = 0.5 V, V_{CM} = −3.0 V to +3.0 V		30	75	μA
I_{IL}	Input Current LOW	V_{DIFF} = −2.0 V, V_{CM} = −3.0 V to +3.0 V			−10	μA
$I_{IH(G)}$	Gate Input Current HIGH	$V_{(G)}$ = 2.4 V			40	μA
		$V_{(G)}$ = V+			1.0	mA
$I_{IL(G)}$	Gate Input Current LOW	$V_{(G)}$ = 0.4 V			−1.6	mA
$I_{IH(ST)}$	Strobe Input Current HIGH	$V_{(ST)}$ = 2.4 V			80	μA
		$V_{(ST)}$ = V+			2.0	mA

μA75108B (Cont.)
Electrical Characteristics Over recommended operating temperature range with V+ = Max and V– = Max, unless otherwise specified.[1, 3]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
$I_{IL(ST)}$	Strobe Input Current LOW	$V_{(ST)}$ = 0.4 V				–3.2	mA
V_{OL}	Output Voltage LOW	I_{OL} = 16 mA, V_{CM} = –3.0 V to +3.0 V	V_{CC} = Min			0.4	V
I_{OH}	Output Current HIGH	V_O = V+	V_{CC} = Min			250	μA
I+	Positive Supply Current	$V_O = V_{OH}$, I_{OH} = 0 V, T_A = 25°C			18	30	mA
I–	Negative Supply Current	$V_O = V_{OH}$, I_{OH} = 0 V, T_A = 25°C			–8.4	–15	mA

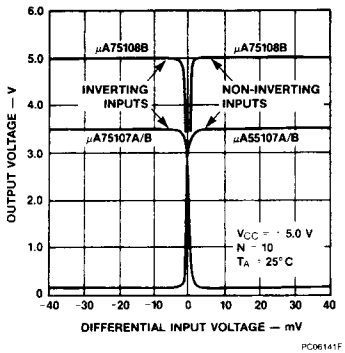
AC Characteristics V_{CC} = ± 5.0 V, R_L = 390 Ω, C_L = 15 pF, T_A = 25°C. (See Test Circuit)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$t_{PLH(D)}$	Propagation Delay Time			19	25	ns
$t_{PHL(D)}$				19	25	ns
$t_{PLH(S)}$				13	20	ns
$t_{PHL(S)}$				13	20	ns

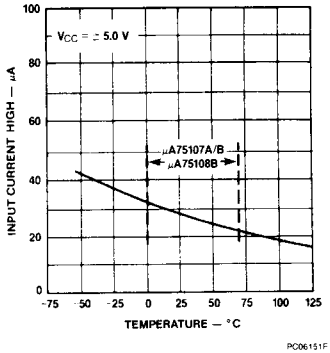
Notes
1. For μA55107A guaranteed supply voltage range is ± 4.5 V to ± 5.5 V and operating temperature range is –55°C ≤ T_A ≤ +125°C. For μA75107A/B and μA75108B guaranteed supply voltage range is ± 4.75 V to ± 5.25 V and operating temperature range is 0°C ≤ T_A ≤ 70°C.
2. Not more than one output should be shorted at a time.
3. V_{CC} Max implies ± 5.5 V or ± 5.25 V, depending on device type.

Typical Performance Curves

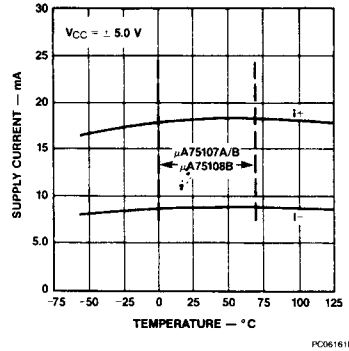
Output Voltage vs Differential Input Voltage



Input Current HIGH Into 1A or 2A vs Ambient Temperature

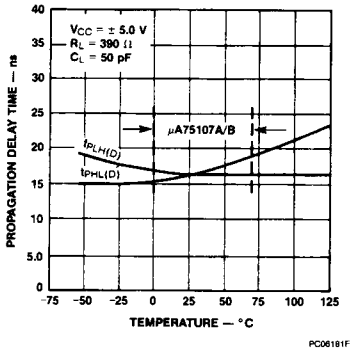


High Logic Level Supply Current vs Ambient Temperature

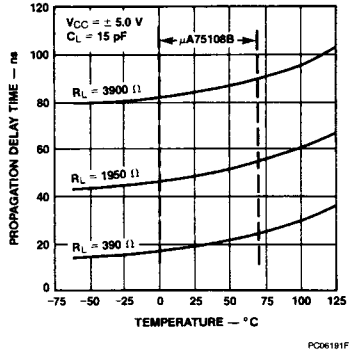


Typical Performance Curves (Cont.)

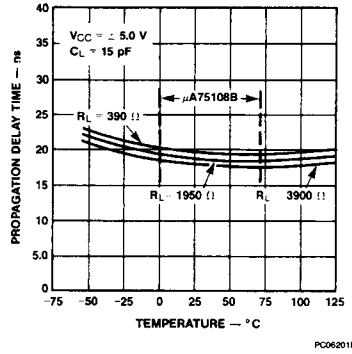
μA55107A, μA75107A/B Propagation Delay Time (Differential Inputs) vs Ambient Temperature



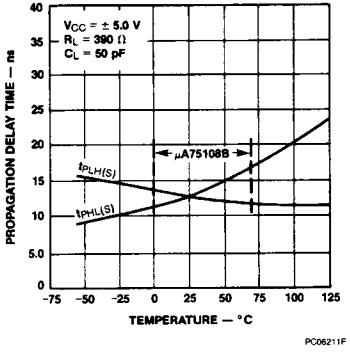
μA75108B Propagation Delay Time LOW-to-HIGH Level vs Ambient Temperature



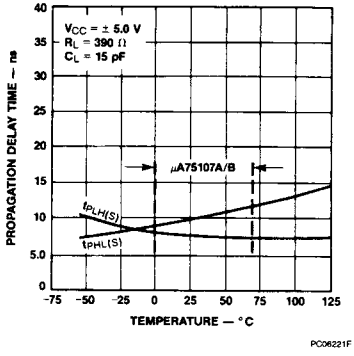
μA75108B Propagation Delay Time HIGH-to-LOW level vs Ambient Temperature



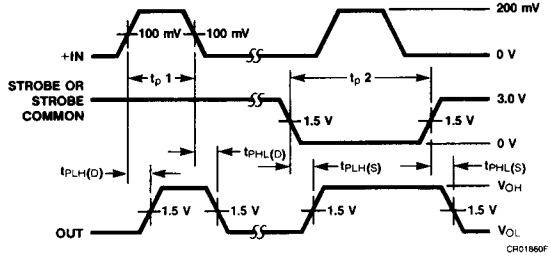
μA75108B Propagation Delay Time (Strobe Inputs) vs Ambient Temperature



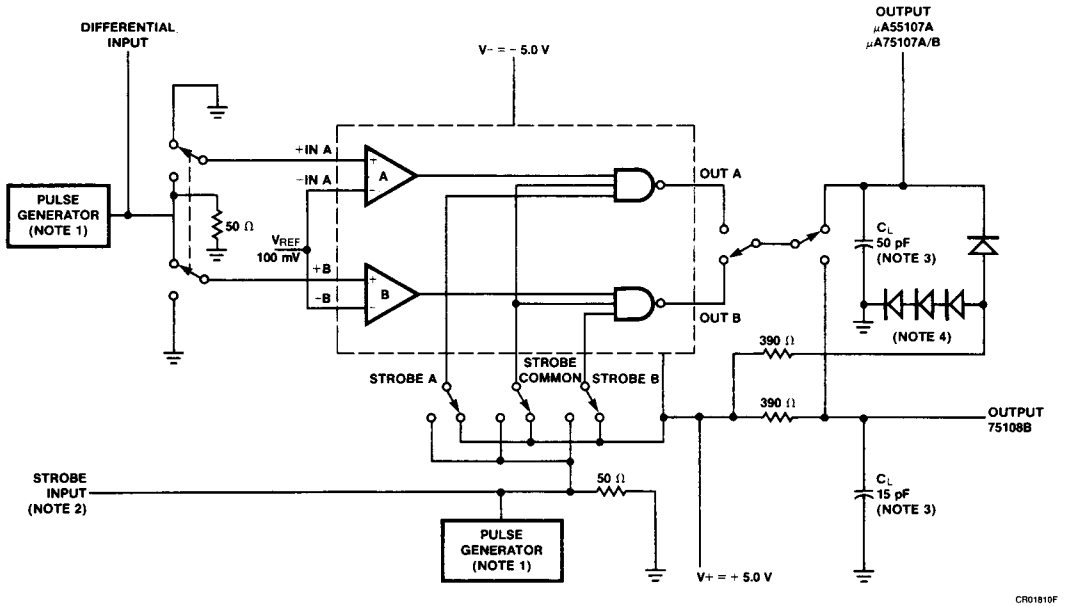
μA55107A, μA75107A/B Propagation Delay Time (Strobe Inputs) vs Ambient Temperature



Voltage Waveforms



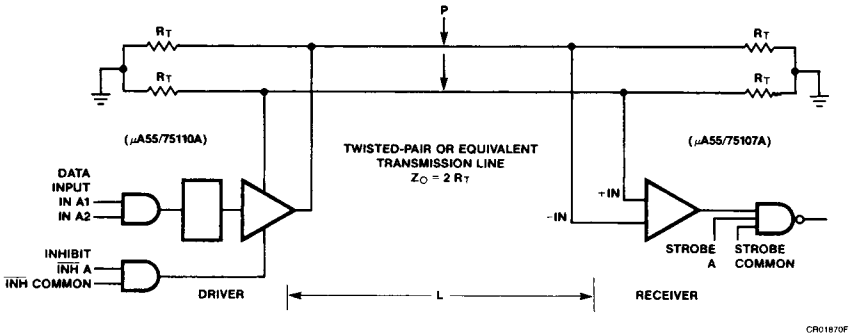
AC Test Circuit



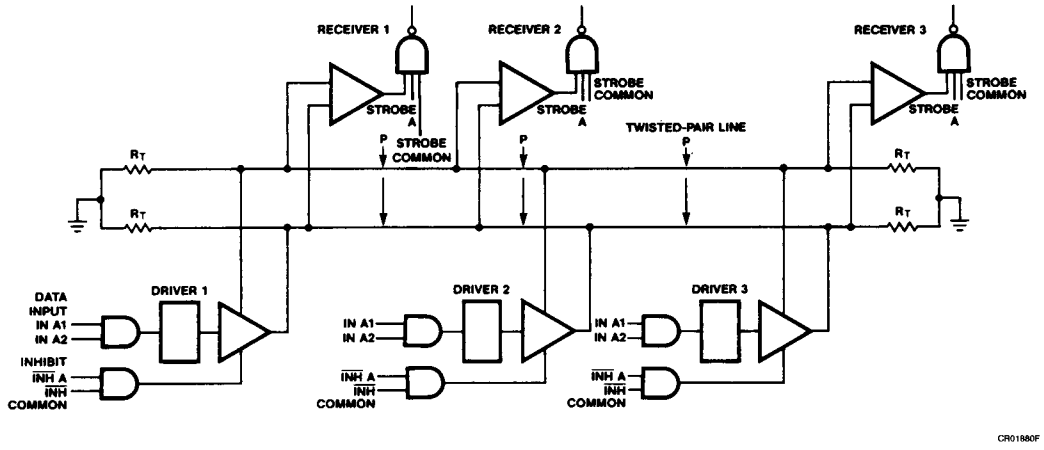
Notes

1. The pulse generators have the following characteristics: $t_r = t_f = 10 \pm 5.0$ ns, $t_{p1} = 500$ ns, PRR = 1.0 MHz, $t_{p2} = 1.0$ μs, PRR = 500 kHz, $Z_O = 50\ \Omega$.
2. Strobe input pulse is applied to Strobe A when inputs A1 – A2 are being tested; to common Strobe when inputs A1 – A2 or B1 – B2 are being tested; and to Strobe B when inputs B1 – B2 are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

Basic Balanced-Line Transmission System



Data-Bus or Party-Line System



Application

The μA55107A, μA75107A dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.
Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver input logic levels. The voltage difference is approximately:

$$V_{DIFF} \simeq 1/2\ I_{O(on)} \cdot R_T \qquad (1)$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

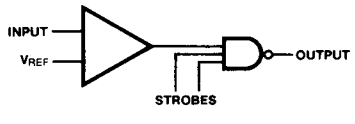
$$V_{DIFF} \simeq I_{O(on)} \cdot R_T \qquad (2)$$

The strobe feature of the receivers and the inhibit feature of the drivers allow the μA55107A, μA75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The μA55107A, μA75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

The μA55107A, μA75107A dual line circuits may also be used in unbalanced or single line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.
The receiver threshold level is established by applying a DC reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so

that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0 V to +3.0 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

Unbalanced or Single-Line Systems



Precautions in the Use of μA55107A, μA75107A and μA75108B Dual Line Receivers

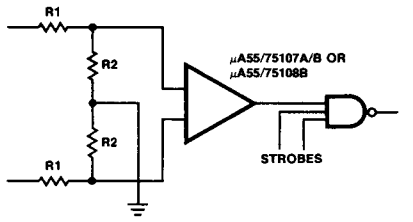
The following precaution should be observed when using or testing μA55107A, μA75107A line circuits.

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

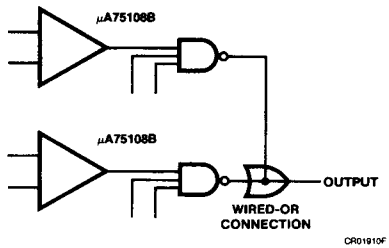
The μA55107A, μA75107A and μA75108B line receivers feature a common mode input voltage range of ±3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common mode range can be extended by the use of external input attenuators. Common mode input voltages can in this way be reduced to ±3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

The μA75108B line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other μA75108B outputs. This allows a level of logic to be implemented without additional logic delay.

Increasing Common Mode Input Voltage Range of Receiver



μA75108B Wired-OR Output Connections



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