11.3Gbps EML Driver with Integrated Micro Controller

M02172
Rev V5

Features

- Data Rates to 11.3Gbps. Single 3.3V supply
- Programmable laser bias current to 150mA
- Programmable laser modulation voltage to 2.5Vpp
- Integrated mode supports SFF-8472/SFP/SFP+ Requirements
- External micro controller mode supports SFF-8472/XFP/SFP/SFP+ requirements
- SFP/XFP compliant safety circuitry
- Provides internal Vcc switch for single point faults
- Supports both CA and CC laser configurations
- Input equalization for SFP+ requirements
- 2-wire or SPI serial interface available
- Programmable GPIO, selectable 6 bit or 10 bit DAC, output offset control via serial interface
- Five user configurable General purpose I/Os
- Two available auxiliary 12 bit ADC inputs
- Provides complete Calibration and Firmware setup
- 86mA typical supply current
- Operating Temperature: -40°C to +95°C
- 5mm x 5mm QFN package

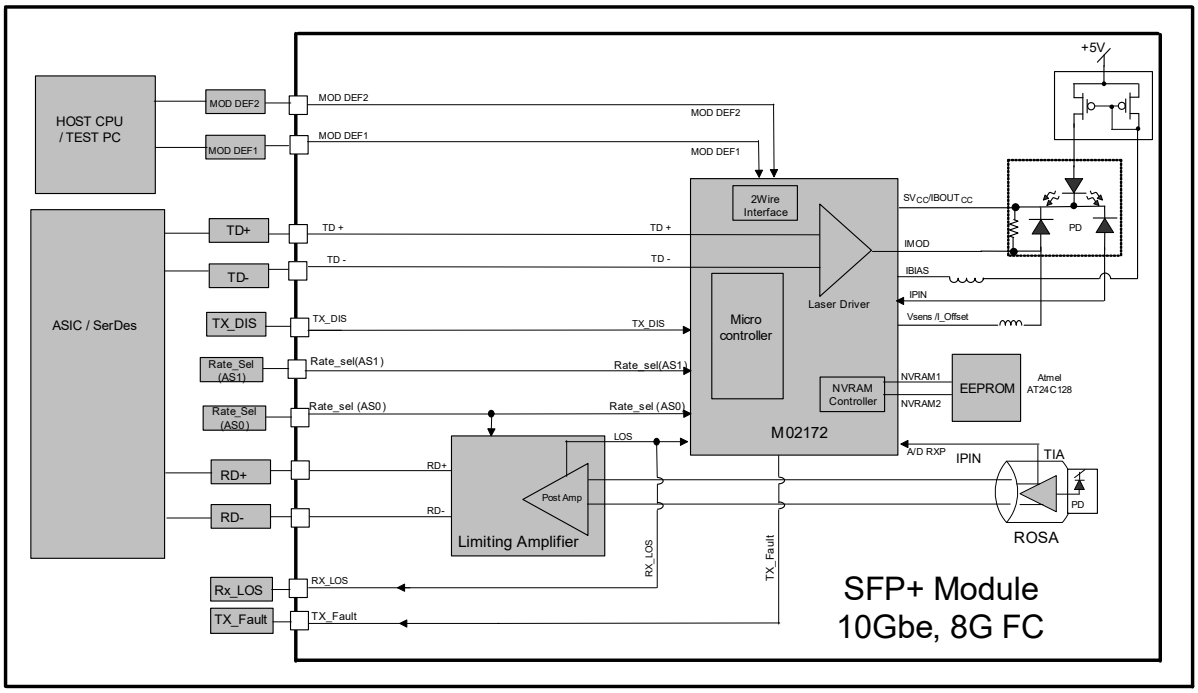
Applications

- IEEE802.3ae 10GBASE-LR
- SFP/SFP+/XFP MSA Modules
- 10 Gigabit Ethernet Modules
- 8G Fiber Channel Modules
- SONET OC-192 Optical Transmitters
- SDH STM-64 Optical Transmitters

The M02172 is designed to drive Electroabsorption Modulated Lasers with a 50Ω characteristic impedance used in Transmitter optical sub-assemblies. In EML applications, the programmable offset adjustment is integrated into the signal output. Output bias (offset) voltage which varies linearly as a function of temperature is provided as required by some EML devices. The M02072 combines a diagnostic monitoring interface compliant with XFP, or SFP+ and a EML driver in a compact 5mm x 5mm QFN package.

Integrated safety circuitry provides latched bias current and modulation voltage shutdown if a fault condition is detected. In addition, external micro mode allows external micro controller to take control of the driver operation, bypassing the internal 8051 micro controller. The device comes with firmware required for diagnostic monitoring, offering a seamless interface for calibration and setup.

M02172 Interface (Integrated Mode) in SFP+ Module



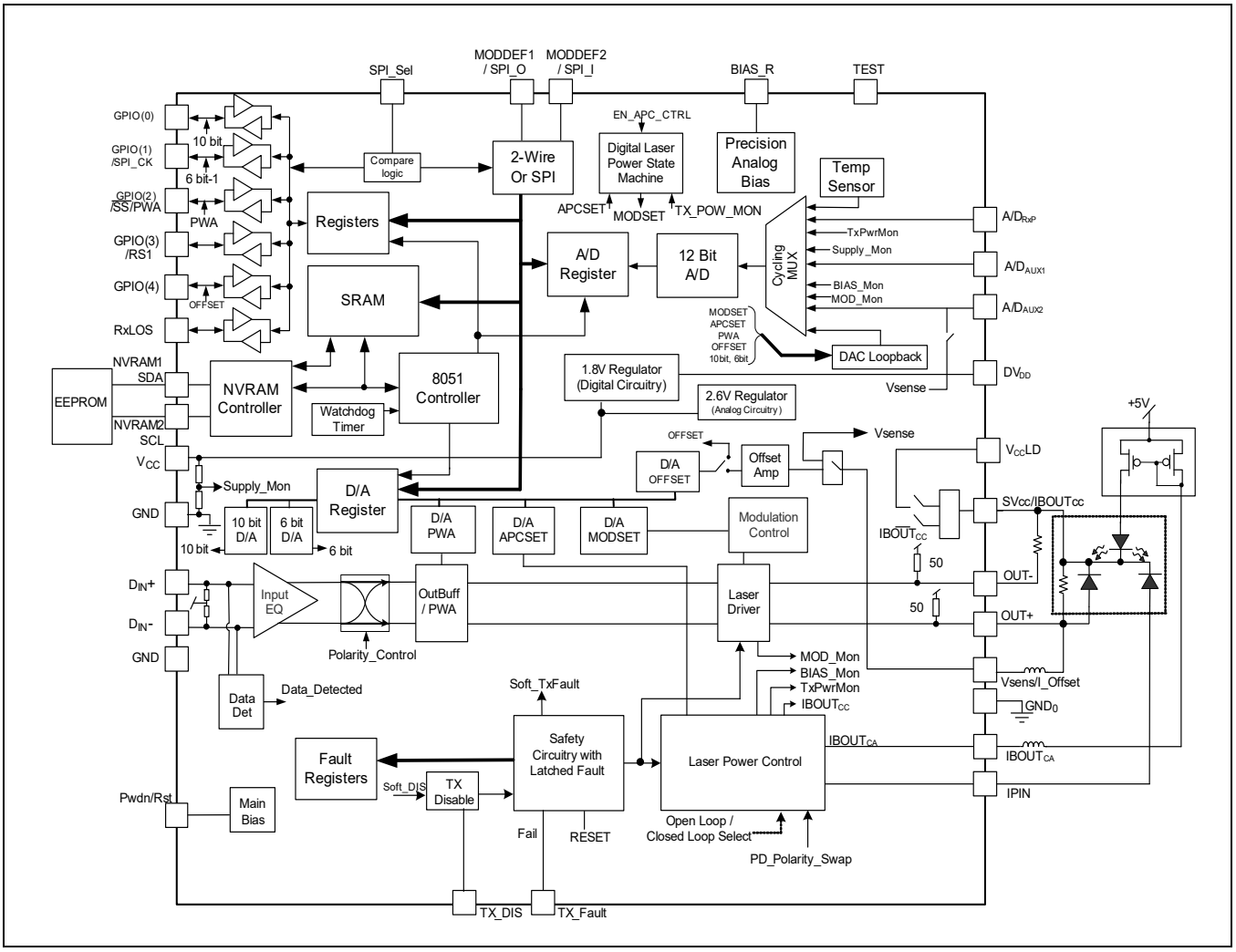
Ordering Information

Part Number	Package	Operating Temperature
M02172G-12*	32 pin, 5mm x 5mm QFN	-40°C to +95°C
*The G in the part number indicates that this is an RoHS compliant package.		

Revision History

Revision	Level	Date	Description
V5	Release	June 2022	Update latched registers information.
V4	Release	March 2022	Add register table to datasheet.
V3	Release	September 2020	Add register information to Pin 27 RxLOS Add register table to datasheet. MKOR package drawing replaced with Unisem. Updated logos and page layout.
E (V2)	Release	December 2010	Update Ordering Information. Remove 8k EEPROM download option as it is not required to meet the SFP t_init and t_serial timing requirements.
D (V1)	Release	June 2009	Final characterization results included in specifications. Applications figure added for Cyotpics 10T3082 EML. Minor corrections made to text explanations.
C (V3A)	Advanced	April 2007	Added SPI, Functional description and Applications Information
B (V2A)	Advanced	March 2007	Changed pins 9, 10 and 29. Updated to meet SFP+ latest Revisions
A (V1A)	Advanced	December 2006	Initial

M02172 Block Diagram



1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	3.3V power supply voltage	-0.4 to +4.0	V
T_A	Operating Ambient Temperature	-40 to +95	°C
T_{STG}	Storage temperature	-65 to +150	°C
$IB_{OUT(MAX)}$	Maximum bias output current at IB_{OUT}	180	mA
$V_{MOD(MAX)}$	Max. modulation voltage	2.5	V_{PP}

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Notes	Rating	Units
Power supply (V_{CC}-GND)		3.3 ± 7.5%	V
Operating ambient	1	-40 to +95	°C
NOTE:			
1. Operating temperature is 95°C for I_{BIAS} = 100mA and 90°C for I_{BIAS} = 150mA			

1.3 DC Characteristics

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C, V_{MOD} = $1V_{pp}$, I_{BIAS} = 40mA, unless otherwise noted.

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Notes	Minimum	Typical	Maximum	Units
V_{CC}	V_{CC} operating voltage			3.05	3.3	3.55	V
I_{CC}	I_{CC} supply current	High-rate mode Low-rate mode Increase due to enabling Pulse Width Adjust	1	– – –	86 80 2	134 – –	mA
I_{CC_DIS}	I_{CC} when part Disabled	Device is disabled		–	36	48	mA
V_{CCTHL}	3.3V supply detection (low voltage) threshold	Minimum of either V_{CC} supply low detection voltage or internal Power on Reset voltage		–	2.6	2.85	V
V_{CCTHH}	3.3V supply detection (high voltage) threshold			3.55	3.8	4.00	V
V_{FAULTL}	Low fault voltage detection threshold ($IBOUT_{CA}$, BIAS_R)	Fault condition occurs when voltage drops below this level		–	400	600	mV
V_{FAULTH}	High fault voltage detection threshold (IBOUTcc)	Fault condition occurs when voltage exceeds this level		V_{CC} - 0.6	V_{CC} - 0.4	–	V
I_{BIAS}	Bias current adjust range	At $IBOUT_{CA}$, $V(IBOUT_{CA})$ > 1.5V At $IBOUT_{CC}$., $V(IBOUT_{CC})$ < 2.5V	2	5	–	150	mA
$I_{BIAS(OFF)}$	Bias current with output disabled	TX_DIS = high and/or SOFT_DIS = high; $V(IBOUT_{CA})$ = V_{CC} for common anode and $V(IBOUT_{CC})$= 0V for common cathode		-	5	150	µA
$BIAS_{RATIO\ CA}$	Ratio of bias current to $BIAS_{MON}$ current in common anode mode	$V(IBOUT_{CA})$ = 1.5V		102	113	124	A/A
$BIAS_{RATIO\ CC}$	Ratio of bias current to $BIAS_{MON}$ current in common cathode mode	$V(IBOUT_{CC})$ = 2.0V		103.5	115	126	A/A
V_{MD}	Monitor diode reverse bias voltage	Minimum is with maximum I_{PIN} current		1.5	2.0	V_{CC}	V
I_{MD}	Monitor diode current adjustment range	For stable APC loop operation		10	–	1400	µA
C_{MDMAX}	Maximum monitor photodiode capacitance	For stable APC loop operation in analog closed mode; includes any additional parasitic capacitance	3	–	–	100	pF
V_{IH_DIS}	TTL/CMOS input high voltage (TX_DIS, Pwdn/Rst, SPI_sel, Test)			2.0	–	V_{CC}	V
V_{IL_DIS}	TTL/CMOS input low voltage (TX_DIS, Pwdn/Rst, SPI_sel, Test)			0	–	0.8	V
V_{IH_IO}	GPIO input high voltage	When configured as a digital input		2.0	–	V_{CC}	V
V_{IL_IO}	GPIO input low voltage			0	–	0.8	V
$I_{LK\_IO\_0-4}$	GPIO 0-4 leakage current	When configured as a tristate digital input		-10	0	10	µA

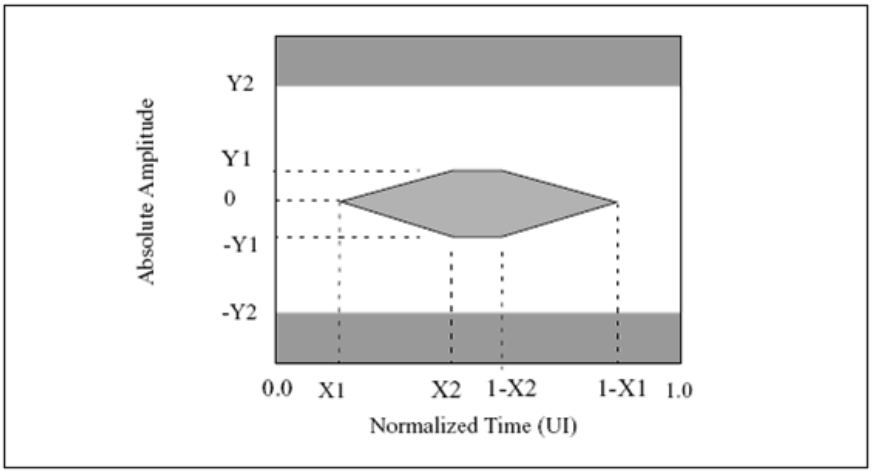
Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Notes	Minimum	Typical	Maximum	Units
V_{IH_LOS}	LOS input high voltage			2.0	–	V_{CC}	V
V_{IL_LOS}	LOS input low voltage			0	–	0.8	V
V_{OH_FAIL}	Logic output high voltage (FAIL)	With external 10kΩ pull-up to V_{CC}		V_{CC} - 0.6	–	–	V
V_{OL_FAIL}	Logic output low voltage (FAIL)	I_{OL} = 1.2mA		–	–	0.4	V
V_{OH_IO}	GPIO output high voltage	When configured as a digital output I_{OH} = -2mA.		2.4	–	V_{CC}	V
V_{OL_IO}	GPIO output low voltage	When configured as a digital output I_{OL} = 2mA		0	–	0.4	V
R_{IN}	Differential input resistance			85	100	115	Ω
R_{OUT}	Output Resistance			42	52	62	Ω
V_{CMSELF}	Self-biased common mode input voltage			–	V_{CC} - 1.3	–	V
V_{INCM}	Common-mode input compliance voltage	Data inputs		V_{CC} - 1.5	–	V_{CC} -$V_{IN(Diff)}$/4	V
$V_{IN(Diff)}$	Differential input voltage	Peak to Peak, Equalizer off		80	–	1000	mV
		For SFP+ applications. (Refer to the Signal compliance mask in Figure 1-1) Equalizer on					
		X1: SFP+ Eye Mask compliance				0.14	UI
		X2: SFP+ Eye Mask compliance				0.35	UI
		Y1: SFP+ Eye Mask compliance		75			mV
		Y2: SFP+ Eye Mask compliance				400	mV

NOTES:

1. Excludes bias and modulation currents delivered to the laser. I_{CC} maximum is for I_{BIAS} = 150mA and I_{MOD} = 2.2V_{PP}
2. The M02172 is designed to support either common anode and common cathode lasers. Once deployed, it is not intended to be switched between laser types.
3. Guaranteed by design and characterization.

Figure 1-1. Differential Input signal Compliance mask at the input of SFP+ module



1.4 AC Characteristics

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C, V_{MOD} = $1V_{pp}$, I_{BIAS} = 40mA, unless otherwise noted.All values measured with the input equalizer on and using 6 inches (15 cm) of FR4 (4000-6/8) non-back drilled stripline trace length.

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Units
V_{MOD}	Modulation voltage adjust range	V_{max}= V_{mod} + V_{offset} < $2.2V_{PP}$ OUTP > 0.8V to keep sufficient head room		0.5	–	2.2	V_{PP}
V_{OFFSET}	Output offset adjust range	Output terminated into 50Ω		0	–	1	V
V_{MOD_RATIO}	Ratio of modulation voltage to MOD_{MON} current	= (V_{MOD})/I_{MODMON}		–	1.6	–	V/mA
PWA	Pulse width adjustment range	50% crossing point at DAC mid range		20	–	80	%
t_R	Modulation output rise / fall times	20% to 80% into 50Ω load. Measured using alternating 1-0 pattern at 2.5Gbps	1, 2	–	28	37	ps
t_F			1, 3	–	40	75	ps
OS	Overshoot of modulation output	Into 50Ω load		–	5	–	%

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Units
RJ	Random jitter	Measured by 7.5GHz Bessel filter at output		–	0.4		ps_{RMS}
DJ	Modulation output deterministic jitter	Peak-to-peak into 50Ω load using 2^{15}-1 PRBS at 10.3Gbps	2		8	15	ps

NOTES:

1. With RS1=1, For Tx Signaling rates > 4.25Gb/s
2. With RS1=0, For Tx Signaling rates ≤ 4.25Gb/s
3. Includes Duty Cycle Distortion

1.5 Soft Control Timing Management

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted using internal micro controller.

Table 1-5. I/O Timing for Soft Control and Status Functions

Symbol	Parameter	Conditions	Notes	Typ	Max	Units
t_off	TX_DIS assert time	Time from TX_DIS bit set until optical output falls below 10% of nominal	1	–	100	ms
t_on	TX_DIS deassert time	Time from TX_DIS bit cleared until optical output rises above 90% of nominal	1	–	100	ms
t_init	Time to initialize, including reset of TX_Fault	Time from power on or negation of TX_FAULT using TX_DISABLE until transmitter output is stable			300	ms
t_fault	TX_Fault assert time	Time from fault to TX_FAULT bit set			100	ms
t_loss_on	RX_LOS assert time	Time from LOS state to RX_LOS bit set			100	ms
t_loss_off	LOS deassert time	Time from non-LOS state to RX_LOS bit cleared			100	ms
t_serial	Serial bus hardware ready	Time from power on until host can read from the serial bus			300	ms

NOTE:

1. Measured from falling clock edge after stop bit of write transaction

1.6 Monitors ADC Specifications

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted.

Table 1-6. A/D Electrical Specifications

Input	Type	Range			Accuracy			Notes
		Minimum	Maximum	Units	Minimum	Maximum	Units	
Tx Power Monitor	(Internal) Current Sinking	10	1400	µA	-10	+10	%	1,2,3
Bias Current Monitor	(Internal) Current Sinking	10	1400	µA	-10	+10	%	1,2,3
Modulation Current Monitor	(Internal) Current Sinking	10	1400	µA	-10	+10	%	1,2,3
Rx Power Monitor	(External) Current Sinking	3	1400	µA	-10	+10	%	1,2,3,4
	Voltage mode	0	2.3	V	-15	+15	mV	2,8,9
Power Supply Monitor	(Internal) Voltage	2.85	3.6	V	-25	+25	mV	2,6
Internal Temperature Monitor	(Internal) Temperature	-40	+105	°C	-3	+3	°C	2,7
AUX1, AUX2	Current Sinking	10	1400	µA	-10	+10	%	1,2,3,4
	Current Sourcing	10	1400	µA	-10	+10	%	1,2,4,5
	Voltage	0	2.3	V	-15	+15	mV	2,8,9
Update Rate	All ADCs	1		kHz	–	–	–	–

NOTES:

1. For definition of sourcing and sinking see Figure 1-2.
2. Module calibration required for valid units.
3. Code 000h means 0µA, code FFFh means 1600µA when sinking current. However, the result is only valid in the range specified.
4. Minimum value of monitored current is achieved with internal digital filter (default setting).
5. Code 000h means 0µA, code FFFh means 1500µA when sourcing current. However, the result is only valid in the range specified
6. Code 000h means 0V, code FFFh means 6.55V. However, the supply monitoring value is only valid in the range specified.
7. ADC output will be offset binary. Code 000h means the lowest temperature the ADC can measure, while FFFh means the highest temperature the ADC can measure.
8. Input impedance of ADC is larger than 100kΩ.
9. Code 000h means 0V, code FFFh means 2.3V. However, the result is only valid in the range specified.

1.7 DAC Specifications

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C.

1.7.1 Bias and Modulation Current DAC Specifications

Table 1-7. Laser Driver Bias and Modulation Current D/A

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	12	–	bits

1.7.2 Internal 6 bit DAC (PWA and Offset) Specifications

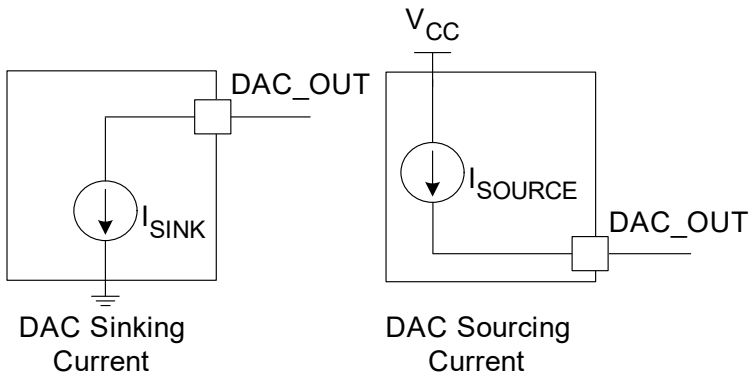
Table 1-8. Internal 6 bit DAC (1)

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	6	–	bits
Full scale output (current sinking)	1.01	–	1.13	mA
Linearity				
DNL	-1	–	+1	LSB
INL	-1	–	+1	LSB
Offset	-5	–	+5	µA
Settling time	–	10	–	µs
Compliance (voltage for sinking current)	1.1	–	2.6	V

NOTE:

1. The pulse width adjust DAC is mapped to GPIO(2) and the Offset DAC is mapped to GPIO(4).

Figure 1-2. DAC Output Definitions



1.7.3 General Purpose 6 bit DAC Specifications

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C.

Table 1-9. General Purpose 6 bit DAC (1)

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	6	–	bits
Full scale output current (current sourcing or sinking)	1.01	1.07	1.13	mA
Linearity				
DNL	-1	–	+1	LSB
INL	-1	–	+1	LSB
Offset				
Current source	–	–	+5	µA
Current sink	-5	-	+5	µA
Settling time	–	10	–	µs
Voltage Compliance				
Current source	0	–	1.1	V
Current sink	1.1	-	2.6	V

NOTE:

1. The General purpose 6 bit DAC is mapped to GPIO(1).

1.7.4 General Purpose 10 bit DAC Specifications

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C.

Table 1-10. General Purpose10 bit DAC (1) ***(1 of 2)***

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	10	–	bits
Voltage Mode Operation (2)				
Full scale output voltage	1.37	1.45	+1.53	V
Linearity				
DNL	-1	–	+1	LSB
INL	-4	–	+4	LSB
Offset	–	–	+1.5	mV
Settling time	–	10	–	µs
Output Resistance	0.8	1	1.2	KΩ
Current Mode Operation (2, 3)				
Full scale output current (current sourcing)	1.40	1.48	+1.56	mA

Table 1-10. General Purpose10 bit DAC (1) (2 of 2)

Parameter	Minimum	Typical	Maximum	Units
Linearity				
DNL	-1	–	+1	LSB
INL	-4	–	+4	LSB
Offset	–	–	+1.5	µA
Settling time	–	10	–	µs
Compliance (voltage for sourcing current)	0	–	1.1	V

NOTE:

1. The General Purpose 10 bit DAC is mapped to GPIO(0).
2. Output may either be a current or a voltage. User selectable.
3. In current mode, DAC output can only source current. See Figure 1-2.

1.8 Inrush Current Specification

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C.

Table 1-11. XFP/SFP+ POR Characteristics

Parameter		Minimum	Typical	Maximum	Units
I_{CC} Peak Inrush ($I_{CC-peak}$)		–	–	50	%
I_{CC} Ramp rate (dI_{CC}/dt) (2)	SFP+			50	mA/µs
	XFP			100	mA/µs

NOTE:

1. Excludes external capacitors. Modules which present a small capacitive load to the host during hotplug are exempt from the inrush current requirements since they limit the total in rush charge.

1.9 Host two-wire Timing Specifications

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C.

The default I2C address is 00h. (MODDEF(1)/SCL and MODDEF(2)/SDA) (Standard Mode or Fast Mode two-wire serial) and NVRAM Controller Timing Specifications (NVRAM1 (SDA) AND NVRAM2 (SCL)) (Fast Mode two-wire serial).

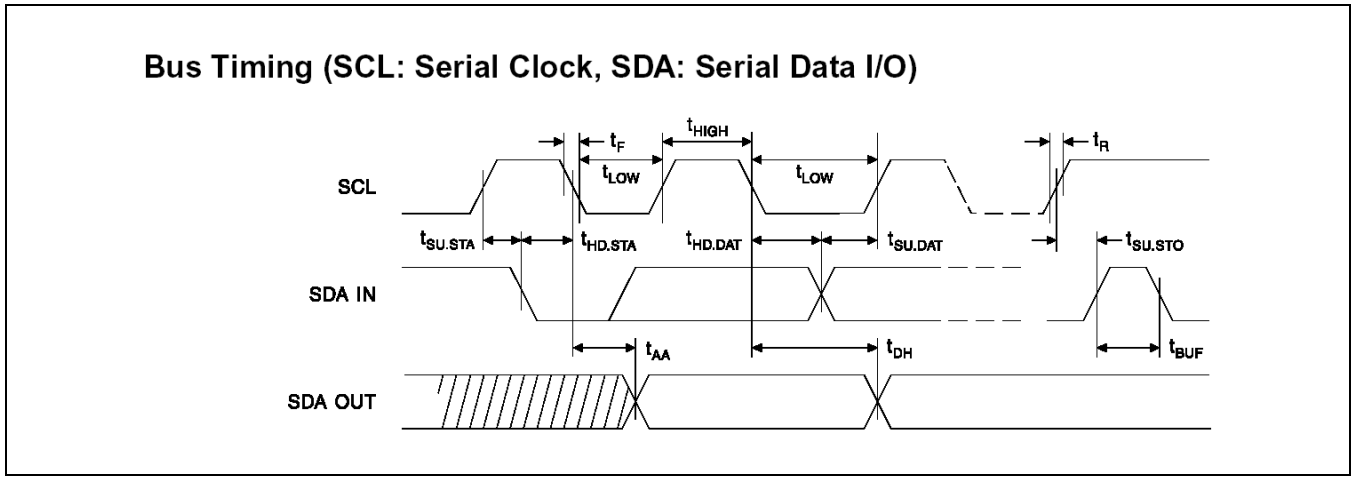
Table 1-12. Host and NVRAM Controller Timing Specifications (see Figure 1-3)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Default I2C address (7 bit) is 00h						
f_{SCL_HOST}	Clock Frequency, SCL (1)		–	–	400	KHz
f_{SCL_NVRAM}	Clock Frequency, SCL		530	–	900	KHz
t_{LOW}	Clock Pulse Width Low		1.3	–	–	µs
t_{HIGH}	Clock Pulse Width High		1.0	–	–	µs
t_{AA}	Clock Low to Data Out Valid		0.05	–	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start		1.3	–	–	µs
t_{HDSTA}	Start Hold Time		0.6	–	–	µs
t_{SUSTA}	Start Set-up Time		0.6	–	–	µs
t_{HDDAT}	Data In Hold Time		3	–	–	ns
t_{SUDAT}	Data In Set-up Time		100	–	–	ns
t_{SUSTO}	Stop Set-up Time		0.6	–	–	µs
t_{f_HOST}	Host Output fall time (2)	20-80%. Capacitive load for each bus line = 10 to 400pF; $R_{PULL-UP}$ = 4.7kΩ to 10kΩ	–	–	100	ns
$R_{PULL-UP\_EE}$	Outputs (NVRAM1 and NVRAM2) internal pull-up resistor value (3)		–	8	–	KΩ
t_{f_NVRAM}	NVRAM Controller Output fall time (3)	20-80%. No external pull-up resistor; 13pf loading	–	–	50	ns
t_{r_NVRAM}	NVRAM Controller Output rise time (3)	20-80%. No external pull-up resistor; 13pf loading	–	–	300	ns
	Time bus must be free before a new transmission start.	Between STOP and START	20			µs
t_{DH}	Data Out Hold Time		50	–	–	ns

NOTES:

1. The host two wire bus is fully compliant with SFP timing requirements to run at 400kHz.
2. For the host interface, the output rise time is determined by user selection of $R_{PULL-UP}$ and the total line capacitance.
3. NVRAM two-wire bus only. Since the M02172 NVRAM1/NVRAM2 is a dedicated two-wire serial bus to the external EEPROM, the M02172 internally includes $R_{PULL-UP}$ to eliminate adding these extra external components.

Figure 1-3. Host and NVRAM Controller Timing Diagrams



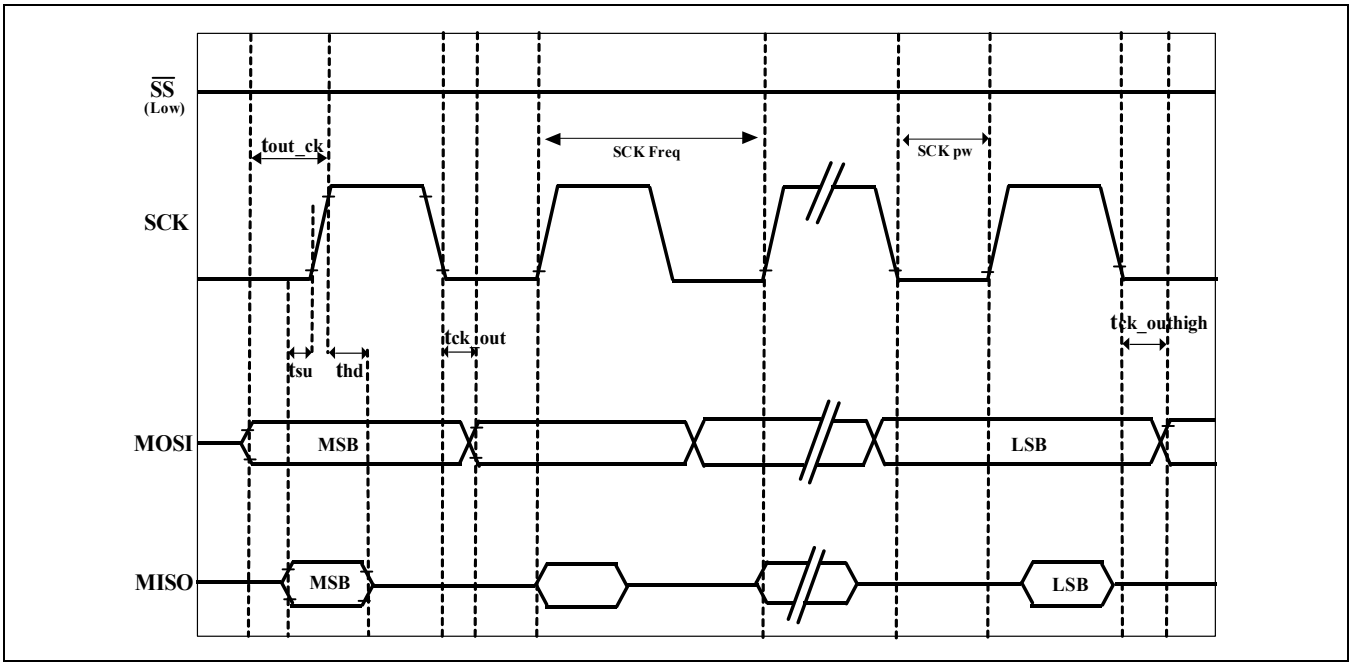
1.10 SPI Electrical Timing Specifications

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C.

Table 1-13. SFP Electrical Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units
	SPI_CK Frequency			10	MHz
	SPI_CK Pulse Width		50% duty cycle		%
	Rise/Fall time		3.6		ns
t_{su}	Setup time		10		ns
t_{hd}	Hold time		10		ns
t_{out_ck}	Out to SPI_CK		0.5 x t_{sck}		ns
t_{ck_out}	SPI_CK to Out		10		ns
$t_{ck\_outhigh}$	SPI_CK to Out high		10		ns

Figure 1-4. SPI Timing Diagram. External controller is Master and M02172 is Slave.



1.11 Control and Status I/O Timing

V_{CC} = 3.05V to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted. Timing values are for hardware pins.

Table 1-14. Timing Requirements of SFP/XFP/SFP+ Control and Status I/O

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_off	TX_DIS assert time	Rising edge of TX_DIS to fall of output signal below 10% of nominal		–	10	µs
t_on	TX_DIS negate time	Falling edge of TX_DIS to rise of output signal above 90% of nominal		–	1	ms
t_init(1)	Time to initialize, including reset of TX_Fault	Time from power on or negation of Tx_Fault using TX_DIS until laser driver output is stable		–	300	ms
t_fault	TX_Fault assert time	From occurrence of fault condition to TX_Fault high		–	100	µs
t_reset	TX_DIS time to start reset	Time TX_DIS must be held high to reset TX_Fault. TX_DIS pulse width required to initialize safety circuitry or reset a latched fault.			10	µs
P-Down/ RST_on	P_Down /RST assert delay	From power down initiation			100	µs
	P_down reset time	Min length of P_down assert to initiate reset	10			µs

NOTE:

1. From power on or hotplug after supply OK or from falling edge of P_Down/Rst

2.0 Pin Definitions

Table 2-1. Pin Descriptions

QFN Pin Number	Name	Function
1	NVRAM1 (SDA)	SDA interface to external EEPROM (internally pulled up to V_{CC} with 8KΩ)
2	NVRAM2 (SCL)	SCL interface to external EEPROM (internally pulled up to V_{CC} with 8KΩ)
3	MODDEF(1) / SPI_O	For 2-wire: MODDEF1 is the serial clock For SPI: SPI_O is slave output
4	MODDEF(2) / SPI_I	For 2-wire: MODDEF2 is the serial data For SPI: SPI_I is slave input
5	V_{CC}	3.3V power supply.Connect to 3.3V
6	Pwdn/Rst	Control input. 60 kΩ internal pull up to V_{CC}. When held high, forces the part into a power down standby mode. The negative edge of Pwdn/Rst signal initiates a complete part (POR) reset. Ground for normal operation
7	DINP	Positive Data Input
8	DINN	Negative Data Input
9	SPI_sel	Control input. When held high indicates SPI is selected (internally pulled down with 60KΩ). When low I2C is selected
10	V_{CC}LD	V_{CC} for the Laser Driver section. Connect to V_{CC}
11	TX_Fault	Safety circuit fault indicator. Open collector output, external resistor pull up to host_V_{CC} required
12	TX_DIS	Control input for Transmit disable. When high or left floating, shuts off both bias and modulation outputs. Set low for normal operation. 7KΩ internal resistor pull-up to V_{CC}
13	GND	Ground. Must be connected to ground for proper device operation
14	IPIN	Monitor photodiode input
15	$IBOUT_{CA}$	Laser bias current output
16	GND0	Ground for modulation output stage. Must be connected to ground for proper device operation
17	Vsense	Can be input or output. For Apogee Imon current sense (Input). For non Apogee, offset control (output)
18	OUTP	Positive modulation output
19	OUTN	Negative modulation output
20	GPIO(4) / Offset DAC	Analog General Purpose I/O. Input or Output or 6 bit DAC (current sinking only)
21	SVCC / $IBOUT_{CC}$	Safety logic controlled V_{CC} to laser anode
22	A/D_{AUX2}	Auxiliary A/D input. Should be left floating when using Vsense or (Apogee mode) feature

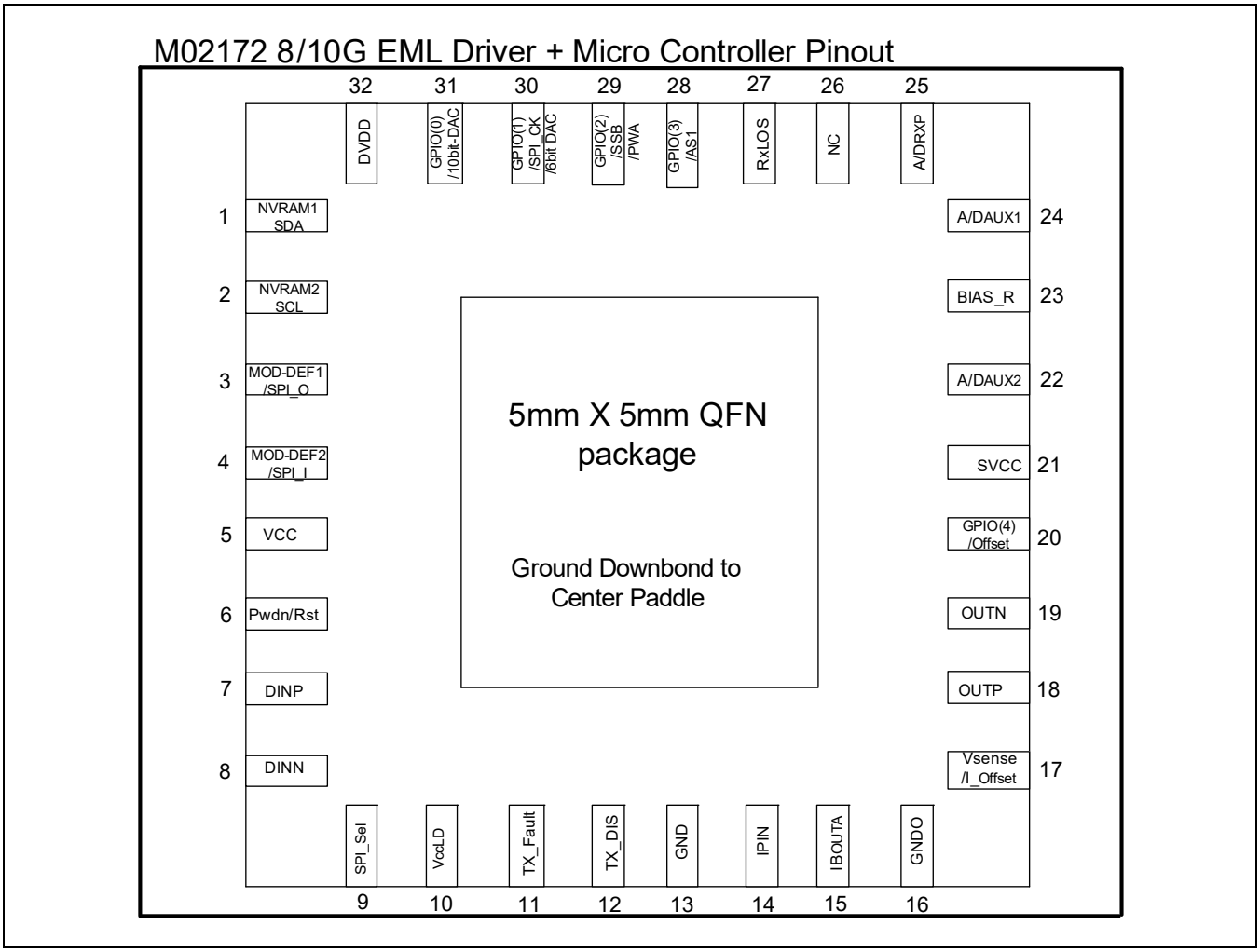
Table 2-1. Pin Descriptions

QFN Pin Number	Name	Function
23	BIAS_R	External resistor for precision bias reference
24	A/D_{AUX1}	Auxiliary A/D input
25	A/D_{RxP}	A/D input for received power monitor
26	NC	Connect to ground for normal operation. (internally pulled down with 60KΩ)
27	RxLOS	Can be selectable Input or Output. If used as input pin, it is Loss of signal from limiting amp (internally pulled down with 60KΩ). If used as output, it is an open collector output. Set Table 3, 0xB6 = 00h for input. Set Table 3, 0xB6 = 40h for output.
28	GPIO(3) / RS1	For SFP+: Can be configured as RS1 rate select (internally pulled down with 60KΩ using an internal switch) For non SFP+: General purpose I/O
29	GPIO(2) / $\overline{SS}$ / PWA	For SPI interface: Slave Select is input to M02172 (should be externally terminated with resistor required for application). Must be low before the data transaction and stay low for the duration of the transaction. For non-SPI: General purpose I/O or 6 bit DAC (current sink only)
30	GPIO(1) / SPI_CK / 6 bit DAC	For SPI interface: SPI_CK is the clock input (10MHz) For non SPI: General purpose I/O or 6 bit DAC (current sourcing or sinking)
31	GPIO(0) / 10 bit DAC	General purpose I/O or 10 bit DAC. Output can be current or voltage. In current mode, DAC output can only source current
32	DVDD	Internally regulated to 1.8V for Digital circuitry. Typically connect a 10nF capacitor to ground
Paddle	GND	Ground. Must be connected to ground for proper device operation

Table 2-2. GPIO PIN Mapping

QFN Pin Number	Pin Name	Integrated Mode SFP Function	External Micro mode SFP Function	External Micro mode XFP Function
20	GPIO(4) / OFFSET DAC	GPIO or DAC	GPIO or DAC	GPIO or DAC
28	GPIO(3) / RS1	RS1 or GPIO	RS1 or GPIO	GPIO
29	GPIO(2) / $\overline{SS}$ / PWA DAC	GPIO or DAC	GPIO or DAC	GPIO or DAC
30	GPIO(1) / SPI_CK / 6 bit DAC	GPIO or DAC	GPIO or SPI or DAC	GPIO or SPI or DAC
31	GPIO(0) / 10 bit DAC	GPIO or DAC	GPIO or DAC	GPIO or DAC

Figure 2-1. Pin Assignments for M02172 Device



3.0 Functional Description

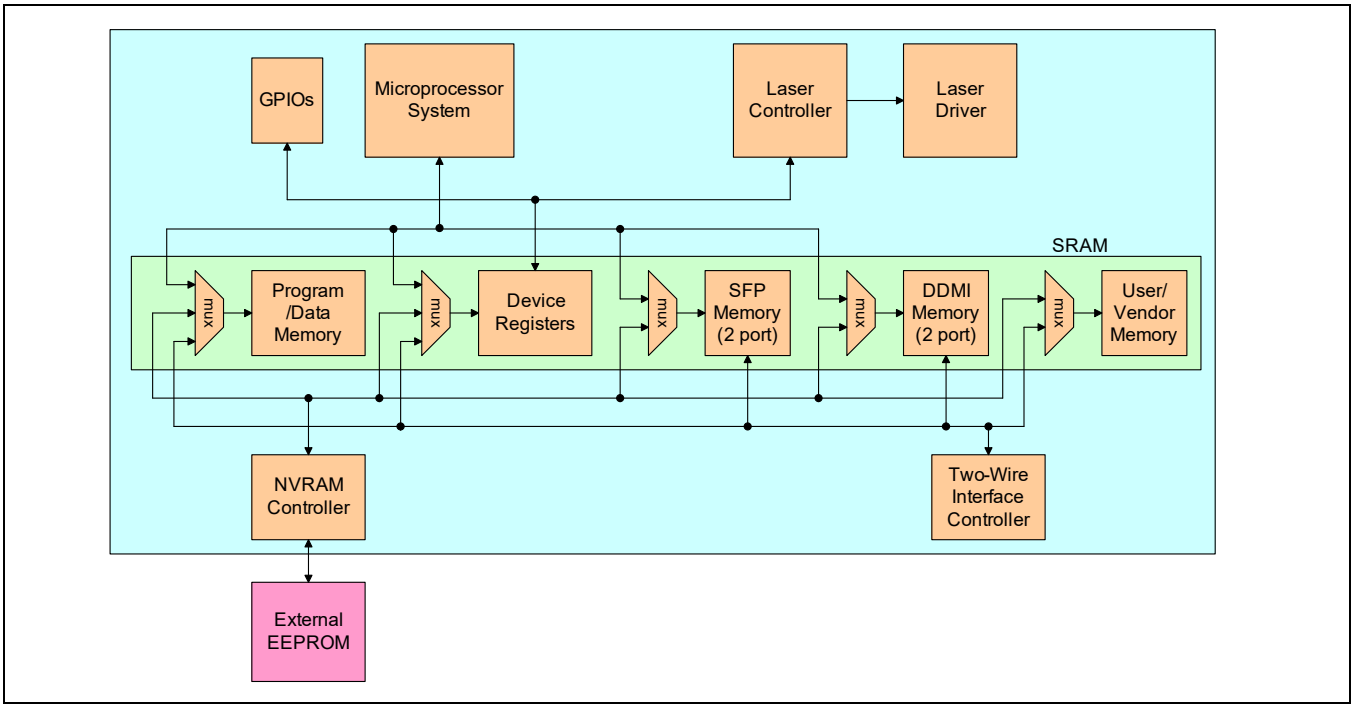
3.1 Overview

The M02172 combines a EML Driver with a SFF-8472 compliant Digital Diagnostic Monitoring Interface for fiber optic transceivers.

The M02172 monitors temperature, voltage, bias and modulation current, transmit and receive power, and other user-defined external parameters. Internal ADCs and comparators allow each parameter to be compared against user-defined threshold levels to provide indication of a fault condition. Integration of the laser driver provides digital control of the laser bias and modulation currents in addition to pulse width control of the modulation current.

Integrated safety circuitry provides latched bias and modulation current shutdown if a fault condition is detected and provides an internal V_{CC} switch.

Figure 3-1. M02172 Architecture



3.2 Features

- Laser Driver with integrated digital diagnostic functions
- 155Mb/s – 11.3Gb/s operation
- Integrated power supply switch for redundant shutdown
- Dual closed-loop OMA control, single-closed-loop and open-loop operation with independently programmable bias and modulation currents
- Compliant with SFF-8431, Rev 3.1 “SFP+” standard for 8.5 and 10.3Gbps
- Compliant with SFF-8472, Rev 10.3: Diagnostic Monitoring Interface for Optical Transceivers
  - Temperature
  - Bias current
  - TX Optical Power
  - RX Optical Power
  - Supply voltage
- Software control of Rate Select, Tx Fault, Tx Disable and Rx LOS
- Alarm/Warning flags are implemented for monitored quantities
- Supports Internal test and calibration
- Automatic power control
- SFP/SFP+ compliant safety circuitry with user selectable bypass
- Pulse width adjustment compensates for asymmetrical laser rise and fall times
- Five user configurable General Purpose I/Os
- Up to four user configurable DAC outputs
- Two available auxiliary 12 bit ADC inputs
- SPI or 2-wire interface, compatible with Serial ID, as defined in the SFP MSA
- Internal A/D – D/A loopback for real time diagnostics
- User and OEM password protection
- Power-on meter (journal timer)
- 12 bit ADC resolution results in exceptional monitor accuracies
- Compact: 32 pin QFN, 5mm x 5mm
- Operating Temp: -40°C to +95°C

3.3 General Description

3.3.1 Overview

The M02172 integrates the digital diagnostic monitoring requirements of SFF-8472 with a highly integrated laser driver intended for applications to 11.3Gbps. The level of integration allows easy set up and calibration of laser power and extinction ratio. The timing requirements of SFF-8472 and the SFP/SFP+ MSA are met when using the

M02172 including soft control timing and status functions of both standards. In addition, integration allows the modulation current monitor to be available digitally and two auxiliary A/Ds are available for customer use in providing features beyond the standards requirements.

The M02172 provides a turn-key solution for SFF-8472 and SFP/SFP+ compliant modules by including firmware that provides the mandatory features of both and enables the manufacturer to easily implement any optional features of their choosing using a simple GUI interface. The M02172 enables automatic module calibration and test that allows for a significant reduction in test cost and complexity.

Many features are user-adjustable, including the APC loop bias control, modulation current including temperature compensation control of the modulation current and laser pulse width adjustment. The M02172 utilizes control of both the bias and modulation currents which allows for management of the optical extinction ratio by compensating for the effects of temperature and aging of the laser.

Safety circuitry is also included to provide a latched shut-down of laser bias and modulation current if a fault condition occurs. An internal V_{CC} switch provides redundant shutdown when operating the device. Safety logic behavior is user configurable.

3.3.2 DDMI Features

This section provides detail on how the Digital Diagnostic Monitoring Interface specified in SFF-8472 is supported in the M02172. The DDMI data is stored in an external EEPROM and accessed through the two-wire serial interface. EEPROM memory is also required to store SFP data, microprocessor code and initial device register values. In order to minimize the additional module complexity and expense of multiple external EEPROMs, the M02172 employs internal memory caches to store the SFP and DDMI data on-chip.

There are two serial interfaces. One (pins MODDEF2_SDA and MODDEF1_SCL) provides access by the host to the stored data. The other (pins NVRAM1_SDA and NVRAM2_SCL) is the interface to the single external EEPROM. Upon power-up, when the device comes out of reset, the device register values are downloaded, followed by the SFP and DDMI data and finally, the microprocessor program code is downloaded and the microprocessor enabled. The timing requirements are given in the Product Specifications Section 1.5, “Soft Control Timing Management,” on page 9.

Two time-stamped versions of the DDMI data are stored in the EEPROM (DDMI 0 and DDMI 1, see Figure 4-4) to ensure that at least one valid data set is available in the event that a module failure occurred when the M02172 was in process of writing data from the on-chip cache memory to the external EEPROM. Each data set (DDMI 0 and DDMI 1) has a checksum for the purpose of determining data integrity. The most recent valid data set is copied to the cache. The SFP data and the microprocessor program code each have their own checksum to determine their integrity similar to the DDMI data.

While the module is in an active state, the data in the DDMI cache is updated by the microprocessor at intervals in compliance with the timing requirements of SFF-8472. The host also has access through the serial interface. To comply with the data integrity requirement, the microprocessor first checks to determine if the host is accessing data before updating the memory. In that event, the update is delayed until the activity ceases. Before the update occurs, the microprocessor also disables the acknowledgment signal of the two-wire interface to prevent the host from initiating a memory access while the cache is being updated.

3.3.2.1 Real-Time Diagnostic Monitoring

Each monitor is independently enabled (to conserve power) by programming the corresponding bit of the ADC control register to a 1. See Table 3-1. The M02172 DDMI memory is updated by the internal M02172 controller with

an update interval of
< 100ms (typically 30ms). The internal M02172 controller must supply the appropriate password before it is allowed to update the DDMI information to prevent corruption of the data if the controller arrives at an unstable state.

The “Ack” of the two-wire interface is disabled during DDMI update. To minimize the duration of the interruption of host access, the internal M02172 controller writes the updated information to shadow registers which is then burst-loaded into the DDMI memory. The interruption of host access will be < 1.2μs.

The DDMI information is periodically copied back to the external EEPROM for protection against loss due to events such as power outages. The frequency of backup is once every twelve hours (derived from the journal timer). Backup of serial ID, diagnostic and other on-chip memory can be initiated by the host through the two-wire interface.

Having separate on-chip and external nonvolatile storage of the DDMI data is a distinct advantage of the M02172 because it allows rapid update of the DDMI data available to the host without exhausting the write endurance of the EEPROM in a short time period. The two most recent backups of the DDMI data are maintained in the external EEPROM at all times. This ensures that a valid data set remains if there is a module failure during the backup operation. Each version has a checksum and a time stamp which determines the most current version. If the information must be reloaded to the on-chip memory, the most recent version with a valid checksum is copied from the EEPROM. The backup operation is transparent to the host with no access interruption.

Table 3-1. ADC Power Down Bit

Monitor	Register Bit Location	Register Bit Name
Modulation Current Monitor	Table 3, 0xC4[2]	mod_adc_pd
Bias Current Monitor	Table 3, 0xCA[2]	bias_adc_pd
Supply Monitor	Table 3, 0xCD[2]	supply_adc_pd
RX Power Monitor	Table 3, 0xD3[2]	rx_pwr_adc_pd
TX Power Monitor	Table 3, 0xD8[2]	tx_pwr_adc_pd
Temperature Sensor Monitor	Table 3, 0xE1[2]	temp_mon_pd
AUX_1	Table 3, 0xD0[2]	aux1_adc_pd
Aux_2	Table 3, 0xDE[2]	aux2_adc_pd

3.3.3 Calibration

The M02172 supports both internal and external calibration as defined by SFF-8472. For internal calibration, the calibration is performed by the M02172 internal controller under software control. For external calibration, the controller simply writes the ADC values to the DDMI memory. One of the two calibrations modes must be enabled to achieve the accuracy specifications.

3.3.4 Alarm and Warning Thresholds

The M02172 supports all the alarm and warning indications defined in SFF-8472. Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These values are defined by the module manufacturer during module initialization and/or calibration and allow the module user to determine when a

particular value is outside of “normal” limits as determined by the module manufacturer. For these indications to be active the thresholds defined in Table 3.15 of SFF-8472 Rev 10.3 “Alarm and Warning Thresholds (2-Wire Address A2h)” must be set. The nominal response time from an alarm or warning condition to the update of the corresponding status bit is 100msec.

The M02172 provides very accurate indication of the present conditions of the module. The sampled diagnostic monitoring signals are stored in device registers. The comparison of each to the corresponding stored threshold values is performed under program control of the microprocessor. Using firmware it is possible to compensate the alarm and warning indications for temperature variations.

3.3.5 Optional Status and Control Bits

The M02172 supports all optional status and control bits (byte 110 of 2 Wire address A2h)defined in Table 3.17 of SFF-8472 Rev 10.3.

3.3.6 Data Inputs

The inputs to the internal data buffer are self-biased through resistors to an internal reference voltage V_{TT}. Input signals can be AC coupled to the part by allowing V_{TT} to float, which sets the common mode input voltage to approximately V_{CC} - 1.3V. Both CML and PECL input signals can be AC coupled to the M02172.

3.3.7 Equalization

For SFP+ applications, the input data can be equalized by enabling the equalizer. SFP+ specifies the jitter requirements at the input of the transmitter under various host board transmission line lengths for both microstrip and stripline. Table 3-2 shows common host board configurations with maximum recommended SFP+ host board trace lengths.

Table 3-2. Host board PCB maximum trace lengths

Type	Material	Trace Width (mm)	Loss Tan	Trace Length (mm)
Microstrip	Standard FR4 (4000-6/8)	0.3	0.022	200
	Nelco (4000-13)	0.3	0.016	300
Stripline	Standard FR4 (4000-6/8)	0.125	0.022	150
	Nelco (4000-13)	0.125	0.016	200

3.3.8 Data Polarity / Pulse Width Adjust

After the data passes through the data input buffer, it enters the pulse width adjust buffer. It incorporates a polarity selection as well as a pulse width adjustment control to compensate for laser pulse width distortion. By adjusting the current from the pwa_dac[5:0], pulse width can be adjusted from 20% to 80%. Pulse width control can be disabled by setting the pwa_en bit low, resulting in approximately 50% crossing point at the output and reduces the supply current by 2mA.

3.3.9 Output Buffer

After the data passes through the pulse width adjust buffer, it enters the output buffer. The output buffer reshapes and ground reference the signal in order to drive the output stage with enough speed and correct output levels.

3.3.10 Photodiode polarity

M02172 supports common anode or common cathode photodiode independently from the laser mode.

3.3.11 Rate select function

To comply with the SFP+ rate select requirement, when the device in low rate mode, power is reduced in the signal path and the compensation is switched on at the outputs.

3.3.12 Pwdn/Rst

This is a multifunction input pin for module power down and reset. When held “high”, in order to meet the power dissipation requirements of XFP applications, the laser is forced to low rate mode and the modulation and bias currents are not set by the DAC. They are set by an internal current reference of low value in order to reduce the power dissipation of the module.

3.3.13 Laser Driver Output Stage

The output stage incorporates feedback to maintain performance over the range of laser modulation current. The output stage is nominally configured to drive EML and DML with 50Ω characteristic impedance. The M02172 has internal 50Ω terminations between the outputs OUTP, OUTN and the internal supply. In EML applications, programmable offset adjustment is integrated into the signal output.

The laser driver output stage is separately grounded from the rest of the circuitry (through GNDO) for optimum performance and control of output characteristics.

Two independent high-frequency compensation networks are included to allow additional flexibility with setting the output response characteristics. A binary network and an additional three bits (oc0, oc1, oc2) can be used to tune two separate internal RC networks at the M02172 output providing control of output stage damping in order to optimize the optical eye diagram.

Laser modulation current is controlled by adjusting the MODSET DAC current. The modulation current can be temperature compensated in the digital state machine by changing the MODSET DAC current by a programmed ratio to the temperature ADC reading. Refer to Section 3.3.16, “Modulation Current Control,” on page 30.

When Pwdn/Rst is high, the MODSET DAC is disconnected and the modulation is set below its lowest value.

3.3.14 GPIO Operation

The M02172 has five GPIOs that can individually be configured as a digital input, a digital input with an interrupt, a digital output, or the output of a DAC. When configured as a digital input the device firmware responds to the signal level on the GPIO. The rate of polling of the GPIO configured as a digital input is defined within the firmware which if implemented, would typically result in polling intervals of 20ms. The digital input with an interrupt is used in the same way, but as an interrupt the response time to a signal change is typically 3ms. The interrupt method is

completely configurable as one of the four following formats: low level or high level causes the interrupt, or rising or falling edge causes the interrupt. As a digital output, the level can be fixed during device initialization/calibration or can be varied by the device firmware (i.e. as a rate select output to a limit amp responding to the module rate select input). Finally, each GPIO can be the output of one of the internal DACs. The DAC mapping is shown in the block diagram and similar to a digital output, the level can be fixed during device initialization/calibration or can be varied by the device firmware changing the DAC setting in response to a defined event.

3.3.15 Automatic Power Control

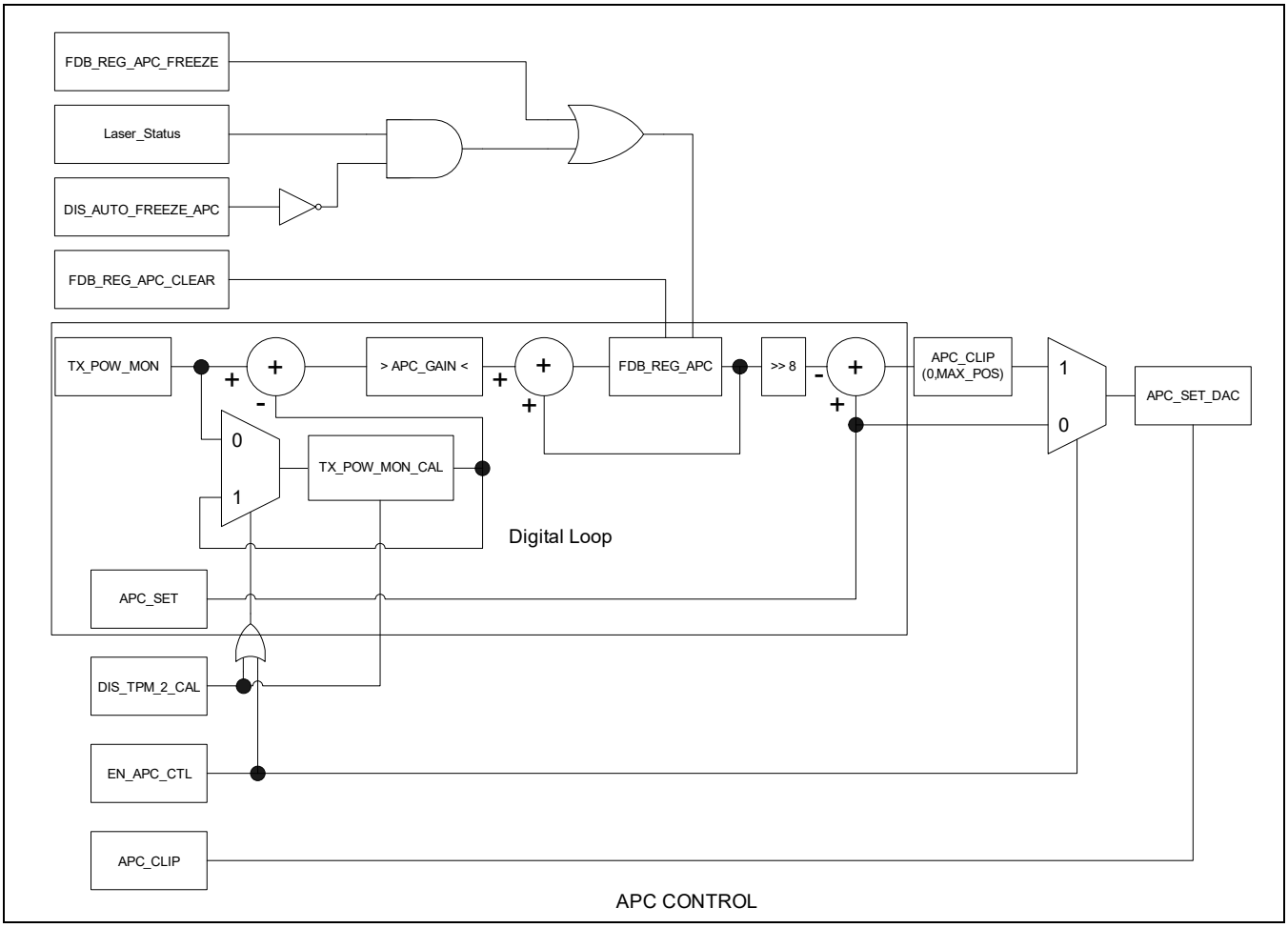
The M02172 incorporates unique and innovative options for controlling the transmitted laser power. Control mechanisms are provided for controlling both the bias current and the modulation current. Each includes multiple techniques which can be independently enabled or disabled. This allows maximum reconfigurability in a wide variety of applications and choice of laser.

3.3.15.1 Bias Current Control

The M02172 allows two methods of controlling the laser bias current: closed loop digital control and open loop control. Each mode is enabled by selections made within the device register settings.

Control of the bias current is illustrated in Figure 3-2. TxPwrMon is an internally mirrored replica of the current flowing into IPIN. The updated TxPwrMon value is written to the tx_pwr_mon registers. All modes start with setting the target output power by writing to the apc_set registers.

Figure 3-2. Bias Current Control



3.3.15.1.1 Closed loop Digital Control

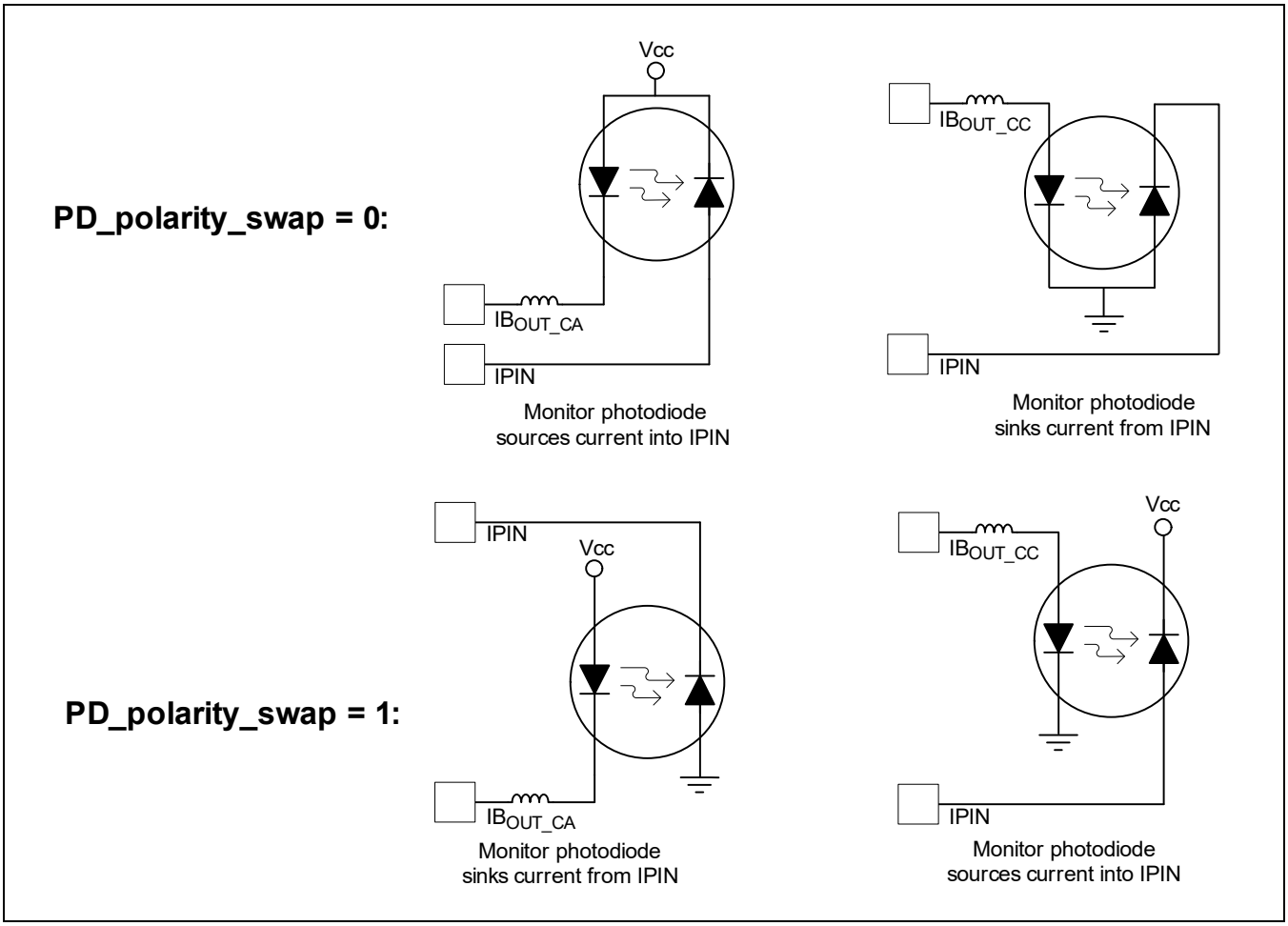
M02172 includes circuitry to automatically maintain laser average output power with use of a monitor photodiode. Figure 3-3 shows various photo diode connection and PD polarity swap configuration examples.

Closed loop digital control is configured by setting apc_cntrl bit high. In closed loop digital control mode the apc_set registers are the uncalibrated reference level for the average optical power. Closed loop digital control varies the bias current (using the apc_set value) to maintain the measured tx_pwr_mon equal to the value stored in the tx_pwr_cal registers during module calibration.

Closed loop digital control is a state machine that utilizes the laser monitor photodiode and requires the desired average value of the output optical power to be stored in the tx_pwr_cal registers. An internal current mirror mirrors the monitor photodiode current at IPIN and is labeled TxPwrMON. The most recent value of TxPwrMon is stored in the TX_POW_MON register. The M02172 utilizes a precision integrator (low pass filter) on TX_POW_MON. The output of the integrator is compared to the desired average value of optical power in the TX_POW_MON_CAL

registers and the resulting 12 bits adjusts the bias current up or down accordingly through the APC_SET_DAC registers.

Figure 3-3. PD polarity swap configuration examples



3.3.15.1.2 Open loop Control

With open loop control there is no feedback from the laser output to the bias control. A value is simply written that corresponds to the desired value of the output bias current. The bias current maintains this output level regardless of laser performance unless a fault condition occurs whereby the safety loop disables the bias current output.

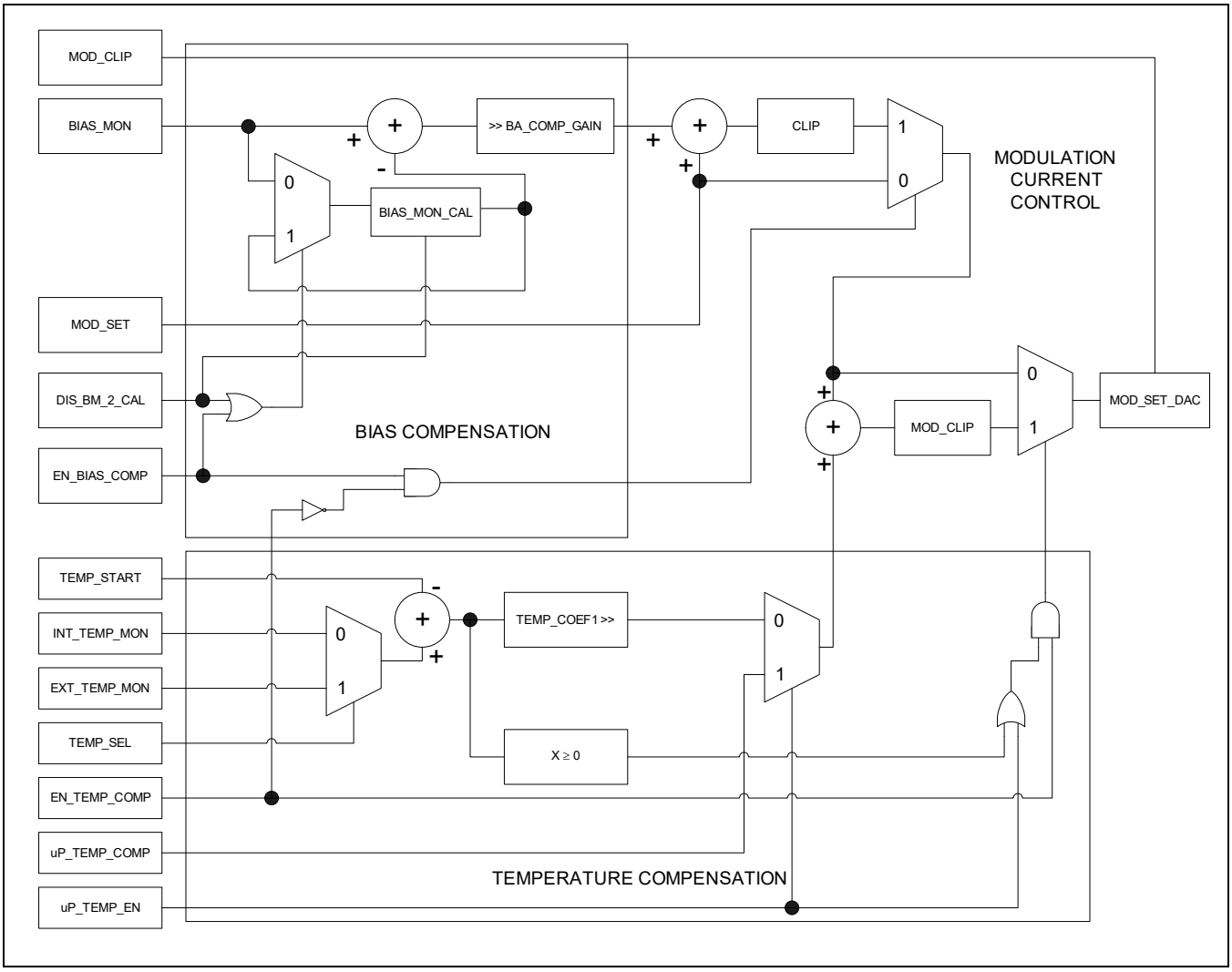
Open loop control of the bias current is achieved by setting apc_cntrl low and writing the desired value to the apc_set register.

Even though the bias current is operating open loop, it is possible to implement temperature compensation under firmware control by using either a look-up table or a polynomial to modify the value with temperature.

3.3.16 Modulation Current Control

Control of the modulation current is open loop with programmable compensation for changes in the bias current and for changes in the temperature. This is illustrated in Figure 3-4.

Figure 3-4. Modulation Current Control



The target modulation current is set by writing to the MOD_SET register.

3.3.16.1 BIAS-Adjusted Compensation of Modulation Current

This form of compensation is configured by setting EN_BIAS_COMP high and EN_TEMP_COMP low. The BIAS_MON ADC is periodically sampled. The new MOD_SET_DAC value is computed based on a ratio set in the BA_COMP_GAIN register.

The register BA_COMP_GAIN is equivalent to “percent bias current slope” factor adjustment on the modulation current. If BIAS_MON (the present bias monitor output) is larger than the BIAS_MON_CAL value (established during module calibration) the modulation current is increased proportionally to their differences (times the programmable constant BA_COMP_GAIN). If the BIAS_MON is smaller than BIAS_MON_CAL then the modulation current is decreased. In this sense, compensation using bias is different from compensation using temperature since BIAS_MON_CAL is a reference current and all modulation current adjustments are made based on any change from this current rather than only by temperature alone.

3.3.16.2 Temperature Compensation of Modulation Current

This form of compensation is configured by setting EN_TEMP_COMP high (default). When enabled, temperature compensation takes precedence over bias-adjusted compensation. The temperature reading can come either from the internal temperature ADC or an external temperature sensor connected to the auxiliary A/D_{AUX2} input, and is selectable by the TEMP_SEL register.

The temperature threshold at which temperature compensation is to start is written into TEMP_START. The first order temperature compensation coefficient TEMP_COEF1 is programmable between -12 to +11. The difference between TEMP_START and the current temperature is multiplied by 2^(TEMP_COEF1). The product is then added to the input MOD_SET and the MOD_SET_DAC value is the result.

The TEMP_START value is in terms of the 12 bit temperature value out of the temperature monitor whether it is based on the internal or an external sensor. The register Temp_Coef1 is the gain applied to the difference between xxx_TEMP_MON (internal or external) and Temp_Start. The result is the modulation current compensation.

Second order temperature compensation is provided by the internal device controller through the register uP_TEMP_COEF by enabling uP_TEMP_EN. If uP_TEMP_EN is high then temperature compensation will come from the firmware through uP_TEMP_COEF. Through the use of firmware compensation, both look-up tables and higher order compensation are possible and can be used to compensate for modulation current versus temperature.

3.3.17 Current Monitors

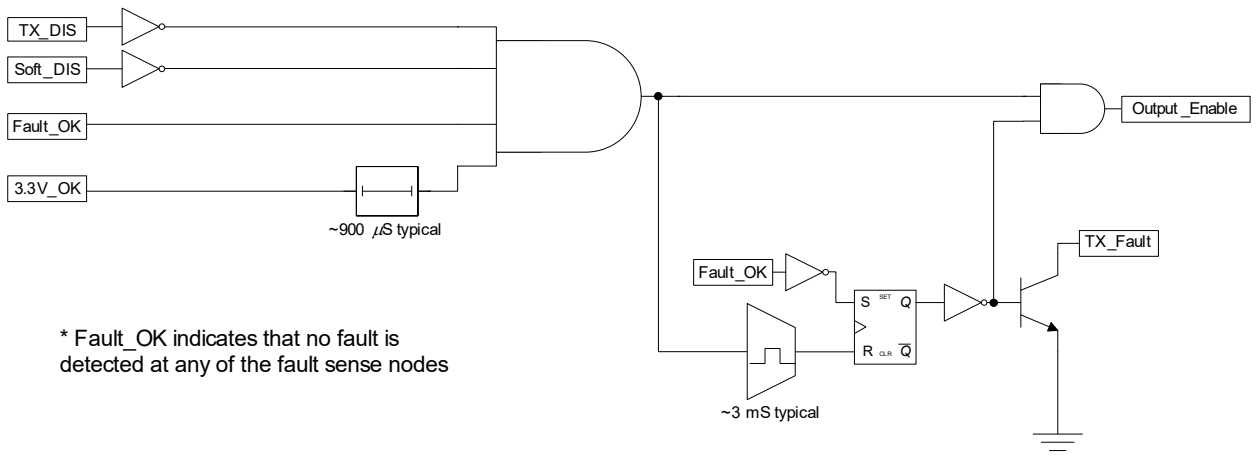
Internal monitors are provided for transmit power ($TxPwr_{MON}$), bias ($BIAS_{MON}$) and modulation current (MOD_{MON}). These are reported through the $TxPwr_{MON}$, $BIAS_{MON}$ and MOD_{MON} A/D registers.

3.3.18 Laser Eye Safety

Using this laser driver in the manner described herein does not ensure that the resulting laser transmitter complies with established standards such as IEC 825. Users must take the necessary precautions to ensure that eye safety and other applicable standards are met. Note that determining and implementing the level of fault tolerance required by the applications that this part is going into is the responsibility of the transmitter designer and manufacturer since the application of this device cannot be controlled by MACOM.

3.3.19 Safety Circuitry

Figure 3-5. M02172 Safety Logic (Safety Circuit Bypass Function not Shown)



For information on bypassing the safety logic, see Section 3.3.19.1, “Safety Circuitry Bypass,” on page 33.

Comparators at V_{CC}LD, $IBOUT_{CA}$, $IBOUT_{CC}$, IPIN and OUTP will assert the TX_Fault output (and will set the appropriate bit in the Diagnostics 2 area of the DDMI memory map Table 4-1) indicating that a fault condition has occurred. This condition is latched and requires SOFT_DIS or TX_DIS to be toggled or device should be power cycled before device reset occurs. SV_{CC} is opened during a fault or disable condition.

By setting either TX_DIS high or SOFT_DIS high, the bias and modulation output currents are disabled. TX_DIS will disable laser bias and modulation current if left floating. TX_DIS must be forced to a low state to enable the outputs.

Safety Circuitry in the M02172 will disable the modulation and bias current and assert the TX_Fault output immediately upon detecting a fault condition. In addition, the supply voltage that sources the laser current (SV_{CC}) will immediately go open circuit and prevent any current from passing through the laser.

Fault conditions checked by the M02172 include shorts to ground or V_{CC} of all pins which can increase the laser power directly or indirectly (i.e. control circuitry).

For an initialization or power-up sequence to be successful, all the fault detection monitors must signal that the device is “healthy”, unless bypassed (see Section 3.3.19.1).

When TX_DIS goes low, pins are checked for shorts to ground or V_{CC} and a TX_Fault condition is latched if there is a fault.

If the state of the pins is OK, a one-shot at the reset pin begins a countdown which will latch a TX_Fault condition if the bias current has not stabilized to an acceptable level during the one-shot time.

The one-shot width is approximately 3 ms.

3.3.19.1 Safety Circuitry Bypass

The M02172 provides the module vendor the ability to change the behavior of the safety logic. As described above, and shown in Figure 3-5, the default operation is that when a fault is detected, the TX_Fault output is asserted and latched and the laser modulation current is disabled.

There are two registers: Laser Driver Control Register 0 and Laser Driver Control Register 1 that allow the module vendor to determine how the M02172 responds to a fault condition. The soft_scb bit of LD Control Register 0 allows the safety circuitry bypass to be enabled.

When safety circuitry bypass is enabled, a fault condition no longer immediately disables the laser modulation current but will assert the TX_Fault output (and set the appropriate bit in the Diagnostics 2 area of the DDMI memory map Table 4-2) indicating that a fault condition has occurred. This condition is latched and can be cleared by toggling either SOFT_DIS or TX_DIS or power cycling the device. However, the result is that laser modulation is interrupted. An alternative method to reset the TX_Fault latch is available when bypass is enabled, the reset_fail bit of LD Control Register 1 will reset the TX_Fault latch and not interrupt the laser output.

Additionally, there is the provision to disable the latching of the TX_Fault output completely. This is accomplished using Latch_override bit in LD Control Register 1. When enabled, it disables the latching of the TX_Fault output meaning that the TX_Fault output will only remain asserted as long as a fault condition persists. If the fault condition is transient, the TX_Fault output will de-assert when the transient condition causing the fault passes.

3.3.19.2 Fault Conditions

This section describes the M02172 operating modes during fault conditions. Over voltage, under voltage, pins shorted to V_{CC} and pins shorted to ground are included in the fault Table 3-3.

Table 3-3. Circuit Response to Single-Point Fault Conditions

Pin Number	Pin Name	Circuit Response to Over-voltage Condition or Short to Vcc	Circuit Response to Under-Voltage Condition or Short to Ground
1-4	NVRAM1, NVRAM2, MOD-DEF(1) MOD-DEF(2)	Does not affect laser power.	Does not affect laser power.
5	V_{CC}	Outputs are disabled if V_{CC} exceeds the supply detection (high level) threshold.	Outputs are disabled if V_{CC} voltage is below the supply detection (low level) threshold.
6	Pwdn/Rst	Module stays in power down mode	Does not affect laser power.
7, 8	D_{IN}+, D_{IN}-	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.(1, 2)	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.(1, 2)
9	SPI_sel	Does not affect laser power.	Does not affect laser power.
10	VccLD	Laser bias current will be shut off, then a fault state occurs.(1)	A fault state occurs.(1)
11	TX_FAULT	Does not affect laser power.	Does not affect laser power.
12	TX_DIS	Bias and modulation outputs are disabled and SVcc is opened.	Does not affect laser power (normal condition for circuit operation).

Table 3-3. Circuit Response to Single-Point Fault Conditions

Pin Number	Pin Name	Circuit Response to Over-voltage Condition or Short to Vcc	Circuit Response to Under-Voltage Condition or Short to Ground
13	GND	A fault state occurs.(1)	Normal operation.
14	I_{PIN}	A fault state occurs. (1, 3)	A fault state occurs. (1, 3)
15	$IBOUT_{CA}$	No safety circuitry on this output	No safety circuitry on this output
16	GNDO	A fault state occurs.(1)	Normal operation.
17	Vsense	Does not affect device operation.(4)	Does not affect device operation.(4)
18	OUTP	Does not affect laser power during common cathode operation. During common anode operation, laser modulation is prevented; the APC loop will increase bias current to compensate for the drop in laser power. If the set output power can not be obtained, a fault state occurs.(1,2)	A fault state occurs.(1)
19	OUTN	Does not affect laser power during common anode operation; does not affect laser power during common cathode operation since output is AC coupled.	Does not affect laser power during common anode operation; does not affect laser power during common cathode operation since output is AC coupled.
20	GPIO(4)	Does not affect laser power.	Does not affect laser power.
21	$SV_{CC}/IBOUT_{CC}$	Does not affect laser power if output is configured for common anode. If output is configured for common cathode operation, a fault state occurs.(1)	In either common anode or common cathode configuration, the laser is turned off and a fault state occurs.(1)
22	A/D_{AUX2}	Does not affect laser power.	Does not affect laser power.
23	BIAS_R	Turns off internal reference current for laser driver bias and modulation; no laser output.	A fault state occurs.(1)
24	A/D_{AUX1}	Does not affect laser power.	Does not affect laser power.
25	A/D_{RxP}	Does not affect laser power.	Does not affect laser power.
26	TEST	Laser Driver is Disabled	Does not affect laser power.
27-31	RxLOS, GPIO(0-3)	Does not affect laser power.	Does not affect laser power.
32	DV_{DD}	A fault state occurs. (1)	Disables laser driver.

NOTES:

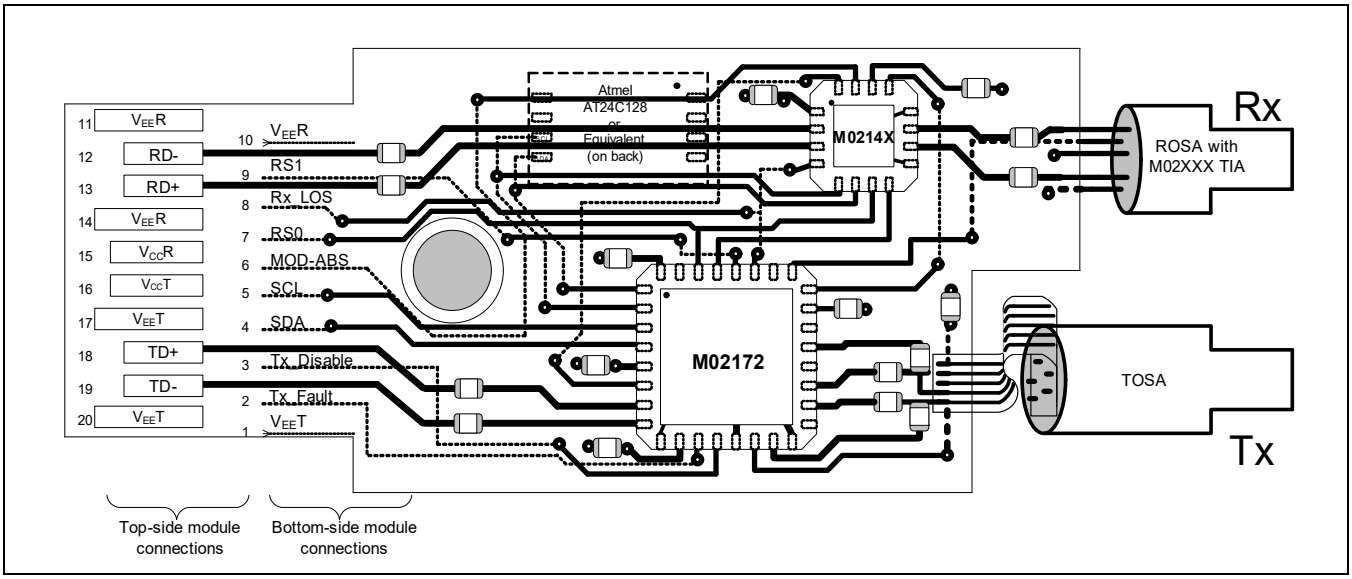
1. Unless the safety circuitry is bypassed, a Fault state will assert the TX_Fault output, disable bias and modulation outputs and open the switch at SV_{CC}.
2. Does not affect laser power when the modulation output is AC coupled to the laser.
3. Does not affect laser power in open loop mode.
4. While the device operation is not affected by voltage applied at pin 17, any external circuitry connected to this pin must also be considered.

4.0 Applications Information

4.1 Applications

- 300 Pin, X2, XFP and SFP/SFP+ Optical Transceivers
- SONET/SDH Transceivers
- 1/10 Gigabit Ethernet Modules
- 1G/2G/4/8/10G Fibre Channel Modules

Figure 4-1. M02172 Placement in SFP+ Module



4.2 Configuring the M02172 for Typical Applications

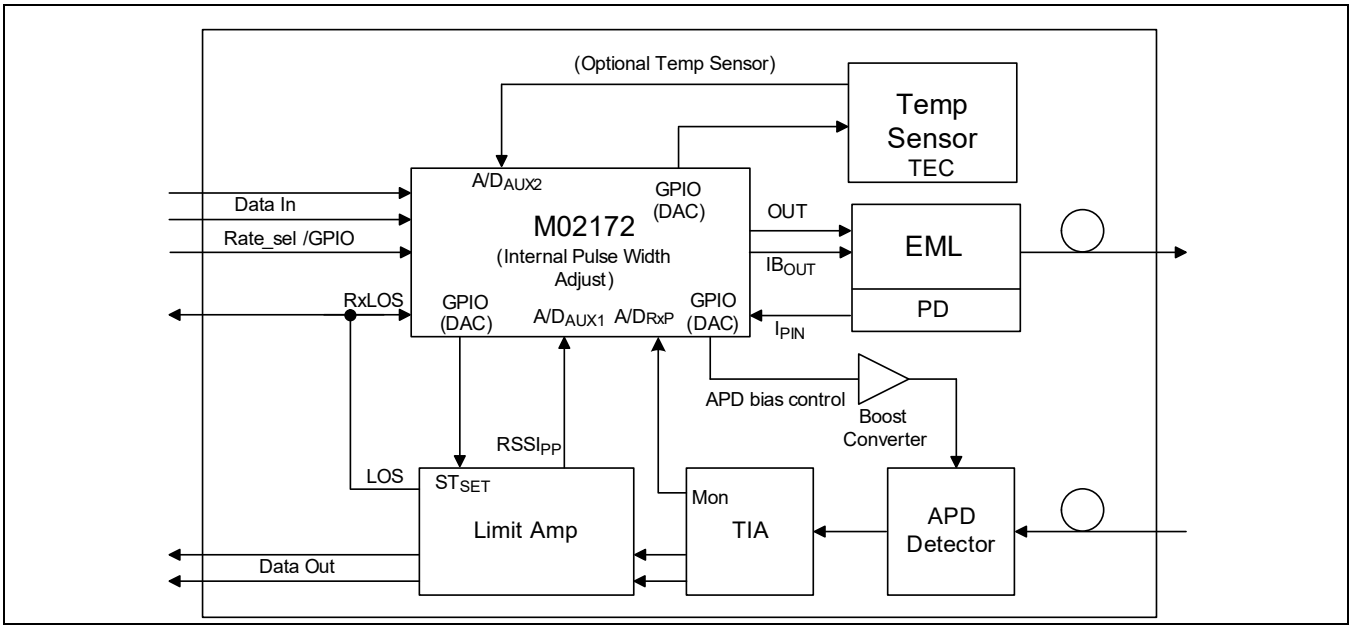
Because of its versatile architecture, the M02172 is easily adapted for a variety of applications. Several typical combinations are presented here, but there is much flexibility for module vendors to create their own variations.

The pulse width adjustment (PWA) DAC, as well as a 10-bit auxiliary DAC and the two 6-bit auxiliary DACs are each connected to one of the four GPIOs to enable their use for external purposes. The received average power (RxP) ADC and the two auxiliary ADCs are external inputs.

4.2.1 Application: M02172 with Externally Modulated Laser

The primary applications for this configuration are OC-192 SONET, 10GFC Fibre Channel, and 10Gigabit Ethernet long-reach (> 80km) transceivers in either 300Pin, X2, XFP and SFP+ form factors. Figure 4-2.

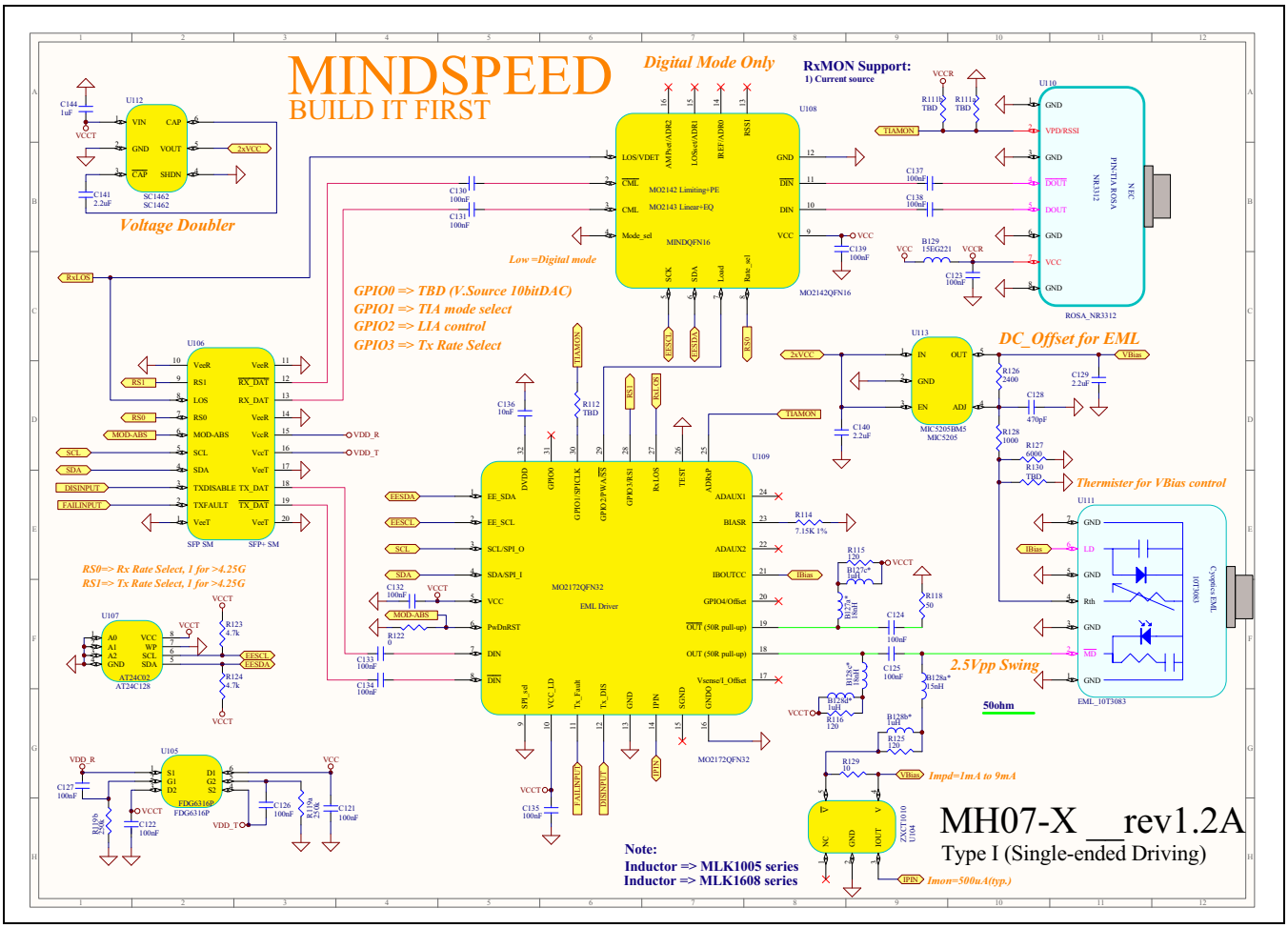
Figure 4-2. M02172 with EML Laser



4.2.2 M02172 SFP+ Reference Design

Below is the schematic for the actual SFP+ implemented reference design on an SFP+ form factor.

Figure 4-3. M02172 SFP+ Reference Design



4.3 Device Monitors Calibration

This section describes how the device, using MACOM supplied firmware, supports the device monitors calibration requirements of SFF-8472. The standard uses the term calibration to refer to the conversion of the raw monitor ADC values to actual temperature, voltage, power, etc. values. This should not be confused with the module calibration (and configuration) features.

4.3.1 Internal and External Calibration of Monitored Parameters

As specified in SFF8472, the monitored parameters can be calibrated either externally or internally. With internal calibration the measurements are calibrated over the operating temperature and voltage and are interpreted in real world units versus raw A/D values. External calibration stores raw A/D values which must be converted to real world units by the host using calibration constants given in Table 3-16 of SFF-8472, Rev 10.3.

4.3.2 Additional or Reserved Monitors

The M02172 includes two auxiliary ADCs for monitoring purposes in addition to the modulation current monitor. Provisions exist in SFF-8472 for two more internally calibrated monitor values with associated alarm and warning levels. However, note that an insufficient number of bytes have been reserved by SFF-8472 to support external calibration for these additional monitored values. Therefore the additional Aux_ADC monitors and/or the modulation current monitor can only be mapped to the reserved locations for internally calibrated monitors and warning levels. If these monitors are not mapped to the reserved locations, the values and alarm/warning levels are still stored in PDRAM.

4.3.3 Real Time Module Diagnostic Miscellaneous Status Bits

The device firmware also monitors the status of the module and updates the miscellaneous status bits stored in (A2h, 110d). The status bits include:

- Tx Disable
- Soft Tx Disable
- Rx Rate Select
- Soft Rx Select
- Tx Fault
- Rx LOS
- Data_Ready_Bar

4.4 Two-wire Host Memory Access Model

All on-chip memories can be accessed via the host two-wire interface using serial device addresses A0h and A2h. The on-chip memory is partitioned into 128 byte tables accessed using 8-bit addresses and a programmable table select byte where the memory partition is configurable to comply with the SFP/SFP+/DDMI standards. The table select byte defaults upon power up to 00h. The table select byte is used as the MSB address bits and if the host attempts to write an invalid table select byte, nothing will be written and if an attempt is made to read using an

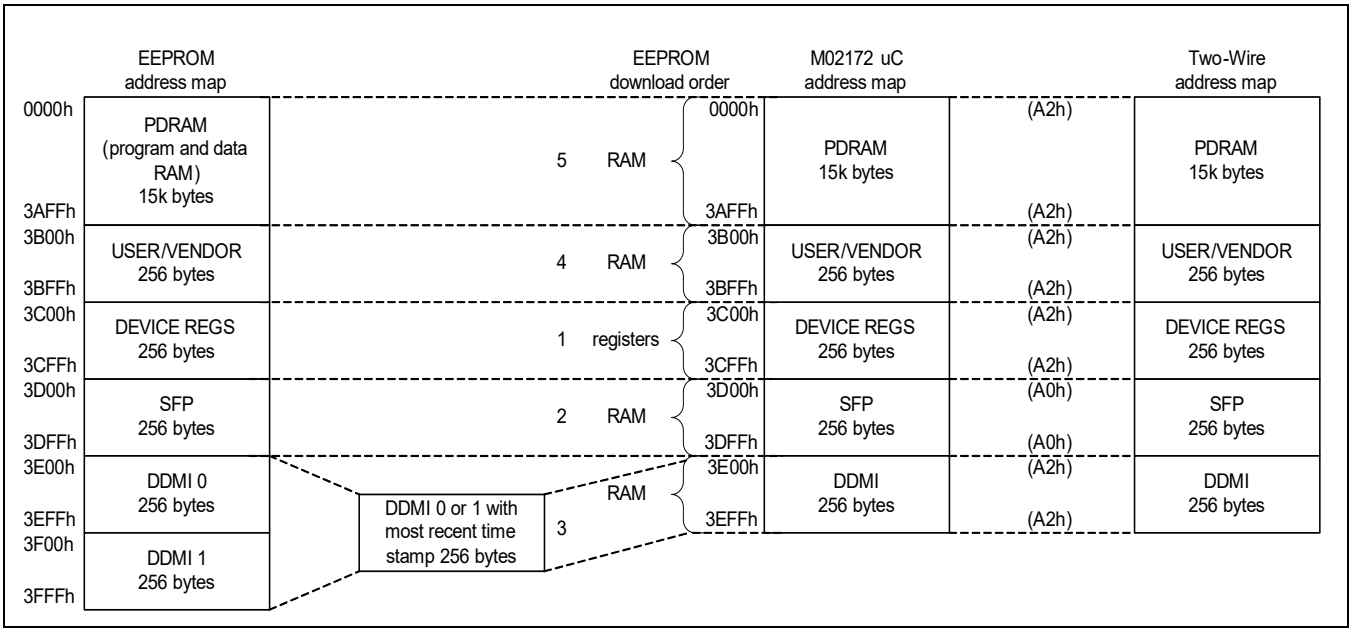
invalid table select byte, the return value will be zero. The host interface memory map is defined in Table 4-1.

Note that the information at both two-wire addresses (A0h and A2h) may be accessed by using the appropriate address without the need for a special address change sequence. This means that accessing information at either address can be accomplished by the host at any time.

Figure 4-4 describes the device memory map to the EEPROM, internal device controller and the host two-wire serial interface.

Section 4.4.3, “Host Two-wire Serial Interface Block (see Table 1-12 and Table 1-14 for specifications),” on page 40 describes the DDMI and SFP/SFP+ memory maps in more detail.

Figure 4-4. Memory Mapping Table



4.4.1 NVRAM Controller Initial Data Download (see Table 1-12 and Table 1-14 for specifications)

The NVRAM Controller block is used to download all the 16 k external RAM from the NVRAM to the internal device registers and memories after power on reset.

During NVRAM download, the M02172 internal uC8051 is disabled while the NVRAM Controller is the master driving the 2-wire EEPROM (NVRAM1 and NVRAM2) bus. The NVRAM Controller first downloads the 256 byte device register data along with the SFP, DDMI and the program and data RAM (PDRAM) checksums (see the “EEPROM download order” column in Figure 4-4). The NVRAM Controller then downloads the 256 byte SFP data image. The SFP checksum is recomputed and compared with the downloaded checksum. (The checksum is defined as the modulo 256 sum of the SFP data.) If the two checksums are not equal, the SFP Checksum Error register bit is set. The M02172 SFP checksum data is held in the Device Registers section of its registers.

The download of the DDMI data is slightly different. The controller reads both data images DDMI 0 and DDMI 1. Each checksum is recomputed and compared with the downloaded checksum from the Device Register section.

The controller also polls the DDMI status register STAT_DDMI to determine which DDMI is the most recent write back to the EEPROM. The DDMI data image containing the most recent data (based on STAT_DDMI) with a valid checksum is loaded into the DDMI memory. If neither checksum is correct the DDMI 0 and DDMI 1 Checksum Error register bit is set and the 256 bytes of data are still loaded into the internal DDMI memory based on the timestamp status bit.

Finally, the NVRAM Controller downloads the program and data image to the internal device RAM. If the checksum comparison fails, the download will be attempted two more times. If all three attempts fail, the download will remain in the internal RAM, the PDRAM Checksum Error register bit is set and the device will be put into host mode in which the device uC8051 is disabled and the only way to control the device is through the host two-wire serial interface. The download can also be initiated by a signal from uC watchdog timers and from the NVRAM Controller control register (02, 80h).

4.4.2 Uploading the Device Registers and Internal Memories (SFP, DDMI, 15 kbyte PDRAM) to the External EEPROM

The NVRAM Controller is allowed to write back device registers and internal memories to the external EEPROM. It can be initiated by either the device uC8051 or through the host two-wire serial interface. This is accomplished by writing to the NVRAM Controller control register.

The uC8051 and the host can be enabled to initiate a W/R backup of the SFP data, the DDMI data, and the device registers. Only the host is allowed to initiate a backup of the 15k PDRAM, user memory and vendor memory.

During the backup of the SFP data, the DDMI data, and the device registers, the finite state machine controller will send an interrupt to the uC8051 forcing the microcontroller into a wait state. To accomplish this, the uC memory bus has to communicate with the 15k PDRAM memory program code. During this time, the uC and the host are able to read the device register section. At the end of the backup, the interrupt is released, bringing the uC out of the wait state. During the write back operation, new checksums of the SFP data, the DDMI data and the 15k PDRAM have to be computed either by the device firmware or by the host controller.

A special case exists for updating the DDMI memory with calibration information. When either the device uC or host sends a command to write back the DDMI data, the NVRAM Controller toggles the STAT_DDMI status bit and writes the DDMI data into the corresponding image in the external EEPROM. The timestamp and checksum are also written to the appropriate locations in the EEPROM. During the backup time to the EEPROM, the host will have read only access (with the appropriate password) of the DDMI and SFP dual-port memories. At the end of the backup mode, the interrupt is released, bringing the uC out of the wait state and the clear on read status bit eeprom_access_done will be asserted when the EEPROM access is complete.

Whenever the host or device initiates a write back of the DDMI memory data to the external EEPROM, a dummy read should follow the write operation to force the device to increment the DDMI memory location in the EEPROM (DDMI 0 or 1) that it will next write back to. (The MACOM supplied firmware performs this function whenever it writes to the EEPROM DDMI memory).

4.4.3 Host Two-wire Serial Interface Block (see Table 1-12 and Table 1-14 for specifications)

- Slave operation only
- Supports 7-bit addressing on the two-wire serial bus
- Supports Standard and Fast Mode transfer rates

- During write back to the 15k program and data RAM (PDRAM), user memory and vendor memory, the NVRAM Controller will send a signal to disable the host acknowledge signal
- Reprogramming the Serial (Slave) device address is described in Section 4.7

The host accesses internal memories using serial device addresses A0h and A2h. Since the host has an 8 bit address interface, to access to all 16k memory locations, the memory is partitioned into 128-byte tables. A table select byte (TSB) is used to provide indirect addressing to each table. The TSB must proceed each read or write access except when a consecutive read or write occurs within the same table already accessed.

The host interface memory map is defined in Table 4-1.

Table 4-1. SFP/DDMI Memory Map

Serial Device Address	Table	Data Address (decimal)	SFF-8472 Description	M02172 Description
A0h (SFP)	00h Lower	0-95	Serial ID	Serial ID
		96-127	Vendor Specific	Vendor Specific
	00h Upper	128-255	Reserved SFF-8079	Reserved SFF-8079
A2h (DDMI)	00h Lower	0-55	Alarm and Warning Thresholds	Diagnostics 1
		56-95	Calibration Constants	
		96-119	Real Time Diagnostic Interface	Diagnostics 2
		120-122	Vendor Specific	Firmware Revision
		123-126		Password Entry
		127		Table Select Byte
	00h Upper	128-247	User Writable Memory	User Memory
		248-255	Vendor Specific	Vendor Specific
A2h (DDMI)	01h Upper	128-255	N/A	User Memory
	02h Upper	128-255	N/A	Vendor Memory
	03h - 04h Upper	128-255	N/A	Device Registers
	05h - 7Ah Upper	128-255	N/A	Program and Data Memory

For serial device address A2h, the lower data addresses always reference the same information regardless of the actual Table Select Byte value (i.e., the diagnostic information is always accessible). The default table for serial device address A2h (or whatever it may be reprogrammed to be) is 00h (i.e. the DDMI specified data fields).

The memory is further partitioned into functional groups, each of which has configurable access permissions and password protection. There are four programmable password configurations. This flexible access methodology allows the module manufacturer to customize access models for a variety of purposes or intended users.

Table 4-2. M02172 DDMI Memory Partitioning (default serial device address A2h)

Data Address (decimal)	Table Select Byte (TSB)					
	00		01	02	03-04	05-7Ah
00 95	Diag 1	DDMI Diagnostics	All lower 128 bytes with table select byte > 0 map to the lower 128 bytes at table 00h			
96 119	Diag 2					
120 127	Vendor Specified (used by MACOM)					
128 247	Reserved		User Memory	Vendor Memory	Device Registers	...Program/Data... (PDRAM)
248 255	Vendor Specified					

Each memory partition is assigned a bit in the read and write access permission registers for each password level.

4.5 Password Protection

Passwords are entered by writing to the password entry bytes (see address A2h 123-126d in Table 4-1). These along with the table select byte are accessible without a password. The on-chip memory is protected from unauthorized access from the host interface by 3 levels (lowest to highest, 0 - 2) of 32-bit passwords.

The access restrictions for each password level is configurable to allow read or write access to different blocks of memory. The memory is partitioned into nine sections as listed in Table 4-3 with each level allowing unique password access.

Table 4-3. The Nine SFP/DDMI Memory Password Protection Partitions

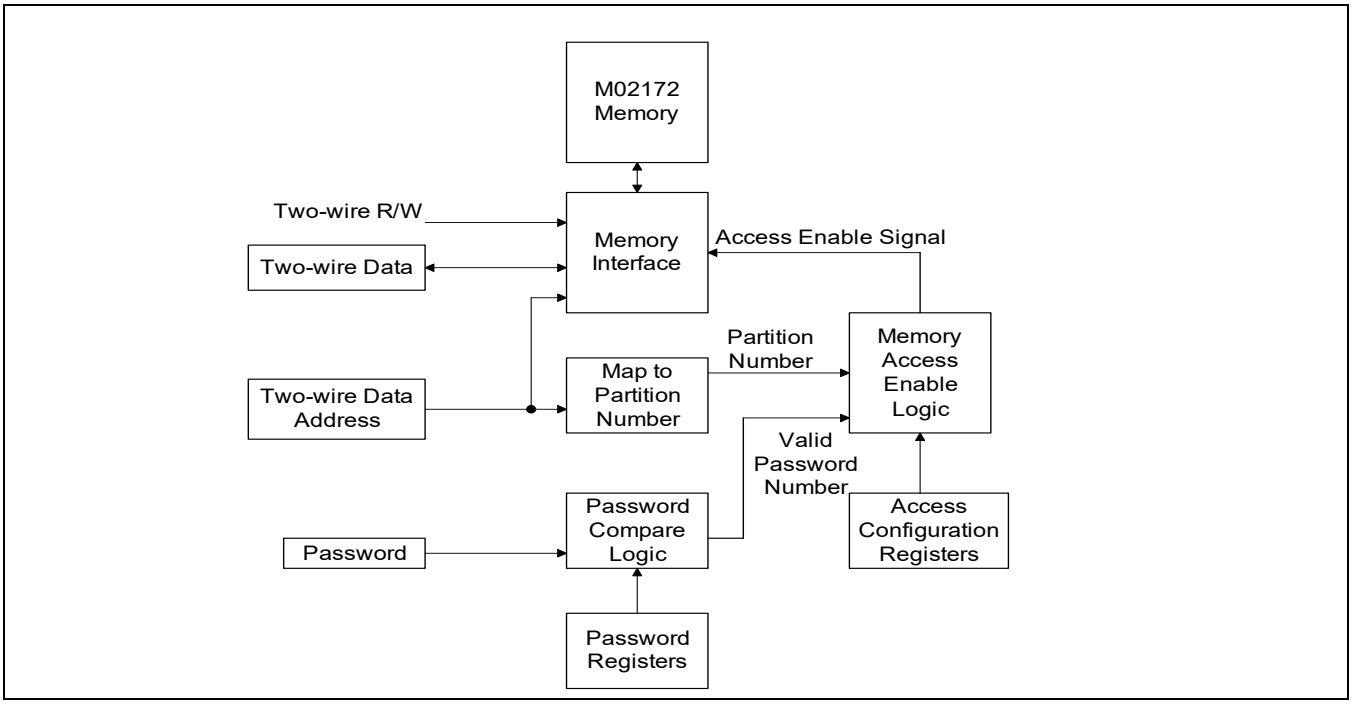
Memory Section	Data Address			Allowable Password Control Level
	Serial Device Address	Table	Address (decimal)	
Diagnostics 1	A2	00h Lower	0-95	0-2
Diagnostics 2	A2	00h Lower	96-119	
Serial ID	A0	00h Lower	0-95	
User	A2	00h Upper	128-247	
	A2	01h Upper	128-255	
Vendor	A0	00h Lower	96-127	
	A2	00h Lower	120-122	
	A2	00h Upper	248-255	
	A2	02h Upper	128-255	
Reserved	A0	00h Upper	128-255	
Program/Data	A2	≥05h Upper	128-255	
Device Registers 1	A2	03h Upper	128-255	
Device Registers 2	A2	04h Upper	128-255	

For each access level, there are internal configuration registers for read access and for write access. The control of access to the on-chip memory is illustrated in Figure 4-5. To access the memory, the host must write a 32-bit password to the appropriate DDMI memory location (see address A2h 123-126d in Table 4-1). The entered password is compared to the four passwords (one for each access level) stored internally. The current access level is defined as that corresponding to the matching password. If the entered password matches none of the stored passwords, access defaults to the lowest level (0 is the lowest level, 2 is the highest level).

The access configuration registers for the current access level defines whether access is enabled to a given memory partition. When the host attempts to access the on-chip memory, the data address is first mapped to a memory partition number. The corresponding bit of the access configuration registers for the current access level are then checked to determine if access should be enabled for this partition. If access is enabled, the memory interface is then allowed to perform the requested access. An example of access definition, using the MACOM supplied software the vendor could configure the level 0 access for read-only for Diagnostics 1 and Diagnostics 2 while all memory is write protected.

Note that the vendor is given complete password control with the MACOM supplied M02172 configuration software. Using the supplied software, the vendor defines the password for each access level and the level of access for the nine SFP/DDMI Memory Password Protection Partitions shown in Table 4-3.

Figure 4-5. Password Access Control Architecture



4.6 Two-Wire Serial Interface

4.6.1 SFP/SFP+ Compliant interface

- SFP/SFP+SFP/SFP+ data read accessible via two-wire serial interface with serial device address A0h (re-programmable).
- SFP/SFP+ data writable via two-wire serial interface with multiple levels of password protection.
- SFP/SFP+ data downloaded from external EEPROM to on-chip RAM after module powers up.
- M02172 internal device controller does not alter SFP/SFP+ data.
- 15Mhz maximum clock rate.
- If the host alters the SFP/SFP+ data, it must supply a checksum at address 3Fh (automatic backup to external EEPROM initiated without interruption access from the host).

4.6.2 DDMI Compliant interface

- Fully SFF-8472 compliant.
- DDMI data read accessible via two-wire interface with serial device address A2h (re-programmable).
- DDMI data writable via two-wire serial interface with multiple levels of password protection.
- DDMI data downloaded from external EEPROM to on-chip RAM after module powers up.

- 400Khz maximum clock rate.
- If the host alters the DDMI data, it must supply a checksum at address 0x3F and 0x5F (automatic backup to external EEPROM initiated without interruption access from the host).

4.6.3 HOST Interface Details

In accordance with SFP/SFP+ MSA and SFF-8472, the M02172 incorporates a two-wire interface that uses the serial EEPROM protocol defined for the Atmel AT24C01A/02/04 family of products. The interface consists of a serial input clock line (SCL, Mod Def 1) and a serial, bi-directional data line (SDA, Mod Def 2). SCL and SDA are each pulled up with an external resistor.

Table 4-4. Two-Wire Interface

Pin	Function	Description
MD1/SCL	Mod-Def 1/Serial Clock	Clock input (open drain)
MD2/SDA	Mod-Def 2/Serial Data	Data input/output (open drain)

During data transmission, SDA can only transition while SCL is low. Changes on SDA when SCL is high indicates a start or stop condition which initiates or terminates the transmission. A start condition occurs when SDA transitions from high to low when SCL is high. Conversely, a low to high transition on SDA when SCL is high indicates a stop condition. The start condition is followed by the device address (A0h for SFP/SFP+ and A2h for DDMI). The data address is transmitted following the device address which is followed by transmission of the data. The M02172 responds to each byte of data with an acknowledgment which is a zero following the received byte. The device can receive data a byte at a time or in sixteen byte sequences (page mode). The transmission is then terminated with the stop condition.

4.6.4 Four-wire SPI Interface Details

For those applications requiring faster programming and read back than an I2C interface can provide, an SPI interface is also provided. When SPI_Sel is high, the 4-wire SPI interface is selected. If SPI_Sel =0, the device returns to the existing 2-wire Interface (MOD_DEF1 and MOD_DEF2) with GPIO[1] and $\overline{SS}$ inputs ignored.

Table 4-5. Four-Wire Serial Interface Description

Pin	Function	Description
SS	Slave Select	Active Low. Allowing SS to return high, changes communication backhoe I2C
SCK	Serial Clock	10MHz maximum
SI	Slave Input	MOD_DEF2 (Data input)
SO	Slave Output	MOD_DEF1 (Data output)

After the transition high-to-low of $\overline{SS}$, the SPI Master will transfer a1 byte instruction (one of 4 instructions at table 1) following by a 1-byte address and 1-byte data for write mode and so forth. SI is sampled by the rising edge of SCK and SO is clocked out by falling edge of SCK. For an SPI Master, SO is sampled by the rising edge of SCK and SI is clocked out by the falling edge of SCK.

Table 4-6. SPI Instructions

Instruction Name	Instruction Format	$\overline{SS}$ at end of current read/write operation	Operation
R-Read	PDDDDx11	H	Random Read
R-Write	xxxxxx10	H	Random Write
S-Read	PDDDDx11	L	Sequential Read
S-Write	xxxxxx10	L	Sequential Write

As a result, the read command changes to: “PDDDD_X11; the Random/Sequence Read command. Where the P bit refers to whether or not the programmable delay mode is turned on or off. The DDDD bits represent the number of cycles by which the read is delayed. For reliable operation, it is recommended that 3 to 8 SPI clock cycles be programmed. (With a 10 MHZ SPI clock). The X’s are don't cares. When P=1, the programmable delay is turned on, and the read value is delayed by the number represented by DDDD bits. For example: If DDDD = 0100, then the read value is output after a 4 cycle delay. DDDD = 1000 means that the read value is output after an 8 cycle delay. When P = 0, the programmable mode is turned off, and the read value is output after a default 8 cycles delay.

SPI Timing Application Notes:

- If the two LSB of the instruction byte are not 11 or 10, no read/write cycle is executed and the SO pin remains tri-stated.
- There are no different instructions for Random R/W and sequential R/W. When slave select, $\overline{SS}$ is extended by n*8-spi clock cycles, and a Random R/W becomes a sequential R/W as in the sequential write timing diagram.
- The sequential R/W continues to roll over the 256 byte addresses if $\overline{SS}$ is extended low.
- A minimum of one SPI clock cycle pulse width is required for Slave Select ($\overline{SS}$) to be deselected between Read-Read, Read-Write, Write-Read, or Write-Write modes.
- At least one SPI clock cycle is required after Slave select $\overline{SS}$ is deasserted.
- As in the two wire slave interface, the SPI interface reserves HOST address 0x7F for table select. Each 128-byte table definition remains as before (at two wire slave address A2h). For example, writing 03h to table select address 0x7F, selects table 0x3, following by a R/W to any address from 0x80 to 0xFF, giving access to Host locations 0x80 to 0xFF.
- SPI Host Read/Writes to any lower addresses (0x00 to 0x7E and 0x7F) are mapped to the 128 byte common area of Diagnostics 1, Diagnostics 2, Vendor specific, Password Entry and Table Select defined in the lower page.
- To access the 256-byte SFP (former two wire slave) address A0h(from two wire interface mode), writing **80**
- **h** (for the lower 128 bytes) and **81h** (for the upper 128 bytes) to table select is required. After writing **80h** or **81h** to table select, SPI host addresses (0x80 to 0xFF) are mapped to the lower 128 bytes or upper 128 bytes of SFP memory.
- Note: it is up to the user to terminate the extension of $\overline{SS}$ in sequential write and change the table select since it can be rolled over 256 bytes address which can roll to lower addresses and data are written to the common area. For example, start writing at address 0xC0 in sequential Write: 0xC0, 0xC1 …….0xFF, 0x00, 0x01 …….0x7E (table select), 0x7F, 0x80, ……. 0xC0, 0xC1 …. 0xFF…….

Figure 4-6. SPI Random Read

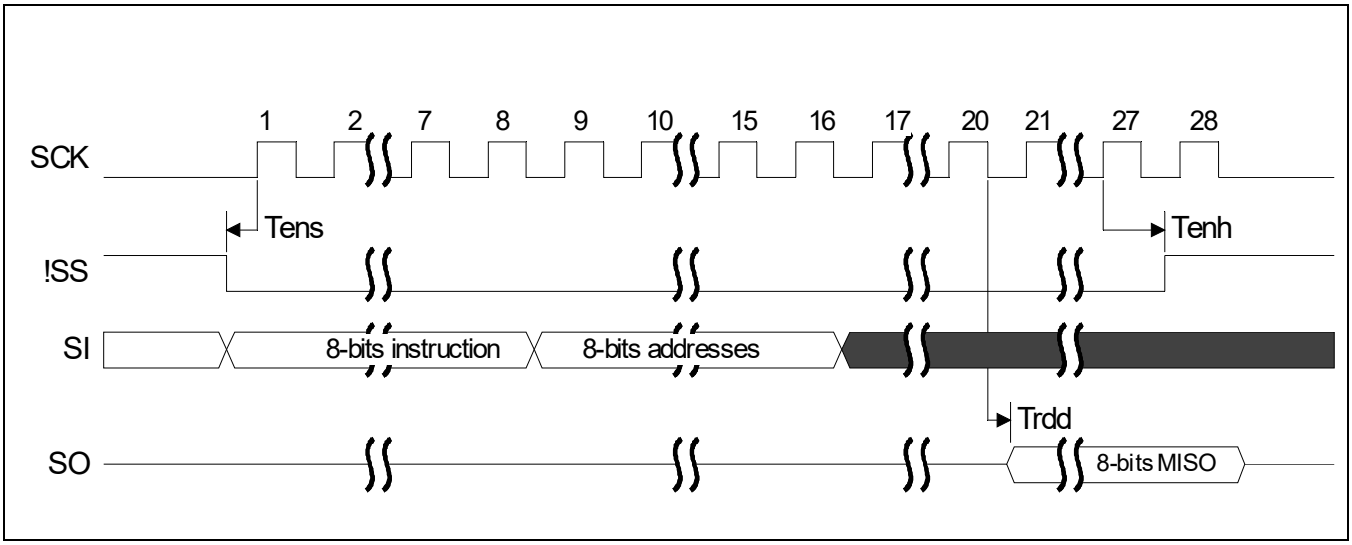


Figure 4-7. SPI Random Write

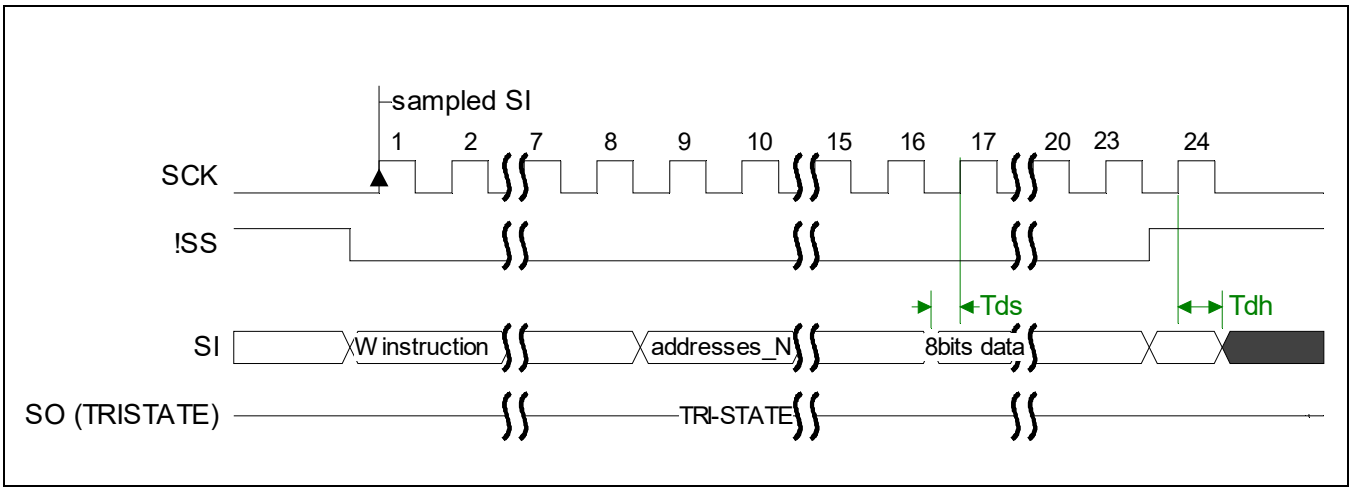


Figure 4-8. SPI Sequential Read

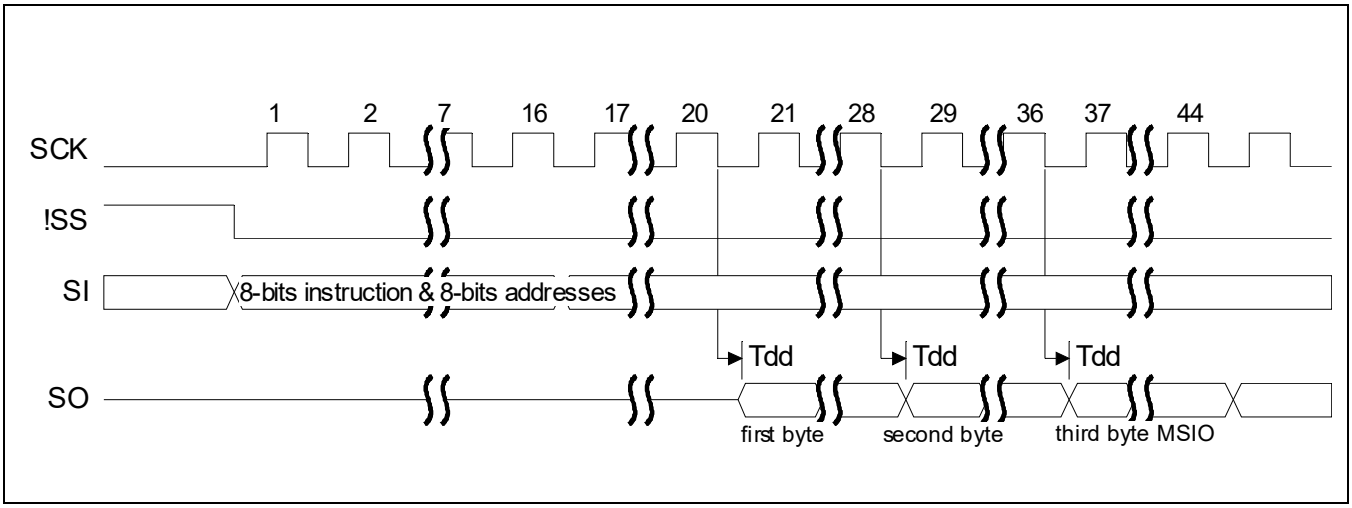
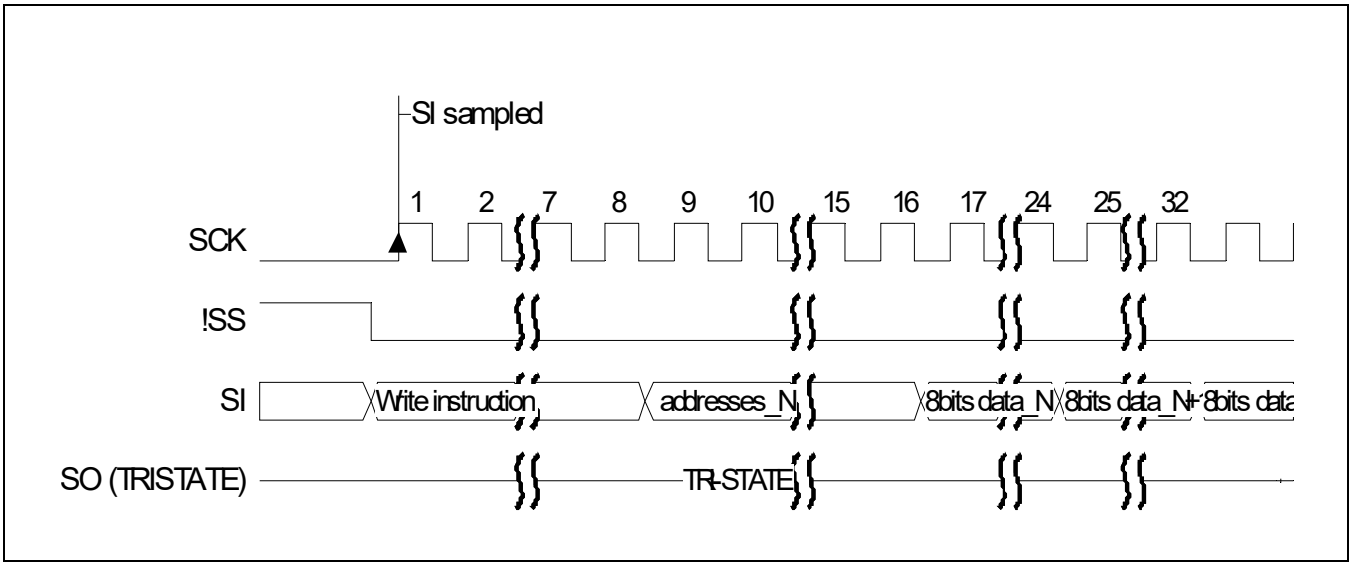


Figure 4-9. SPI Sequential Write



4.7 Reprogramming the Serial Device Address

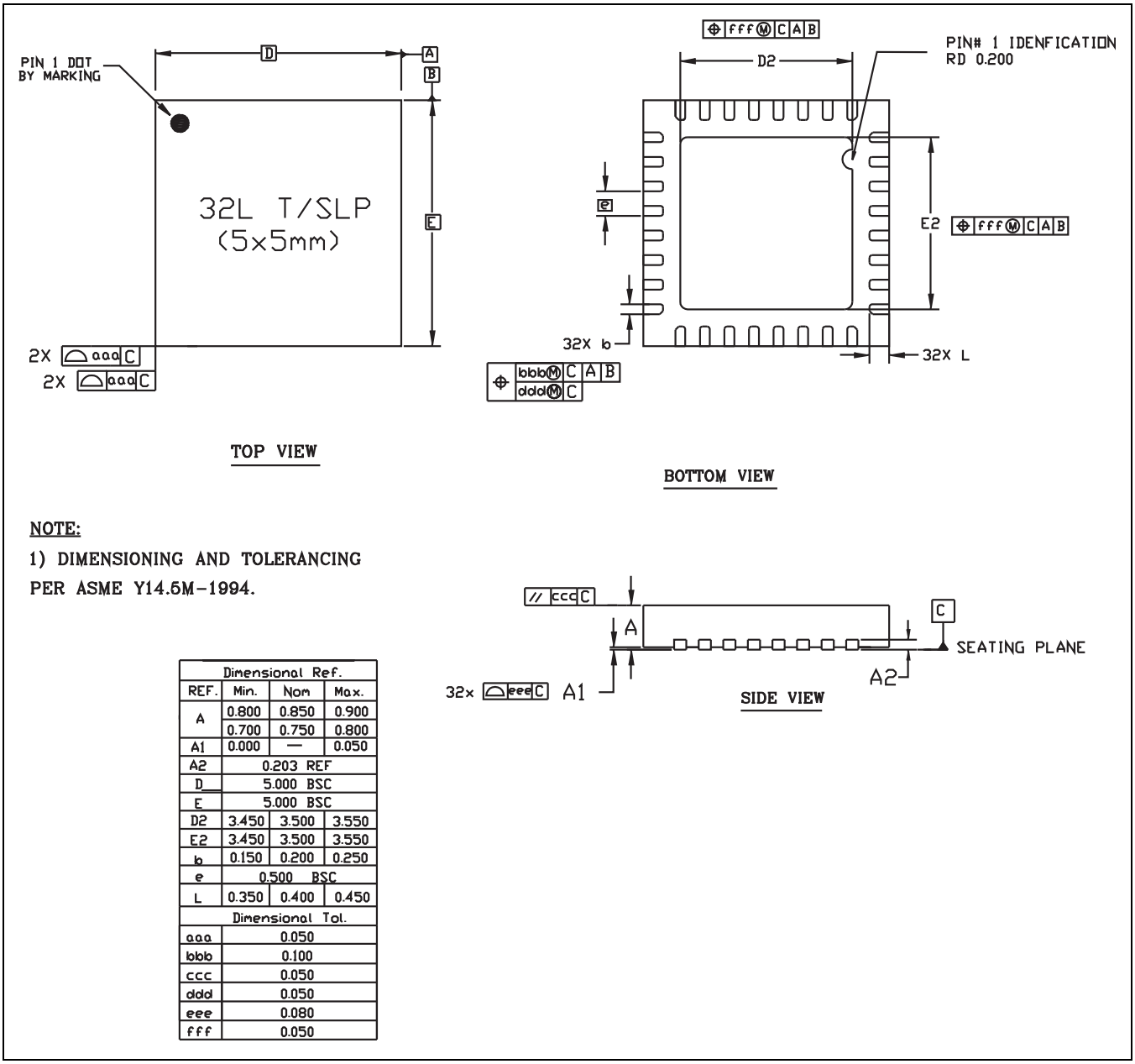
When more than one device is sharing the two-wire interface it will be necessary to change the serial device address of each module to allow the host independent access to each module. This is accomplished using the Two-wire Serial Control Register that when set, redefines how the TX_DIS pin is interpreted by the M02172. In this mode, if TX_DIS is high, the M02172 will not respond to any serial device address from the host interface. If TX_DIS is low, the M02172 will respond when the serial device address is its own, allowing the particular device to be accessed (TX_DIS is performing as a device select pin).

When the host sets this control bit, all modules will be placed in this reprogramming mode. Individually selecting a module through an individual module's TX_DIS pin allows the modules address to be uniquely programmed. Module addresses are 8 bit words. The LSB selects a read or write operation and is not part of the address. The second bit is defined to be a zero for SFP and a one for DDMI, thus DDMI addresses are always 2 greater than the SFP addresses in a module (e.g. A0h and A2h the default SFP and DDMI addresses). This means that the first six MSBs are what constitute the unique module address. The serial device address is held in the Physical Address Control Register. Only one address is written. The reprogrammed address is now the SFP serial device address. As detailed above, the DDMI serial device address is now an increment of 2 greater than the SFP address.

Once each module has had its address reprogrammed, to exit this reprogramming mode is accomplished by again using the Two-wire Serial Control Register to define the TX_DIS pin to its normal function. This operation must be performed on each module as they now each possess a unique serial device address.

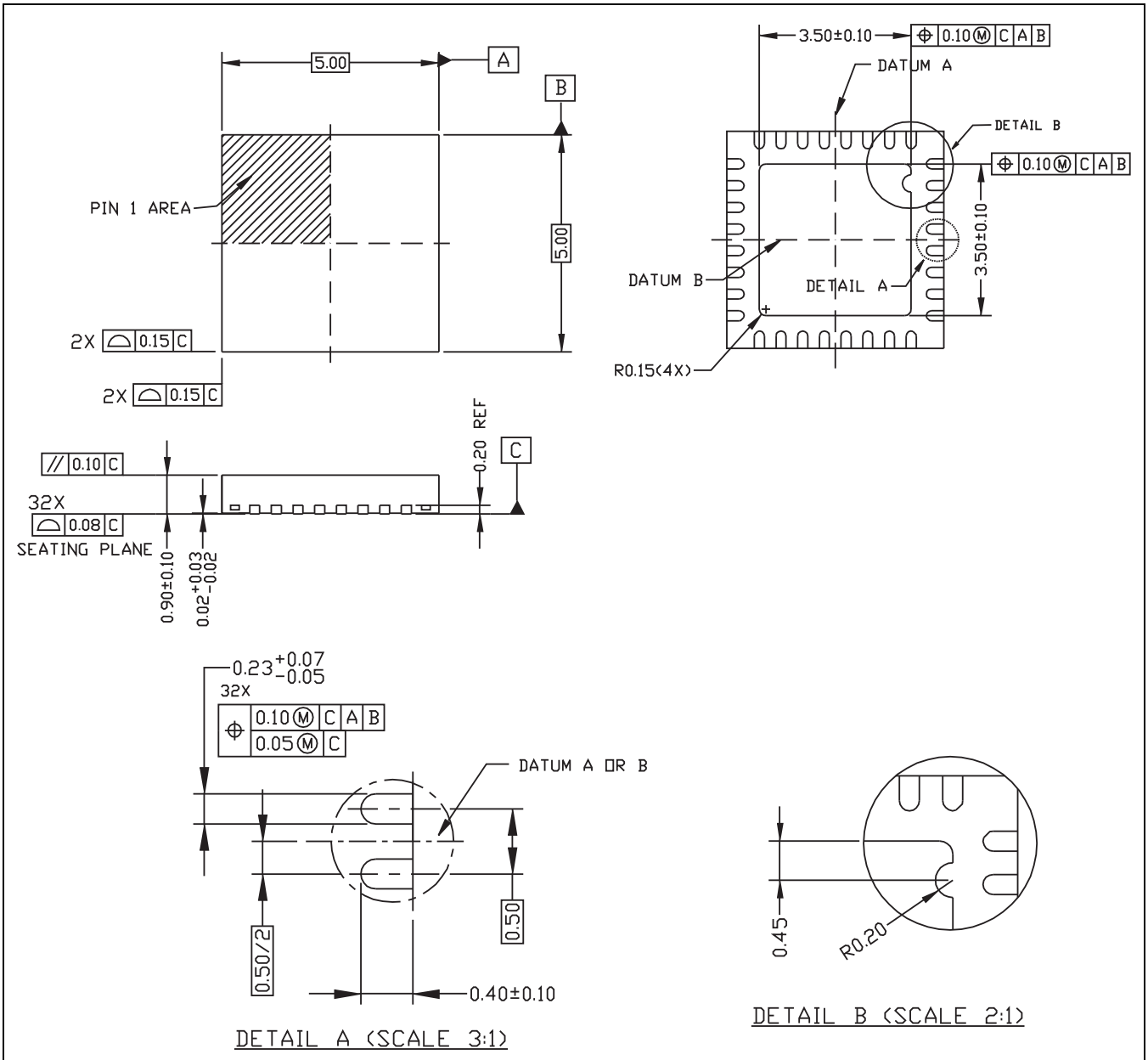
5.0 Package Specification

Figure 5-1. QFN32 Package Information (Unisem)



Dimensional Ref.			
REF.	Min.	Nom	Max.
A	0.800	0.850	0.900
	0.700	0.750	0.800
A1	0.000	—	0.050
A2	0.203 REF		
D	5.000 BSC		
E	5.000 BSC		
D2	3.450	3.500	3.550
E2	3.450	3.500	3.550
b	0.150	0.200	0.250
e	0.500 BSC		
L	0.350	0.400	0.450
Dimensional Tol.			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

Figure 5-2. QFN32 Package Information (ASEM)



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

6.0 Control Register Map and Description

Control Registers Map and Descriptions

6.1 Register Summary

Table 6-1. Register Summary - These registers are located at I2C address (7-bit) 00h

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Dflt	R/W
Table 3 Registers												
03h	80h	EEC_CTRL	*RSVD*		dis_rd_ddmi_block	dload_select	operation				00h	R/W (SC)
03h	81h	SERIAL_CTRL	*RSVD*				reprogram_en	2wire_sec_mode	2wire_mode	boot_mode_en	00h	R/W
03h	8Ah	EEC_STAT_0	*RSVD*	smm_state			sda_output_en	timeout_error	page_chksum_error	*RSVD*	08h	R
03h	8Bh	EEC_STAT_1	checksum								00h	R
03h	8Ch	EEC_STAT_2	bit_count				smi_state				00h	R
03h	8Dh	EEC_STAT_3	byte_count					smi_command			00h	R
03h	8Eh	GPIO_SAMPLE	gpio_in_smp_rate								00h	R/W
03h	8Fh	GPIO_MASK	*RSVD*				gpio3_irq_mask	gpio2_irq_mask	gpio1_irq_mask	gpio0_irq_mask	00h	R/W
03h	90h	GPIO_OUT	*RSVD*		gpio4_out_en	gpio4_out_val	gpio3_out_val	gpio2_out_val	gpio1_out_val	gpio0_out_val	00h	R/W
03h	91h	GPIO0_CTRL	*RSVD*		gpio0_intr_trig		gpio0_mode		*RSVD*		08h	R/W
03h	93h	GPIO1_CTRL	*RSVD*		gpio1_intr_trig		gpio1_mode		*RSVD*		08h	R/W
03h	95h	GPIO2_CTRL	*RSVD*		gpio2_intr_trig		gpio2_mode		*RSVD*		08h	R/W
03h	97h	GPIO3_CTRL	*RSVD*		gpio3_intr_trig		gpio3_mode		*RSVD*		08h	R/W
03h	99h	GPIO_IRQ	*RSVD*		2wire_sec_mode_status	2wire_mode_status	gpio3_irq	gpio2_irq	gpio1_irq	gpio0_irq	00h	R
03h	9Bh	UC_CTRL_1	*RSVD*					uc_disable	access_done	dload_done	00h	R
03h	9Ch	GPIO_IN	gpio3_in	gpio2_in	gpio1_in	gpio0_in	gpio4_in	*RSVD*			00h	R
03h	B5h	PHY_ADDR	*RSVD*		phy_addr						00h	R/W
03h	B7h	RX_CTRL	*RSVD*							rx_los	00h	R
03h	B8h	LASER_CTRL0	soft_scb	sb_in	soft_cc_sel	dis_mod_rst	pd_polarity_swap	*RSVD*	offset_en	pwa_en	00h	R/W
03h	B9h	LASER_CTRL1	datadetect_en	polarity_swap	ignore_ipin	bias_comp	reset_fail	latch_overdrive	hold_monitors	soft_fail	40h	R/W
03h	BBh	LASER_STAT0	cf_ibout	ssb_status	state_of_dis_pin	*RSVD*	status_spi_sel	status_ccsel	status_fail	laser_status	00h	R
03h	BCh	LASER_STAT1	status_pwdn_rst	vcc3_status	data_detect	ipin_low	ipin_high	biasr_status	dvdd_status	outp_status	00h	R
03h	BDh	MOD_CTRL	*RSVD*	mcu_temp_comp	bm_copy	temp_sel	*RSVD*		mod_temp_comp	bias_temp_-comp	02h	R/W
03h	BEh	MOD_SET_0	modulation_target[7:0]								00h	R/W

Table 6-1. Register Summary - These registers are located at I2C address (7-bit) 00h

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Dflt	R/W
03h	BFh	MOD_SET_1	*RSVD*				modulation_target[11:8]				00h	R/W
03h	C0h	MOD_CLIP_0	mod_max[7:0]								00h	R/W
03h	C1h	MOD_CLIP_1	*RSVD*				mod_max[11:8]				00h	R/W
03h	C2h	MOD_CUR_MON_0	mod_mon[7:0]								00h	R
03h	C3h	MOD_CUR_MON_1	*RSVD*				mod_mon[11:8]				00h	R
03h	C4h	MOD_CUR_CTRL	*RSVD*				mod_adc_cal	mod_adc_pd	*RSVD*		08h	R/W
03h	C5h	BIAS_CTRL	*RSVD*				tpm_copy	apc_cntrl	*RSVD*		00h	R/W
03h	C6h	BIAS_CUR_MON_0	bias_mon[7:0]								00h	R
03h	C7h	BIAS_CUR_MON_1	*RSVD*				bias_mon[11:8]				00h	R
03h	C8h	BIAS_CUR_CAL_0	bias_mon_cal[7:0]								00h	R/W
03h	C9h	BIAS_CUR_CAL_1	*RSVD*				bias_mon_cal[11:8]				00h	R/W
03h	CAh	BIAS_CUR_CTRL	*RSVD*				bias_adc_cal	bias_adc_pd	*RSVD*		08h	R/W
03h	CBh	SUPPLY_MON_0	supply_mon[7:0]								00h	R
03h	CCh	SUPPLY_MON_1	*RSVD*				supply_mon[11:8]				00h	R
03h	CDh	SUPPLY_CTRL	*RSVD*				supply_adc_cal	supply_adc_pd	cal_adj[1:0]		09h	R/W
03h	CEh	AUX1_MON_0	aux1_val[7:0]								00h	R
03h	CFh	AUX1_MON_1	*RSVD*				aux1_val[11:8]				00h	R
03h	D0h	AUX1_CTRL	*RSVD*				aux1_adc_cal	aux1_adc_pd	aux1_adc_dir	aux1_adc_sel	08h	R/W
03h	D1h	RX_PWR_MON_0	rx_pwr_mon[7:0]								00h	R
03h	D2h	RX_PWR_MON_1	*RSVD*				rx_pwr_mon[11:8]				00h	R
03h	D3h	RX_PWR_CTRL	*RSVD*				rx_pwr_adc_cal	rx_pwr_adc_pd	*RSVD*		08h	R/W
03h	D4h	TX_PWR_MON_0	tx_pwr_mon[7:0]								00h	R
03h	D5h	TX_PWR_MON_1	*RSVD*				tx_pwr_mon[11:8]				00h	R
03h	D6h	TX_PWR_CAL_0	tx_pwr_cal[7:0]								00h	R/W
03h	D7h	TX_PWR_CAL_1	*RSVD*				tx_pwr_cal[11:8]				00h	R/W
03h	D8h	TX_PWR_CTRL	*RSVD*				tx_pwr_adc_cal	tx_pwr_adc_pd	*RSVD*		08h	R/W
03h	DCh	AUX2_VAL_0	aux2_val[7:0]								00h	R
03h	DDh	AUX2_VAL_1	*RSVD*				aux2_val[11:8]				00h	R
03h	DEh	AUX2_CTRL	*RSVD*				aux2_adc_cal	aux2_adc_pd	aux2_adc_dir	aux2_adc_sel	09h	R/W
03h	DFh	TEMP_MON_0	temp_mon[7:0]								00h	R
03h	E0h	TEMP_MON_1	*RSVD*				temp_mon[11:8]				00h	R
03h	E1h	TEMP_MON_CTRL	*RSVD*				temp_mon_cal	temp_mon_pd	*RSVD*		09h	R/W
03h	E2h	TEMP_START_0	temp_start[7:0]								00h	R/W
03h	E3h	TEMP_START_1	*RSVD*				temp_start[11:8]				00h	R/W
03h	E4h	TEMP_COEF	*RSVD*			temp_coef[4:0]					00h	R/W
03h	E7h	APC_SET_0	apc_set[7:0]								00h	R/W

Table 6-1. Register Summary - These registers are located at I2C address (7-bit) 00h

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Dflt	R/W
03h	E8h	APC_SET_1	*RSVD*				apc_set[11:8]				00h	R/W
03h	E9h	APC_CLIP_0	apc_clip[7:0]								00h	R/W
03h	EAh	APC_CLIP_1	*RSVD*				apc_clip[11:8]				00h	R/W
03h	EBh	GAIN_CTRL	*RSVD*		ba_gain_ctrl[3:0]				apc_gain_ctrl		00h	R/W
03h	ECh	APC_FDB_MON_0	apc_fdb_mon[7:0]								00h	R
03h	EDh	APC_FDB_MON_1	apc_fdb_mon[15:8]								00h	R
03h	EEh	APC_FDB_MON_2	*RSVD*		apc_fdb_mon[21:16]						00h	R
03h	EFh	BIAS_DAC_CODE_0	bias_dac[7:0]								00h	R
03h	F0h	BIAS_DAC_CODE_1	*RSVD*				bias_dac[11:8]				00h	R
03h	F1h	BIAS_DAC_CTRL	*RSVD*						bias_dac_hp	bias_dac_pd	00h	R/W
03h	F2h	MOD_DAC_CODE_0	mod_dac[7:0]								00h	R
03h	F3h	MOD_DAC_CODE_1	*RSVD*				mod_dac[11:8]				00h	R
03h	F4h	MOD_DAC_CTRL	*RSVD*						mod_dac_hp	mod_dac_pd	00h	R/W
03h	F5h	PULSEW_DAC_CODE	*RSVD*		pwa_dac[5:0]						00h	R/W
03h	F6h	PULSEW_DAC_CTRL	*RSVD*						pulsew_dac_hp	pulsew_dac_pd	00h	R/W
03h	F7h	6BIT_DAC2	*RSVD*		6bit_dac2[5:0]						00h	R/W
03h	F8h	6BIT_DAC2_CTRL	*RSVD*						6bit_dac2_hp	6bit_dac2_pd	00h	R/W
03h	F9h	6BIT_DAC1	*RSVD*		6bit_dac1[5:0]						00h	R/W
03h	FAh	6BIT_DAC1_CTRL	*RSVD*					6bit_dac1_sink	6bit_dac1_hp	6bit_dac1_pd	00h	R/W
03h	FBh	10B_DAC_CODE_0	10bit_dac[7:0]								00h	R/W
03h	FCh	10B_DAC_CODE_1	*RSVD*						10bit_dac[9:8]		00h	R/W
03h	FDh	10B_DAC_CTRL	*RSVD*					output_mode	10bit_dac_hp	10bit_dac_pd	00h	R/W
Table 4 Registers												
04h	80h	PWD0_0	pwd_level0 [7:0]								00h	R/W
04h	81h	PWD0_1	pwd_level0[15:8]								00h	R/W
04h	82h	PWD0_2	pwd_level0[23:16]								00h	R/W
04h	83h	PWD0_3	pwd_level0[31:24]								00h	R/W
04h	84h	PWD1_0	pwd_level1[7:0]								00h	R/W
04h	85h	PWD1_1	pwd_level1[15:8]								00h	R/W
04h	86h	PWD1_2	pwd_level1[23:16]								00h	R/W
04h	87h	PWD1_3	pwd_level1[31:24]								00h	R/W
04h	88h	PWD2_0	pwd_level2[7:0]								00h	R/W
04h	89h	PWD2_1	pwd_level2[15:8]								00h	R/W
04h	8Ah	PWD2_2	pwd_level2[23:16]								00h	R/W
04h	8Bh	PWD2_3	pwd_level2[31:24]								00h	R/W
04h	90h	RD_ACCESS0_0	tbl3_pw0_r	pgrm_pw0_r	sfp_rsvd_pw0_r	vnd_spcfc_pw0_r	usr_wrt_pw0_r	ser_id_pw0_r	diag2_pw0_r	diag1_pw0_r	00h	R/W

Table 6-1. Register Summary - These registers are located at I2C address (7-bit) 00h

Page	Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Dflt	R/W
04h	91h	RD_ACCESS0_1	*RSVD*							tbl4_pw0_r	00h	R/W
04h	92h	RD_ACCESS1_0	tbl3_pw1_r	pgrm_pw1_r	sfp_rsvd_pw1_r	vnd_spcfc_pw1_r	usr_wrt_pw1_r	ser_id_pw1_r	diag2_pw1_r	diag1_pw1_r	00h	R/W
04h	93h	RD_ACCESS1_1	*RSVD*							tbl4_pw1_r	00h	R/W
04h	94h	RD_ACCESS2_0	tbl3_pw2_r	pgrm_pw2_r	sfp_rsvd_pw2_r	vnd_spcfc_pw2_r	usr_wrt_pw2_r	ser_id_pw2_r	diag2_pw2_r	diag1_pw2_r	00h	R/W
04h	95h	RD_ACCESS2_1	*RSVD*							tbl4_pw2_r	00h	R/W
04h	96h	RD_ACCESS3_0	tbl3_pw3_r	pgrm_pw3_r	sfp_rsvd_pw3_r	vnd_spcfc_pw3_r	usr_wrt_pw3_r	ser_id_pw3_r	diag2_pw3_r	diag1_pw3_r	00h	R/W
04h	97h	RD_ACCESS3_1	*RSVD*							tbl4_pw3_r	00h	R/W
04h	98h	WR_ACCESS0_0	tbl3_pw0_w	pgrm_pw0_w	sfp_rsvd_pw0_w	vnd_spcfc_p-w0_w	usr_wrt_pw0_w	ser_id_pw0_w	diag2_pw0_w	diag1_pw0_w	00h	R/W
04h	99h	WR_ACCESS0_1	*RSVD*							tbl4_pw0_w	00h	R/W
04h	9Ah	WR_ACCESS1_0	tbl3_pw1_w	pgrm_pw1_w	sfp_rsvd_pw1_w	vnd_spcfc_p-w1_w	usr_wrt_pw1_w	ser_id_pw1_w	diag2_pw1_w	diag1_pw1_w	00h	R/W
04h	9Bh	WR_ACCESS1_1	*RSVD*							tbl4_pw1_w	00h	R/W
04h	9Ch	WR_ACCESS2_0	tbl3_pw2_w	pgrm_pw2_w	sfp_rsvd_pw2_w	vnd_spcfc_p-w2_w	usr_wrt_pw2_w	ser_id_pw2_w	diag2_pw2_w	diag1_pw2_w	00h	R/W
04h	9Dh	WR_ACCESS2_1	*RSVD*							tbl4_pw2_w	00h	R/W
04h	9Eh	WR_ACCESS3_0	tbl3_pw3_w	pgrm_pw3_w	sfp_rsvd_pw3_w	vnd_spcfc_p-w3_w	usr_wrt_pw3_w	ser_id_pw3_w	diag2_pw3_w	diag1_pw3_w	00h	R/W
04h	9Fh	WR_ACCESS3_1	*RSVD*							tbl4_pw3_w	00h	R/W
04h	D4h	DIG_FILT_BPASS	*RSVD*			bias_cur_val	aux_val	rx_pwr_val	ext_cur_val	ext_temp_val	00h	R/W
04h	D5h	DIG_FILT_CTRL	*RSVD*			dig_filt_gain			dig_filt_div		1Ah	R/W
04h	D6h	BIAS_CUR_FINAL_0	bias_curr_final[7:0]								00h	R
04h	D7h	BIAS_CUR_FINAL_1	*RSVD*				bias_curr_final[11:8]				00h	R
04h	D8h	AUX_FINAL_0	aux_final[7:0]								00h	R
04h	D9h	AUX_FINAL_1	*RSVD*				aux_final[11:8]				00h	R
04h	DAh	RX_PWR_FINAL_0	rx_pwr__final[7:0]								00h	R
04h	DBh	RX_PWR_FINAL_1	*RSVD*				rx_pwr__final[11:8]				00h	R
04h	DEh	EXT_TEMP_FINAL_0	ext_temp_final[7:0]								00h	R
04h	DFh	EXT_TEMP_FINAL_1	*RSVD*				ext_temp_final[11:8]				00h	R
04h	E0h	A_LASER_CTRL2	oc2	oc1	oc0	core_comp	lr_comp_off	t_comp_off	bias_mon_mag	short_z_offset	00h	R/W
04h	E1h	A_LASER_CTRL3	c_off	measure_rpoly	measure_ib	soft_tx_dis	eq1	eq_on	bias_ratio1	bias_ratio0	00h	R/W
04h	E2h	A_LASER_CTRL4	beta_comp1	beta_comp0	tc2_off	dcd_cor_on	edge_sel	soft_rs1_rate	hard_rs1_en	rs1_rate	00h	R/W
04h	E3h	LASER_STAT2	*RSVD*	eml_mode	*RSVD*						40h	R
04h	E6h	ANALOG_CTRL	*RSVD*					rxp_volcur_ctrl	imax_ctrl	*RSVD*	00h	R/W

6.2 Table Select 03h Register Details

Page: 03h
Address: 80h
Register Name: EEC_CTRL
Default Value: 00h
Description: EEC Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R/W
5	dis_rd_ddmi_block	0b: enable to block during Host read 24 byte DDMI 0x60 – 0x77 1b: disable to block during Host read 24 byte DDMI 0x60 – 0x77	0b	R/W
4	dload_select	0b: download 15k PDRAM 1b: download 8k PDRAM	0b	R/W
3:0	operation	0000b: No Operation **Valid only in two-wire serial mode.** 0001b: Read-back chip registers (256Bytes) 0010b: Read-back SFP registers (256Bytes) 0011b: Read-back DDMI registers (256Bytes) 0100b: Read-back User/Vendor memory (256Bytes) 0101b: Read-back PDRAM (15KBytes) 0110b: Write-back chip registers (256Bytes) 0111b: Write-back SFP registers and update checksum (256Bytes+) 1000b: Write-back DDMI registers and update checksum (256Bytes+) 1001b: Write-back User/Vendor memory and update checksum (256Bytes+) 1010b: Write-back PDRAM and update checksum (15Kbytes+) 1011b - 1111b: Reserved	0000b	SC

Page: 03h
Address: 81h
Register Name: SERIAL_CTRL
Default Value: 00h
Description: Two-wire Serial Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R/W
3	reprogram_en	0b: enable to block during Host read 24 byte DDMI 0x60 – 0x77 1b: disable to block during Host read 24 byte DDMI 0x60 – 0x77	0b	R/W

Bit(s)	Name	Description	Default	Type
2	2wire_sec_mode	0b: Enable uC mode. uC has control of all memories. 1b: Enable two-wire serial secondary mode. two-wire serial interfaced host has control over DDMI, SFP memories and chip registers. uC is set to an infinite wait loop. Note: This bit can only be modified by the two-wire serial interfaced host.	0b	R/W
1	2wire_mode	0b: Enable uC mode. uC has control of all memories. 1b: Enable two-wire serial mode. two-wire serial interfaced host has control over all memories. uC is disabled. Takes precedence over two-wire serial Secondary Mode Enable bit. Note: This bit can only be modified by the two-wire serial interfaced host.	0b	R/W
0	boot_mode_en	0b: Normal operation 1b: Initiate boot-up mode, read-back data from EEPROM and reset the uC. Note: This bit can only be modified by the two-wire serial interfaced host.	0b	R/W

Page: 03h
Address: 8A
Register Name: EEC_STAT_0
Default Value: 08h
Description: ECC Status Register 0

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved	0b	R
6:4	smm_state	EEC Internal State Machine 000b: Idle 001b: Read 011b: Write 100b: Done 1001b - 1111b: Reserved	000b	R
3	sda_output_en	Output enable for EEPROM interface data bus. 0b: sda is output 1b: sda is input	1b	R
2	timeout_error	Write operation to EEPROM timed out. (No ack received from EEPROM)	0b	R (SC)
1	page_chksum_error	Error indication for checksum failure during page write 0b: No Error 1b: Checksum for page write does not match	0b	R (SC)
0	RSVD	Reserved	0b	R

Page: 03h
Address: 8Bh
Register Name: EEC_STAT_1
Default Value: 00h
Description: ECC Status Register 1

Bit(s)	Name	Description	Default	Type
7:0	checksum	Checksum computed for current operation	0000 0000b	R

Page: 03h
Address: 8Ch
Register Name: EEC_STAT_2
Default Value: 00h
Description: ECC Status Register 2

Bit(s)	Name	Description	Default	Type
7:4	bit_count	Number of bits on the SDA for each SMI state	0000b	R
3:0	smi_state	2-wire interface to EEPROM state 0000: IDLE 0001: WR_START 0010: RW_ADDR1 0011: RW_ADDR2 0100: WR_DATA 0101: WR_STOP 0110: RD_START 0111: RD_DATA 1000: RD_STOP others: Reserved	0000b	R

Page: 03h
Address: 8Dh
Register Name: EEC_STAT_3
Default Value: 00h
Description: ECC Status Register 2

Bit(s)	Name	Description	Default	Type
7:3	byte_count	Number of bytes sent on SDA [4:0], only LSB 5 bits are output	0000 0b	R
2:0	smi_command	Command Sent to SMI (operation READ/WRITE eeprom) 000: NOP 101: Page Write to EEPROM 111: Page Read from EEPROM others: Reserved	000b	R

Page: 03h
Address: 8Eh
Register Name: GPIO_SAMPLE
Default Value: 00h
Description: **GPIO Input Sample Rate Control Register**

Bit(s)	Name	Description	Default	Type
7:0	gpio_in_smp_rate	Counter that determines how frequently the GPIO inputs are sampled. Period can be set from 0 to 255 clock cycles. Setting this register to 0 will cause the GPIO inputs to be sampled every clock cycle.	0000 0000b	R/W

Page: 03h
Address: 8Fh
Register Name: GPIO_MASK
Default Value: 00h
Description: GPIO Input IRQ Mask Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R/W
3	gpio3_irq_mask	0b: Mask interrupt to uC observed on GPIO 3 input. 1b: Do not mask interrupt observed on GPIO 3 input.	0b	R/W
2	gpio2_irq_mask	0b: Mask interrupt to uC observed on GPIO 2 input. 1b: Do not mask interrupt observed on GPIO 2 input.	0b	R/W
1	gpio1_irq_mask	0b: Mask interrupt to uC observed on GPIO 1 input. 1b: Do not mask interrupt observed on GPIO 1 input.	0b	R/W
0	gpio0_irq_mask	0b: Mask interrupt to uC observed on GPIO 0 input. 1b: Do not mask interrupt observed on GPIO 0 input.	0b	R/W

Page: 03h
Address: 90h
Register Name: GPIO_OUT
Default Value: 00h
Description: GPIO Output Force State Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R/W
5	gpio4_out_en	1b: Enable GPIO4 analog mode 0b: GPIO4 is digital input	0b	R/W
4	gpio4_out_val	No effect, because OEN of this GPIO is tied to logic 1	0b	R/W
3	gpio3_out_val	When GPIO3 is configured in output mode the state of this bit is forced on the GPIO3 pad.	0b	R/W
2	gpio2_out_val	When GPIO2 is configured in output mode the state of this bit is forced on the GPIO2 pad.	0b	R/W
1	gpio1_out_val	When GPIO1 is configured in output mode the state of this bit is forced on the GPIO1 pad.	0b	R/W
0	gpio0_out_val	When GPIO0 is configured in output mode the state of this bit is forced on the GPIO0 pad.	0b	R/W

Page: 03h
Address: 91h
Register Name: GPIO0_CTRL
Default Value: 08h
Description: GPIO 0 Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R/W
5:4	gpio0_intr_trig	The interrupt is triggered by one of the following events on GPIO 0 input. 00b: Level low 01b: Level high 10b: Falling edge 11b: Rising edge	00b	R/W
3:2	gpio0_mode	00b: Output only mode 01b: Reserved 10b: Input interrupt mode 11b: Enable GPIO 0 analog mode	10b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: 93h
Register Name: GPIO1_CTRL
Default Value: 08h
Description: GPIO 1 Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R/W
5:4	gpio1_intr_trig	The interrupt is triggered by one of the following events on GPIO 1 input. 00b: Level low 01b: Level high 10b: Falling edge 11b: Rising edge	00b	R/W
3:2	gpio1_mode	00b: Output only mode 01b: Reserved 10b: Input interrupt mode 11b: Enable GPIO 1 analog mode	10b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: 95h
Register Name: GPIO2_CTRL
Default Value: 08h
Description: GPIO 2 Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R/W
5:4	gpio2_intr_trig	The interrupt is triggered by one of the following events on GPIO 2 input. 00b: Level low 01b: Level high 10b: Falling edge 11b: Rising edge	00b	R/W
3:2	gpio2_mode	00b: Output only mode 01b: Reserved 10b: Input interrupt mode 11b: Enable GPIO 2 analog mode	10b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: 97h
Register Name: GPIO3_CTRL
Default Value: 08h
Description: GPIO 3 Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R/W
5:4	gpio3_intr_trig	The interrupt is triggered by one of the following events on GPIO 3 input. 00b: Level low 01b: Level high 10b: Falling edge 11b: Rising edge	00b	R/W
3:2	gpio3_mode	00b: Output only mode 01b: Reserved 10b: Input interrupt mode 11b: Enable GPIO 3 analog mode	10b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: 99h
Register Name: GPIO_IRQ
Default Value: 00h
Description: GPIO Interrupt Status Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5	2wire_sec_mode_status	0: Normal operational mode 1: Two-wire serial secondary mode is enabled. uC is in wait state, while two-wire serial interfaced host has access to DDMI, SFT and chip registers	0b	R
4	2wire_mode_status	0: Normal operational mode 1: Two-wire serial secondary mode is enabled. uC is disabled, while two-wire serial interfaced host has access to DDMI, SFT, PDRAM and chip registers.	0b	R
3	gpio3_irq	GPIO 3 IRQ status. (Clear on read.)	0b	R
2	gpio2_irq	GPIO 2 IRQ status. (Clear on read.)	0b	R
1	gpio1_irq	GPIO 1 IRQ status. (Clear on read.)	0b	R
0	gpio0_irq	GPIO 0 IRQ status. (Clear on read.)	0b	R

Page: 03h
Address: 9Bh
Register Name: UC_CTRL_1
Default Value: 00h
Description: Micro Controller Control Register 1

Bit(s)	Name	Description	Default	Type
7:3	RSVD	Reserved	0000 0b	R/W
2	uc_disable	0b: Enable internal MCU 1b: Disable internal MCU	0b	R/W
1	access_done	0b: EEPROM is being accessed 1b: EEPROM access is complete	0b	R
0	dload_done	0b: Boot-up EEPROM download in progress or PDRAM read-back/write-back in progress 1b: EEPROM download complete and MCU begins operation	0b	R

Page: 03h
Address: 9Ch
Register Name: GPIO_IN
Default Value: 00h
Description: GPIO Input Register

Bit(s)	Name	Description	Default	Type
7	gpio3_in	0b: Low input state on GPIO 1b: High input state on GPIO	0b	R
6	gpio2_in	0b: Low input state on GPIO 1b: High input state on GPIO	0b	R
5	gpio1_in	0b: Low input state on GPIO 1b: High input state on GPIO	0b	R
4	gpio0_in	0b: Low input state on GPIO 1b: High input state on GPIO	0b	R
3	gpio4_in	0b: Low input state on GPIO 1b: High input state on GPIO	0b	R
2:0	RSVD	Reserved	000b	R

Page: 03h
Address: B5h
Register Name: PHY_ADDR
Default Value: 00h
Description: Physical Address Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:0	phy_addr	Two-wire serial physical address bits [5:1]. Bit [0] is hard coded to 0 for SFP address space and 1 for DDMI, Table 3/4 registers, PDRAM, and USER/VENDOR address spaces.	00 0000b	R/W

Page: 03h
Address: B7h
Register Name: RX_CTRL
Default Value: 00h
Description: RX Control Register

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R
0	rx_los	RX_LOS pins status bit.	0b	R

Page: 03h
Address: B8h
Register Name: LASER_CTRL0
Default Value: 00h
Description: Laser Control Register 0

Bit(s)	Name	Description	Default	Type
7	soft_scb	When high, laser driver TX_FAULT output will go high if a fault state occurs, but laser driver does not automatically disable.	0b	R/W
6	sb_in	Sidebar Input. When high modulation current is increased by approximately 4%. When low modulation current is at the level set by MOD_{SET}.	0b	R/W
5	soft_cc_sel	Selects common-cathode mode. Serves same function as CCSEL pin; Reserve for possible use if CCSEL pin is not brought out of package.	0b	R/W
4	dis_mod_rst	0: enable the forced POR function 1: disable the forced POR function In case the PWR_RST input is used only for power-down function	0b	R/W
3	pd_polarity_swap	Selects the polarity of the photodiode. 0b: Photodiode anode sources current into IPIN for common anode laser configurations and sinks current from IPIN for common cathode laser configurations 1b: Photodiode cathode sinks current from IPIN for common anode laser configurations and sources current into IPIN for common cathode laser configurations	0b	R/W
2	RSVD	Reserved	0b	R/W
1	offset_en	0b: Disable offset adjustment using 6 bit-1 DAC 1b: Enable offset adjustment using 6 bit-1 DAC	0b	R/W
0	pwa_en	0b: Disable pulse-width adjustment using 6 bit-2 DAC 1b: Enable pulse-width adjustment using 6 bit-2 DAC	0b	R/W

Page: 03h
Address: B9h
Register Name: LASER_CTRL1
Default Value: 40h
Description: Laser Driver Control Register 1

Bit(s)	Name	Description	Default	Type
7	datadetect_en	0b: Disable data detection 1b: Enable data detection	0b	R/W
6	polarity_swap	0b: When DINP > DINN, OUTN sinks current When DINN > DINP, OUTP sinks current 1b: Reverses the above relationship	1b	R/W
5	ignore_ipin	0b: Normal operation 1b: Ignore IPIN fault status	0b	R/W
4	bias_comp	Bias output compensation is optimized depending on whether a ferrite is or is not used at IBOUT and/or SVCC. 0b: Ferrite is used 1b: Ferrite is not used	0b	R/W

Bit(s)	Name	Description	Default	Type
3	reset_fail	Toggling this bit high and then low will reset the TX_FAULT output latch of the crude faults CF/VCCOK/softDIS (only applies when soft_scb = 1)	0b	R/W
2	latch_overdrive	When high, bypasses Latching of TX_FAULT; applies only when soft_scb = 1b.	0b	R/W
1	hold_monitors	0b: Monitors turn off upon laser driver disable. 1b: Holds the last monitor values when the laser driver is disabled while this bit is high.	0b	R/W
0	soft_fail	0b: TX_FAULT is asserted when safety logic detects a fault condition 1b: Force TX_FAULT output to high	0b	R/W

Page: 03h
Address: BBh
Register Name: LASER_STAT0
Default Value: 00h
Description: Laser Driver Status Register 0

Bit(s)	Name	Description	Default	Type
7	cf_ibout	0b: Normal operation 1b: indicates a crude Fault on IboutCA/CC	0b	R
6	ssb_status	Status of SSB pad	0b	R
5	state_of_dis_pin	Shows state of TX_DIS pin (high = disabled) (used for Reprogramming Serial Device Address) When high, the bias and modulation outputs are off.	0b	R
4	RSVD	Reserved	0b	R
3	status_spi_sel	State of SPI_Sel pad	0b	R
2	status_ccsel	State of (CCSEL pad OR soft_CCsel) Signals the digital block whether output is configured for common cathode or common anode mode.	0b	R
1	status_fail	This signals the status of the FAIL output pad (high = fault state)	0b	R
0	laser_status	“OR”ing of anything that can shut-off Laser output (DISpin/softDis/ Safetyfault)	0b	R

Page: 03h
Address: BCh
Register Name: LASER_STAT1
Default Value: 00h
Description: Laser Driver Status Register 1

Bit(s)	Name	Description	Default	Type
7	status_pwdn_rst	State of Pwdn_Rst pad	0b	R
6	vcc3_status	1: Indicates VCC3 is too high or too low	0b	R
5	data_detect	A high at this bit indicates data detected at the inputs of the laser driver.	0b	R
4	ipin_low	A high at this bit indicates that the Ipin voltage is too low (within 100mV of GND).	0b	R
3	ipin_high	A high at this bit indicates that the Ipin voltage is too high (within 100mV of Vcc3).	0b	R

Bit(s)	Name	Description	Default	Type
2	biasr_status	Indicates a Fault on Bias R	0b	R
1	dvdd_status	Indicates a Fault on AV_{DD}/DV_{DD}	0b	R
0	outp_status	Indicates a Fault on OUTP pin	0b	R

Page: 03h
Address: BDh
Register Name: MOD_CTRL
Default Value: 02h
Description: Modulation Control Register

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved	0b	R/W
6	mcu_temp_comp	Microprocessor temperature compensation enable	0b	R/W
5	bm_copy	Disable BIAS_MON copy to BIAS_MON_CAL	0b	R/W
4	temp_sel	Temperature monitor select 0: internal temp monitor 1: external temp monitor	0b	R/W
3:2	RSVD	Reserved	00b	R/W
1	mod_temp_comp	Enable modulation current temperature compensation	1b	R/W
0	bias_temp_comp	Enable modulation current bias compensation	0b	R/W

Page: 03h
Address: BEh
Register Name: MOD_SET_0
Default Value: 00h
Description: Modulation Current Generator Register 0

Bit(s)	Name	Description	Default	Type
7:0	modulation_target[7:0]	Modulation open loop target LSB	00h	R/W

Page: 03h
Address: BFh
Register Name: MOD_SET_1
Default Value: 00h
Description: Modulation Current Generator Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	modulation_target[11:8]	Modulation open loop target MSB	0000b	R/W

Page: 03h
Address: C0h
Register Name: MOD_CLIP_0
Default Value: 00h
Description: Modulation Clip Register 0

Bit(s)	Name	Description	Default	Type
7:1	mod_max[7:0]	Modulation max DAC current value LSB	00h	R/W

Page: 03h
Address: C1h
Register Name: MOD_CLIP_1
Default Value: 00h
Description: Modulation Clip Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	mod_max[11:8]	Modulation max DAC current value MSB	0000b	R/W

Page: 03h
Address: C2h
Register Name: MOD_ CUR_MON_0
Default Value: 00h
Description: Modulation Current Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	mod_mon[7:0]	Mod ADC value LSB	00h	R

Page: 03h
Address: C3h
Register Name: MOD_ CUR_MON_1
Default Value: 00h
Description: Modulation Current Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	mod_mon[11:8]	Mod ADC value MSB. Latched when register MOD_MON_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: C4h
Register Name: MOD_CUR_CTRL
Default Value: 08h
Description: Modulation Current Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	mod_adc_cal	0: MOD ADC calibration is disabled 1: MOD ADC calibration is enabled	1b	R/W
2	mod_adc_pd	0: MOD ADC is in normal operation 1: MOD ADC is powered down	0b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: C5h
Register Name: BIAS_CTRL
Default Value: 00h
Description: Bias Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R/W
3	tpm_copy	Disable TX_PWR_MON copy to TX_PWR_MON_CAL.	0b	R/W
2	apc_cntrl	0b: Open loop 1b: Enable APC closed loop mode	0b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: C6h
Register Name: BIAS_ CUR_MON_0
Default Value: 00h
Description: Bias Current Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	bias_mon[7:0]	Bias current value LSB	00h	R

Page: 03h
Address: C7h
Register Name: BIAS_ CUR_MON_1
Default Value: 00h
Description: Bias Current Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	bias_mon[11:8]	Bias ADC value MSB. Latched when register BIAS_MON_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: C8h
Register Name: BIAS_CUR_CAL_0
Default Value: 00h
Description: Bias Current Calibration Register 0

Bit(s)	Name	Description	Default	Type
7:0	bias_mon_cal[7:0]	Bias Current (Bias comp) closed loop target LSB.	00h	R/W

Page: 03h
Address: C9h
Register Name: BIAS_CUR_CAL_1
Default Value: 00h
Description: Bias Current Calibration Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R/W
3:0	bias_mon_cal[11:8]	Bias Current (Bias comp) closed loop target MSB. Latched when register BIAS_CUR_CAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R/W

Page: 03h
Address: CAh
Register Name: BIAS_CUR_CTRL
Default Value: 08h
Description: Bias Current Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R

Bit(s)	Name	Description	Default	Type
3	bias_adc_cal	0: BIAS ADC calibration is disabled 1: BIAS ADC calibration is enabled	1b	R/W
2	bias_adc_pd	0: BIAS ADC is in normal operation 1: BIAS ADC is powered down	0b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: CBh
Register Name: SUPPLY_MON_0
Default Value: 00h
Description: Supply Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	supply_mon[7:0]	Supply ADC value LSB	00h	R

Page: 03h
Address: CCh
Register Name: SUPPLY_MON_1
Default Value: 00h
Description: Supply Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	supply_mon[11:8]	Supply ADC value MSB. Latched when register SUPPLY_MON_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: CDh
Register Name: SUPPLY_CTRL
Default Value: 09h
Description: Supply Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	supply_adc_cal	0: Supply ADC calibration is disabled 1: Supply ADC calibration is enabled	1b	R/W
2	supply_adc_pd	0: Supply ADC is in normal operation 1: Supply ADC is powered down	0b	R/W
1:0	cal_adj[1:0]	00: 5uA 01: 10uA 10: 15uA 11: 20uA	01b	R/W

Page: 03h
Address: CEh
Register Name: AUX1_MON_0
Default Value: 00h
Description: A/D AUX1 Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	aux1_val[7:0]	Aux1 value LSB (from A/Daux1)	00h	R

Page: 03h
Address: CFh
Register Name: AUX1_MON_1
Default Value: 00h
Description: A/D AUX1 Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	aux1_val[11:8]	Aux1 value MSB (from A/DAUX1). Latched when register AUX1_VAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: D0h
Register Name: AUX1_CTRL
Default Value: 08h
Description: AUX1 Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	aux1_adc_cal	0: AUX1 ADC calibration is disabled 1: AUX1 ADC calibration is enabled	1b	R/W
2	aux1_adc_pd	0: AUX1 ADC is in normal operation 1: AUX1 ADC is powered down	0b	R/W
1	aux1_adc_dir	0: Current is sinking to AUX1 ADC 1: Current is sourcing from AUX1 ADC	0b	R/W
0	aux1_adc_sel	0: Input to the AUX1 ADC is a current 1: Input to the AUX1 ADC is a voltage	0b	R/W

Page: 03h
Address: D1h
Register Name: RX_PWR_MON_0
Default Value: 00h
Description: RX Power Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	rx_pwr_mon[7:0]	Receive power value LSB	00h	R

Page: 03h
Address: D2h
Register Name: RX_PWR_MON_1
Default Value: 00h
Description: RX Power Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	rx_pwr_mon[11:8]	Receive power value MSB. Latched when register RX_PWR_MON_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: D3h
Register Name: RX_PWR_CTRL
Default Value: 08h
Description: RX Power Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	rx_pwr_adc_cal	0: RX Power ADC calibration is disabled 1: RX Power ADC calibration is enabled	1b	R/W
2	rx_pwr_adc_pd	0: RX Power ADC is in normal operation 1: RX Power ADC is powered down	0b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: D4h
Register Name: TX_PWR_MON_0
Default Value: 00h
Description: TX Power Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	tx_pwr_mon	TX power value LSB [7:0]	00h	R

Page: 03h
Address: D5h
Register Name: TX_PWR_MON_1
Default Value: 00h
Description: TX Power Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	tx_pwr_mon	TX power value MSB [11:8]. Latched when register TX_PWR_MON_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: D6h
Register Name: TX_PWR_CAL_0
Default Value: 00h
Description: TX Power Calibration Register 0

Bit(s)	Name	Description	Default	Type
7:0	tx_pwr_cal	TX power current closed loop target LSB [7:0]	00h	R/W

Page: 03h
Address: D7h
Register Name: TX_PWR_CAL_1
Default Value: 00h
Description: TX Power Calibration Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	tx_pwr_cal	TX power current closed loop target MSB [11:8]. Latched when register TX_PWR_CAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R/W

Page: 03h
Address: D8h
Register Name: TX_PWR_CTRL
Default Value: 08h
Description: TX Power Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R

Bit(s)	Name	Description	Default	Type
3	tx_pwr_adc_cal	0: TX Power ADC calibration is disabled 1: TX Power ADC calibration is enabled	1b	R/W
2	tx_pwr_adc_pd	0: TX Power ADC is in normal operation 1: TX Power ADC is powered down	0b	R/W
1:0	RSVD	Reserved	00b	R/W

Page: 03h
Address: DCh
Register Name: AUX2_VAL_0
Default Value: 00h
Description: AUX2 Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	aux2_val[7:0]	AUX2 monitor LSB (External Temp ADC)	00h	R

Page: 03h
Address: DDh
Register Name: AUX2_VAL_1
Default Value: 00h
Description: AUX2 Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	aux2_val[11:8]	AUX2 monitor MSB (from A/D aux2). Latched when register AUX2_VAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: DEh
Register Name: AUX2_CTRL
Default Value: 09h
Description: AUX2 Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	aux2_adc_cal	0: AUX2 ADC calibration is disabled 1: AUX2 ADC calibration is enabled	1b	R/W
2	aux2_adc_pd	0: AUX2 ADC is in normal operation 1: AUX2 ADC is powered down	0b	R/W
1	aux2_adc_dir	0: Current is sinking to AUX2 ADC 1: Current is sourcing from AUX2 ADC	0b	R/W
0	aux2_adc_sel	0: Input to the AUX2 ADC is a current 1: Input to the AUX2 ADC is a voltage	1b	R/W

Page: 03h
Address: DFh
Register Name: TEMP_MON_0
Default Value: 00h
Description: Internal Temperature Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	temp_mon[7:0]	Internal Temperature ADC value LSB	00h	R

Page: 03h
Address: E0h
Register Name: TEMP_MON_1
Default Value: 00h
Description: Internal Temperature Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	temp_mon[11:8]	Internal Temperature ADC value MSB. Latched when register TEMP_MON_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 03h
Address: E1h
Register Name: TEMP_MON_CTRL
Default Value: 09h
Description: TX Power Control Register

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	temp_mon_cal	0: Internal Temperature ADC calibration is disabled 1: Internal Temperature ADC calibration is enabled	1b	R/W
2	temp_mon_pd	0: Internal Temperature ADC is in normal operation 1: Internal Temperature ADC is powered down	0b	R/W
1:0	RSVD	Reserved	01b	R/W

Page: 03h
Address: E2h
Register Name: TEMP_START_0
Default Value: 00h
Description: Temperature Start Register 0

Bit(s)	Name	Description	Default	Type
7:0	temp_start[7:0]	Temp Start Register LSB	00h	R/W

Page: 03h
Address: E3h
Register Name: TEMP_START_1
Default Value: 00h
Description: Temperature Start Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	temp_start[11:8]	Temp Start Register MSB.	0000b	R/W

Page: 03h
Address: E4h
Register Name: TEMP_COEF
Default Value: 00h
Description: Temperature Coefficient Register 1

Bit(s)	Name	Description	Default	Type
7:5	RSVD	Reserved	000b	R
4:0	temp_coef[4:0]	Temp coefficient 5bits	0 0000b	R/W

Page: 03h
Address: E7h
Register Name: APC_SET_0
Default Value: 00h
Description: APC Set Control Register 0

Bit(s)	Name	Description	Default	Type
7:0	apc_set	APC set control LSB [7:0]	00h	R/W

Page: 03h
Address: E8h
Register Name: APC_SET_1
Default Value: 00h
Description: APC Set Control Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	apc_set	APC set control MSB [11:8].	0000b	R/W

Page: 03h
Address: E9h
Register Name: APC_CLIP_0
Default Value: 00h
Description: APC Clip Control Register 0

Bit(s)	Name	Description	Default	Type
7:0	apc_clip[7:0]	APC clip control LSB	00h	R/W

Page: 03h
Address: EAh
Register Name: APC_CLIP_1
Default Value: 00h
Description: APC Clip Control Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	apc_clip[11:8]	APC clip control MSB.	0000b	R/W

Page: 03h
Address: EBh
Register Name: GAIN_CTRL
Default Value: 00h
Description: Gain Control Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:2	ba_gain_ctrl	Modulation current (Bias comp) close loop gain. Values set the gain from a right shift of 0 (0000b) to right shift of 7 (0111b) or left shift of 1 (1111b) to left shift of 8 (1000b)	00 00b	R/W
1:0	apc_gain_ctrl	APC close loop gain.	00b	R/W

Page: 03h
Address: ECh
Register Name: APC_FDB_MON_0
Default Value: 00h
Description: APC Feedback Monitor Register 0

Bit(s)	Name	Description	Default	Type
7:0	apc_fdb_mon[7:0]	APC closed loop integrator register 0	00h	R

Page: 03h
Address: EDh
Register Name: APC_FDB_MON_1
Default Value: 00h
Description: APC Feedback Monitor Register 1

Bit(s)	Name	Description	Default	Type
7:0	apc_fdb_mon[15:8]	APC closed loop integrator register 1	00h	R

Page: 03h
Address: EEh
Register Name: APC_FDB_MON_2
Default Value: 00h
Description: APC Feedback Monitor Register 2

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:0	apc_fdb_mon[21:16]	APC closed loop integrator register 2	00 0000b	R

Page: 03h
Address: EFh
Register Name: BIAS_DAC_CODE_0
Default Value: 00h
Description: Bias DAC Code Register 0

Bit(s)	Name	Description	Default	Type
7:0	bias_dac[7:0]	APC generated bias code, LSB	00h	R

Page: 03h
Address: F0h
Register Name: BIAS_DAC_CODE_1
Default Value: 00h
Description: Bias DAC Code Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	bias_dac[11:8]	APC generated bias code, MSB	0000b	R

Page: 03h
Address: F1h
Register Name: BIAS_DAC_CTRL
Default Value: 00h
Description: Bias DAC Control Register

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	0000 00b	R
1	bias_dac_hp	0: DAC is in low power mode 1: DAC is in high power mode	0b	R/W
0	bias_dac_pd	0: DAC is in normal operation 1: DAC is powered down	0b	R/W

Page: 03h
Address: F2h
Register Name: MOD_DAC_CODE_0
Default Value: 00h
Description: Modulation DAC Code Register 0

Bit(s)	Name	Description	Default	Type
7:0	mod_dac[7:0]	APC generated modulation code, LSB	00h	R

Page: 03h
Address: F3h
Register Name: MOD_DAC_CODE_1
Default Value: 00h
Description: Modulation DAC Code Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	mod_dac[11:8]	APC generated modulation code, MSB	0000b	R

Page: 03h
Address: F4h
Register Name: MOD_DAC_CTRL
Default Value: 00h
Description: Modulation DAC Control Register

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	0000 00b	R
1	mod_dac_hp	0: DAC is in low power mode 1: DAC is in high power mode	0b	R/W
0	mod_dac_pd	0: DAC is in normal operation 1: DAC is powered down	0b	R/W

Page: 03h
Address: F5h
Register Name: PULSEW_DAC_CODE
Default Value: 00h
Description: Pulse Width DAC Code Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:0	pwa_dac[5:0]	Pulse width DAC code	00 0000b	R/W

Page: 03h
Address: F6h
Register Name: PULSEW_DAC_CTRL
Default Value: 00h
Description: Pulse Width DAC Control Register

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	0000 00b	R
1	pulsew_dac_hp	0: DAC is in low power mode 1: DAC is in high power mode	0b	R/W
0	pulsew_dac_pd	0: DAC is in normal operation 1: DAC is powered down	0b	R/W

Page: 03h
Address: F7h
Register Name: 6BIT_DAC2
Default Value: 00h
Description: 6 Bit DAC2 Code Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:0	6bit_dac2[5:0]	6 bit DAC2 code. Controls the 6 bit DAC at GPIO4	00 0000b	R/W

Page: 03h
Address: F8h
Register Name: 6BIT_DAC2_CTRL
Default Value: 00h
Description: 6 Bit DAC2 Control Register

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	0000 00b	R
1	6bit_dac2_hp	0: DAC2 is in low power mode 1: DAC2 is in high power mode	0b	R/W
0	6bit_dac2_pd	0: DAC2 is in normal operation 1: DAC2 is powered down	0b	R/W

Page: 03h
Address: F9h
Register Name: 6BIT_DAC1
Default Value: 00h
Description: 6 Bit DAC1 Code Register

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:0	6bit_dac1[5:0]	6 bit DAC1 code. Controls the 6 bit DAC at GPIO1	00 0000b	R/W

Page: 03h
Address: FAh
Register Name: 6BIT_DAC1_CTRL
Default Value: 00h
Description: 6 Bit DAC1 Control Register

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	0000 00b	R
1	6bit_dac1_hp	0: DAC1 is in low power mode 1: DAC1 is in high power mode	0b	R/W
0	6bit_dac1_pd	0: DAC1 is in normal operation 1: DAC1 is powered down	0b	R/W

Page: 03h
Address: FBh
Register Name: 10B_DAC_CODE_0
Default Value: 00h
Description: 10 Bit DAC Code Register 0

Bit(s)	Name	Description	Default	Type
7:0	10bit_dac[7:0]	10 bit DAC code LSB	00h	R/W

Page: 03h
Address: FCh
Register Name: 10B_DAC_CODE_1
Default Value: 00h
Description: 10 Bit DAC Code Register 1

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	0000 00b	R
1:0	10bit_dac[9:8]	10 bit DAC code MSB	00b	R/W

Page: 03h
Address: FDh
Register Name: 10B_DAC_CTRL
Default Value: 00h
Description: 10 Bit DAC Control Register

Bit(s)	Name	Description	Default	Type
7:3	RSVD	Reserved	0000 0b	R
2	output_mode	0: DAC is in current mode 1: DAC is in voltage mode	0b	R/W
1	10bit_dac_hp	0: DAC is in low power mode 1: DAC is in high power mode	0b	R/W
0	10bit_dac_pd	0: DAC is in normal operation 1: DAC is powered down	0b	R/W

6.3 Table Select 04h Register Details

Page: 04h
Address: 80h
Register Name: PWD0_0
Default Value: 00h
Description: Password Level 0 Register 0

Bit(s)	Name	Description	Default	Type
7:0	pwd_level0[7:0]	Byte 1 of 4 byte Level 0 password	00h	R/W

Page: 04h
Address: 81h
Register Name: PWD0_1
Default Value: 00h
Description: Password Level 0 Register 1

Bit(s)	Name	Description	Default	Type
7:0	pwd_level0[15:8]	Byte 2 of 4 byte Level 0 password	00h	R/W

Page: 04h
Address: 82h
Register Name: PWD0_2
Default Value: 00h
Description: Password Level 0 Register 2

Bit(s)	Name	Description	Default	Type
7:0	pwd_level0[23:16]	Byte 3 of 4 byte Level 0 password	00h	R/W

Page: 04h
Address: 83h
Register Name: PWD0_3
Default Value: 00h
Description: Password Level 0 Register 3

Bit(s)	Name	Description	Default	Type
7:0	pwd_level0[31:24]	Byte 4 of 4 byte Level 0 password	00h	R/W

Page: 04h
Address: 84h
Register Name: PWD1_0
Default Value: 00h
Description: Password Level 1 Register 0

Bit(s)	Name	Description	Default	Type
7:0	pwd_level1[7:0]	Byte 1 of 4 byte Level 1 password	00h	R/W

Page: 04h
Address: 85h
Register Name: PWD1_1
Default Value: 00h
Description: Password Level 1 Register 1

Bit(s)	Name	Description	Default	Type
7:0	pwd_level1[15:8]	Byte 2 of 4 byte Level 1 password	00h	R/W

Page: 04h
Address: 86h
Register Name: PWD1_2
Default Value: 00h
Description: Password Level 1 Register 2

Bit(s)	Name	Description	Default	Type
7:0	pwd_level1[23:16]	Byte 3 of 4 byte Level 1 password	00h	R/W

Page: 04h
Address: 87h
Register Name: PWD1_3
Default Value: 00h
Description: Password Level 1 Register 3

Bit(s)	Name	Description	Default	Type
7:0	pwd_level1[31:24]	Byte 4 of 4 byte Level 1 password	00h	R/W

Page: 04h
Address: 88h
Register Name: PWD2_0
Default Value: 00h
Description: Password Level 2 Register 0

Bit(s)	Name	Description	Default	Type
7:0	pwd_level2[7:0]	Byte 1 of 4 byte Level 2 password	00h	R/W

Page: 04h
Address: 89h
Register Name: PWD2_1
Default Value: 00h
Description: Password Level 2 Register 1

Bit(s)	Name	Description	Default	Type
7:0	pwd_level2[15:8]	Byte 2 of 4 byte Level 2 password	00h	R/W

Page: 04h
Address: 8Ah
Register Name: PWD2_2
Default Value: 00h
Description: Password Level 2 Register 2

Bit(s)	Name	Description	Default	Type
7:0	pwd_level2[23:16]	Byte 3 of 4 byte Level 2 password	00h	R/W

Page: 04h
Address: 8Bh
Register Name: PWD2_3
Default Value: 00h
Description: Password Level 2 Register 3

Bit(s)	Name	Description	Default	Type
7:0	pwd_level2[31:24]	Byte 4 of 4 byte Level 2 password	00h	R/W

Page: 04h
Address: 90h
Register Name: RD_ACCESS0_0
Default Value: 00h
Description: Read Access Level 0 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw0_r	0: Table 03h registers read access not allowed for Level 0 user 1: Table 03h registers read access allowed for Level 0 users	0b	R/W
6	pgrm_pw0_r	0: Program/Data registers read access not allowed for Level 0 users 1: Program/Data registers read access allowed for Level 0 users	0b	R/W
5	sfp_rsvd_pw0_r	0: Reserved registers read access not allowed for Level 0 users 1: Reserved registers read access allowed for Level 0 users	0b	R/W
4	vnd_spcfc_pw0_r	0: Vendor registers read access not allowed for Level 0 users 1: Vendor registers read access allowed for Level 0 users	0b	R/W
3	usr_wrt_pw0_r	0: User registers read access not allowed for Level 0 users 1: User registers read access allowed for Level 0 users	0b	R/W
2	ser_id_pw0_r	0: Serial ID registers read access not allowed for Level 0 users 1: Serial ID registers read access allowed for Level 0 users	0b	R/W
1	diag2_pw0_r	0: Diagnostics 2 registers read access not allowed for Level 0 users 1: Diagnostics 2 registers read access allowed for Level 0 users	0b	R/W
0	diag1_pw0_r	0: Diagnostics 1 registers read access not allowed for Level 0 users 1: Diagnostics 1 registers read access allowed for Level 0 users	0b	R/W

Page: 04h
Address: 91h
Register Name: RD_ACCESS0_1
Default Value: 00h
Description: Read Access Level 0 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw0_r	0: Table 04h registers read access not allowed for Level 0 users 1: Table 04h registers read access allowed for Level 0 users	0b	R/W

Page: 04h
Address: 92h
Register Name: RD_ACCESS1_0
Default Value: 00h
Description: Read Access Level 1 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw1_r	0: Table 03h registers read access not allowed for Level 1 user 1: Table 03h registers read access allowed for Level 1 users	0b	R/W
6	pgrm_pw1_r	0: Program/Data registers read access not allowed for Level 1 users 1: Program/Data registers read access allowed for Level 1 users	0b	R/W
5	sfp_rsvd_pw1_r	0: Reserved registers read access not allowed for Level 1 users 1: Reserved registers read access allowed for Level 1 users	0b	R/W
4	vnd_spcfc_pw1_r	0: Vendor registers read access not allowed for Level 1 users 1: Vendor registers read access allowed for Level 1 users	0b	R/W
3	usr_wrt_pw1_r	0: User registers read access not allowed for Level 1 users 1: User registers read access allowed for Level 1 users	0b	R/W
2	ser_id_pw1_r	0: Serial ID registers read access not allowed for Level 1 users 1: Serial ID registers read access allowed for Level 1 users	0b	R/W
1	diag2_pw1_r	0: Diagnostics 2 registers read access not allowed for Level 1 users 1: Diagnostics 2 registers read access allowed for Level 1 users	0b	R/W
0	diag1_pw1_r	0: Diagnostics 1 registers read access not allowed for Level 1 users 1: Diagnostics 1 registers read access allowed for Level 1 users	0b	R/W

Page: 04h
Address: 93h
Register Name: RD_ACCESS1_1
Default Value: 00h
Description: Read Access Level 1 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw1_r	0: Table 04h registers read access not allowed for Level 1 users 1: Table 04h registers read access allowed for Level 1 users	0b	R/W

Page: 04h
Address: 94h
Register Name: RD_ACCESS2_0
Default Value: 00h
Description: Read Access Level 2 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw2_r	0: Table 03h registers read access not allowed for Level 2 user 1: Table 03h registers read access allowed for Level 2 users	0b	R/W
6	pgrm_pw2_r	0: Program/Data registers read access not allowed for Level 2 users 1: Program/Data registers read access allowed for Level 2 users	0b	R/W
5	sfp_rsvd_pw2_r	0: Reserved registers read access not allowed for Level 2 users 1: Reserved registers read access allowed for Level 2 users	0b	R/W
4	vnd_spcfc_pw2_r	0: Vendor registers read access not allowed for Level 2 users 1: Vendor registers read access allowed for Level 2 users	0b	R/W
3	usr_wrt_pw2_r	0: User registers read access not allowed for Level 2 users 1: User registers read access allowed for Level 2 users	0b	R/W
2	ser_id_pw2_r	0: Serial ID registers read access not allowed for Level 2 users 1: Serial ID registers read access allowed for Level 2 users	0b	R/W
1	diag2_pw2_r	0: Diagnostics 2 registers read access not allowed for Level 2 users 1: Diagnostics 2 registers read access allowed for Level 2 users	0b	R/W
0	diag1_pw2_r	0: Diagnostics 1 registers read access not allowed for Level 2 users 1: Diagnostics 1 registers read access allowed for Level 2 users	0b	R/W

Page: 04h
Address: 95h
Register Name: RD_ACCESS2_1
Default Value: 00h
Description: Read Access Level 2 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw2_r	0: Table 04h registers read access not allowed for Level 2 users 1: Table 04h registers read access allowed for Level 2 users	0b	R/W

Page: 04h
Address: 96h
Register Name: RD_ACCESS3_0
Default Value: 00h
Description: Read Access Level 3 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw3_r	0: Table 03h registers read access not allowed for Level 3 user 1: Table 03h registers read access allowed for Level 3 users	0b	R/W
6	pgrm_pw3_r	0: Program/Data registers read access not allowed for Level 3 users 1: Program/Data registers read access allowed for Level 3 users	0b	R/W
5	sfp_rsvd_pw3_r	0: Reserved registers read access not allowed for Level 3 users 1: Reserved registers read access allowed for Level 3 users	0b	R/W
4	vnd_spcfc_pw3_r	0: Vendor registers read access not allowed for Level 3 users 1: Vendor registers read access allowed for Level 3 users	0b	R/W
3	usr_wrt_pw3_r	0: User registers read access not allowed for Level 3 users 1: User registers read access allowed for Level 3 users	0b	R/W
2	ser_id_pw3_r	0: Serial ID registers read access not allowed for Level 3 users 1: Serial ID registers read access allowed for Level 3 users	0b	R/W
1	diag2_pw3_r	0: Diagnostics 2 registers read access not allowed for Level 3 users 1: Diagnostics 2 registers read access allowed for Level 3 users	0b	R/W
0	diag1_pw3_r	0: Diagnostics 1 registers read access not allowed for Level 3 users 1: Diagnostics 1 registers read access allowed for Level 3 users	0b	R/W

Page: 04h
Address: 97h
Register Name: RD_ACCESS3_1
Default Value: 00h
Description: Read Access Level 3 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw3_r	0: Table 04h registers read access not allowed for Level 3 users 1: Table 04h registers read access allowed for Level 3 users	0b	R/W

Page: 04h
Address: 98h
Register Name: WR_ACCESS0_0
Default Value: 00h
Description: Write Access Level 0 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw0_w	0: Table 03h registers write access not allowed for Level 0 user 1: Table 03h registers write access allowed for Level 0 users	0b	R/W
6	pgrm_pw0_w	0: Program/Data registers write access not allowed for Level 0 users 1: Program/Data registers write access allowed for Level 0 users	0b	R/W
5	sfp_rsvd_pw0_w	0: Reserved registers write access not allowed for Level 0 users 1: Reserved registers write access allowed for Level 0 users	0b	R/W
4	vnd_spcfc_pw0_w	0: Vendor registers write access not allowed for Level 0 users 1: Vendor registers write access allowed for Level 0 users	0b	R/W
3	usr_wrt_pw0_w	0: User registers write access not allowed for Level 0 users 1: User registers write access allowed for Level 0 users	0b	R/W
2	ser_id_pw0_w	0: Serial ID registers write access not allowed for Level 0 users 1: Serial ID registers write access allowed for Level 0 users	0b	R/W
1	diag2_pw0_w	0: Diagnostics 2 registers write access not allowed for Level 0 users 1: Diagnostics 2 registers write access allowed for Level 0 users	0b	R/W
0	diag1_pw0_w	0: Diagnostics 1 registers write access not allowed for Level 0 users 1: Diagnostics 1 registers write access allowed for Level 0 users	0b	R/W

Page: 04h
Address: 99h
Register Name: WR_ACCESS0_1
Default Value: 00h
Description: Write Access Level 0 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw0_w	0: Table 04h registers write access not allowed for Level 0 users 1: Table 04h registers write access allowed for Level 0 users	0b	R/W

Page: 04h
Address: 9Ah
Register Name: WR_ACCESS1_0
Default Value: 00h
Description: Write Access Level 1 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw1_w	0: Table 03h registers write access not allowed for Level 1 user 1: Table 03h registers write access allowed for Level 1 users	0b	R/W
6	pgrm_pw1_w	0: Program/Data registers write access not allowed for Level 1 users 1: Program/Data registers write access allowed for Level 1 users	0b	R/W
5	sfp_rsvd_pw1_w	0: Reserved registers write access not allowed for Level 1 users 1: Reserved registers write access allowed for Level 1 users	0b	R/W
4	vnd_spcfc_pw1_w	0: Vendor registers write access not allowed for Level 1 users 1: Vendor registers write access allowed for Level 1 users	0b	R/W
3	usr_wrt_pw1_w	0: User registers write access not allowed for Level 1 users 1: User registers write access allowed for Level 1 users	0b	R/W
2	ser_id_pw1_w	0: Serial ID registers write access not allowed for Level 1 users 1: Serial ID registers write access allowed for Level 1 users	0b	R/W
1	diag2_pw1_w	0: Diagnostics 2 registers write access not allowed for Level 1 users 1: Diagnostics 2 registers write access allowed for Level 1 users	0b	R/W
0	diag1_pw1_w	0: Diagnostics 1 registers write access not allowed for Level 1 users 1: Diagnostics 1 registers write access allowed for Level 1 users	0b	R/W

Page: 04h
Address: 9Bh
Register Name: WR_ACCESS1_1
Default Value: 00h
Description: Write Access Level 1 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw1_w	0: Table 04h registers write access not allowed for Level 1 users 1: Table 04h registers write access allowed for Level 1 users	0b	R/W

Page: 04h
Address: 9Ch
Register Name: WR_ACCESS2_0
Default Value: 00h
Description: Write Access Level 2 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw2_w	0: Table 03h registers write access not allowed for Level 2 user 1: Table 03h registers write access allowed for Level 2 users	0b	R/W
6	pgrm_pw2_w	0: Program/Data registers write access not allowed for Level 2 users 1: Program/Data registers write access allowed for Level 2 users	0b	R/W
5	sfp_rsvd_pw2_w	0: Reserved registers write access not allowed for Level 2 users 1: Reserved registers write access allowed for Level 2 users	0b	R/W
4	vnd_spcfc_pw2_w	0: Vendor registers write access not allowed for Level 2 users 1: Vendor registers write access allowed for Level 2 users	0b	R/W
3	usr_wrt_pw2_w	0: User registers write access not allowed for Level 2 users 1: User registers write access allowed for Level 2 users	0b	R/W
2	ser_id_pw2_w	0: Serial ID registers write access not allowed for Level 2 users 1: Serial ID registers write access allowed for Level 2 users	0b	R/W
1	diag2_pw2_w	0: Diagnostics 2 registers write access not allowed for Level 2 users 1: Diagnostics 2 registers write access allowed for Level 2 users	0b	R/W
0	diag1_pw2_w	0: Diagnostics 1 registers write access not allowed for Level 2 users 1: Diagnostics 1 registers write access allowed for Level 2 users	0b	R/W

Page: 04h
Address: 9Dh
Register Name: WR_ACCESS2_1
Default Value: 00h
Description: Write Access Level 2 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw2_w	0: Table 04h registers write access not allowed for Level 2 users 1: Table 04h registers write access allowed for Level 2 users	0b	R/W

Page: 04h
Address: 9Eh
Register Name: WR_ACCESS3_0
Default Value: 00h
Description: Write Access Level 3 Register 0

Bit(s)	Name	Description	Default	Type
7	tbl3_pw3_w	0: Table 03h registers write access not allowed for Level 3 user 1: Table 03h registers write access allowed for Level 3 users	0b	R/W
6	pgrm_pw3_w	0: Program/Data registers write access not allowed for Level 3 users 1: Program/Data registers write access allowed for Level 3 users	0b	R/W
5	sfp_rsvd_pw3_w	0: Reserved registers write access not allowed for Level 3 users 1: Reserved registers write access allowed for Level 3 users	0b	R/W
4	vnd_spcfc_pw3_w	0: Vendor registers write access not allowed for Level 3 users 1: Vendor registers write access allowed for Level 3 users	0b	R/W
3	usr_wrt_pw3_w	0: User registers write access not allowed for Level 3 users 1: User registers write access allowed for Level 3 users	0b	R/W
2	ser_id_pw3_w	0: Serial ID registers write access not allowed for Level 3 users 1: Serial ID registers write access allowed for Level 3 users	0b	R/W
1	diag2_pw3_w	0: Diagnostics 2 registers write access not allowed for Level 3 users 1: Diagnostics 2 registers write access allowed for Level 3 users	0b	R/W
0	diag1_pw3_w	0: Diagnostics 1 registers write access not allowed for Level 3 users 1: Diagnostics 1 registers write access allowed for Level 3 users	0b	R/W

Page: 04h
Address: 9Fh
Register Name: WR_ACCESS3_1
Default Value: 00h
Description: Write Access Level 3 Register 1

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved	0000 000b	R/W
0	tbl4_pw3_w	0: Table 04h registers write access not allowed for Level 3 users 1: Table 04h registers write access allowed for Level 3 users	0b	R/W

Page: 04h
Address: D4h
Register Name: DIG_FILT_BPASS
Default Value: 00h
Description: Bypass Digital Filter Register

Bit(s)	Name	Description	Default	Type
7:5	RSVD	Reserved	000b	R/W
4	bias_cur_val	1: bypass digital filter 0: digital filter is used	0b	R/W
3	aux_val	1: bypass digital filter 0: digital filter is used	0b	R/W
2	rx_pwr_val	1: bypass digital filter 0: digital filter is used	0b	R/W
1	ext_cur_val	1: bypass digital filter 0: digital filter is used	0b	R/W
0	ext_temp_val	1: bypass digital filter 0: digital filter is used	0b	R/W

Page: 04h
Address: D5h
Register Name: DIG_FILT_CTRL
Default Value: 1Ah
Description: Digital Filter Control Register

Bit(s)	Name	Description	Default	Type
7:5	RSVD	Reserved	000b	R/W
4:2	dig_filt_gain	000: Multiplied by 0 001: Multiplied by 1/8 010: Multiplied by 1/4 011: Multiplied by 1/2 100: Multiplied by 2 101: Multiplied by 4 110: Multiplied by 3	110b	R/W
1:0	dig_filt_div	00: divided by 1 01: divided by 2 10: divided by 4 11: divided by 8	10b	R/W

Page: 04h
Address: D6h
Register Name: BIAS_CUR_FINAL_0
Default Value: 00h
Description: Bias Current Output Filter Register 0

Bit(s)	Name	Description	Default	Type
7:0	bias_curr_final[7:0]	Bias Cur output filter value LSB	00h	R

Page: 04h
Address: D7h
Register Name: BIAS_CUR_FINAL_1
Default Value: 00h
Description: Bias Current Output Filter Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	bias_curr_final[11:8]	Bias Cur output filter value MSB. Latched when register BIAS_CUR_FINAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 04h
Address: D8h
Register Name: AUX_FINAL_0
Default Value: 00h
Description: AUX Output Filter Register 0

Bit(s)	Name	Description	Default	Type
7:0	aux_final[7:0]	Aux output filter value LSB.	00h	R

Page: 04h
Address: D9h
Register Name: AUX_FINAL_1
Default Value: 00h
Description: AUX Output Filter Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	aux_final[11:8]	Aux output filter value MSB. Latched when register AUX_FINAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 04h
Address: DAh
Register Name: RX_PWR_FINAL_0
Default Value: 00h
Description: RX Power Output Filter Register 0

Bit(s)	Name	Description	Default	Type
7:0	rx_pwr_final[7:0]	RX power output filter value LSB.	00h	R

Page: 04h
Address: DBh
Register Name: RX_PWR_FINAL_1
Default Value: 00h
Description: RX Power Output Filter Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	rx_pwr_final[11:8]	RX power output filter value MSB. Latched when register RX_PWR_FINAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 04h
Address: DEh
Register Name: EXT_TEMP_FINAL_0
Default Value: 00h
Description: External Temp Output Filter Register 0

Bit(s)	Name	Description	Default	Type
7:0	ext_temp_final[7:0]	External Temp output filter value LSB.	00h	R

Page: 04h
Address: DFh
Register Name: EXT_TEMP_FINAL_1
Default Value: 00h
Description: External Temp Output Filter Register 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3:0	ext_temp_final[11:8]	External Temp output filter value MSB. Latched when register EXT_TEMP_FINAL_0 is read. Note: This byte is only latched when read from internal MCU and not when read externally through SPI/I2C.	0000b	R

Page: 04h
Address: E0h
Register Name: A_LASER_CTRL2
Default Value: 00h
Description: Laser Control Register 2

Bit(s)	Name	Description	Default	Type
7	oc2	0: normal compensation on the output stage 1: add some RC to the outputs	0b	R/W
6	oc1	0: normal compensation on the output stage 1: add some RC to the outputs	0b	R/W
5	oc0	0: normal compensation on the output stage 1: add some RC to the outputs	0b	R/W
4	core_comp	0: normal compensation on the output stage 1: slows down the core of the output stage	0b	R/W
3	lr_comp_off	0: normal compensation on the output stage 1: disable the automatic low poly compensation of the output stage	0b	R/W
2	t_comp_off	0: normal compensation on the output stage 1: disable the automatic temperature compensation of the output stage	0b	R/W
1	bias_mon_mag	0: normal operation 1: A magnified version of the bias monitoring is available on the extra current input of the ADC_MUX	0b	R/W
0	short_z_offset	This bit is used to short the zero in the offset current generator block in case no ferrite is used on Vsense pin (the pin that generates the offset current) 0: normal operation (a ferrite is present on the board) 1: zero shorted out, no ferrite on the board	0b	R/W

Page: 04h
Address: E1h
Register Name: A_LASER_CTRL3
Default Value: 00h
Description: Laser Control Register 3

Bit(s)	Name	Description	Default	Type
7	c_off	0: default mode, a cap is connected to IbiasCA for better stability 1: the cap is disconnected.	0b	R/W
6	measure_rpoly	0: txpwr_mon ADC measures the tx power 1: txpwr_mon ADC measures the internal reference current source base on low poly R and at 250uA TYP	0b	R/W
5	measure_ib	0: txpwr_mon ADC measures the tx power 1: txpwr_mon ADC measures the bipolar base current. This can be done only if rs1_rate = 1	0b	R/W

Bit(s)	Name	Description	Default	Type
4	soft_tx_dis	Disable control through two-wire serial interface. When low, the bias and modulation outputs are disabled. When high, the laser driver bias and modulation outputs are enabled if all other conditions allow. Defaults to disabled (low) state upon power-up until DAC registers have been loaded from EEPROM 1: Enable laser driver 0: Disable laser driver	0b	R/W
3	eq1	Change the equalization characteristic	0b	R/W
2	eq_on	0: disable the equalizer 1: enable the equalizer	0b	R/W
1	bias_ratio1	Change the bias ratio	0b	R/W
0	bias_ratio0	Change the bias ratio	0b	R/W

Page: 04h
Address: E2h
Register Name: A_LASER_CTRL4
Default Value: 00h
Description: Laser Control Register 4

Bit(s)	Name	Description	Default	Type
7	beta_comp1	0: normal compensation on the output stage 1: disable the beta compensation of the output stage and force a constant current instead of the beta dependent current	0b	R/W
6	beta_comp0	0: normal compensation on the output stage 1: disable the beta compensation of the output stage and force a constant current instead of the beta dependent current beta_comp1 beta_comp0 Current 0 0 50uA 0 1 200uA 1 0 300uA 1 1 400uA	0b	R/W
5	tc2_off	0: normal compensation on the output stage 1: enable another type of automatic temperature compensation of the output stage (this compensation is not base on the beta measurement)	0b	R/W
4	dcd_cor_on	0: normal operation, no DCD correction 1: enable the internal DCD correction (pwa_en must be set to 1 and pwa_dac[5:0] to 00)	0b	R/W
3	edge-sel	When DIS_Mod_Rst bit is low: 0: a high at Pwdn/Rst pin initiate a POR 1: a falling edge at Pwdn/Rst pin initiate a POR	0b	R/W

Bit(s)	Name	Description	Default	Type
2	soft_rs1_rate	0: Enable transmit lower rate function (<4.5Gb/s) 1: Enable transmit full rate function (8.5Gb/s and above)	0b	R/W
1	hard_rs1_en	0: Pull down on GPIO3 not connected, 1: Pull down on GPIO3 connected	0b	R/W
0	rs1_rate	When hard_RS1_en=1, the voltage on GPIO3 is mapped to RS1_rate 0: Enable transmit lower rate function (<4.5Gb/s) 1: Enable transmit full rate function (8.5Gb/s and above)	0b	R/W

Page: 04h
Address: E3h
Register Name: LASER_STAT2
Default Value: 40h
Description: Laser Driver Status Register 2

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved	0b	R
6	eml_mode	1: Indicates the part is M02172	1b	R
5:0	RSVD	Reserved	00 0000b	R

Page: 04h
Address: E6h
Register Name: ANALOG_CTRL
Default Value: 00h
Description: Analog Control Register

Bit(s)	Name	Description	Default	Type
7:3	RSVD	Reserved	0000 0b	R/W
2	rxp_volcur_ctrl	0: RXP channel is in current mode 1: RXP channel is in voltage mode	0b	R/W
1	imax_ctrl	0: No extra 10% current is sent to TIA 1: Extra 10% current is sent to TIA	0b	R/W
0	RSVD	Reserved	0b	R/W