Integrated Device Technology, Inc.

256K x 16 CMOS STATIC RAM MODULE

IDT7M4016

FEATURES:

- High-density 4 megabit CMOS static RAM module
- Fast access time
  - commercial: 25ns (max.)
  - military: 35ns (max.)
- Low power consumption
- Available in 48-pin, 900 mil wide sidebrazed DIP (Dual In-line Package)
- Multiple GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

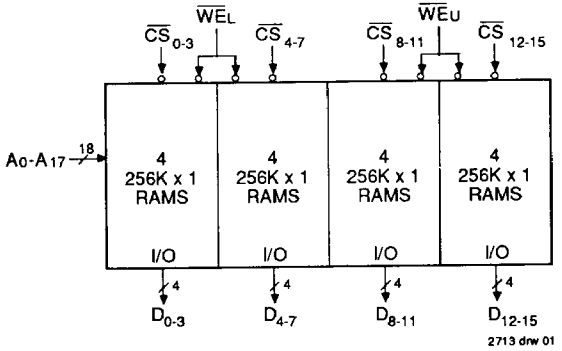
The IDT7M4016 is a 4 megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen (256K x 1) static RAMs in leadless chip carriers. The IDTM4016 is an upgrade from the IDT7M624 (64K x 16 RAM module) offering four times the memory density in the same size package. Making four chip select lines available (one for each group of four RAMs) allows the user to configure the memory into a 256K x 16, 512K x 8 or 1024K x 4 organization.

The IDT7M4016 is packaged in a 48-pin, 900 mil wide sidebrazed DIP. This enables four megabits of static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the IDT7M4016 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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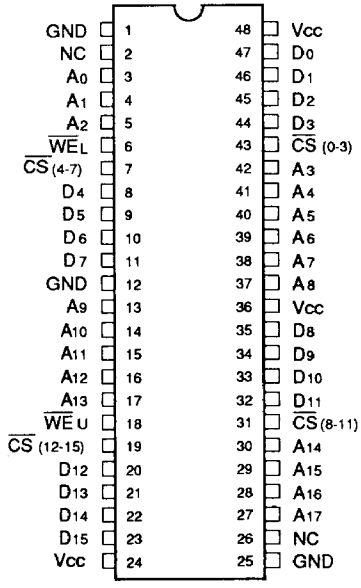
PIN CONFIGURATION (1)



2713 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimension, please refer to module drawing M15 in the packaging section.

PIN NAMES

Vcc	Power
GND	Ground
A0–A17	Addresses
D0–D15	Data Input/Output
$\overline{CS}$0-3	Chip Selects
$\overline{WE}$L	Write Enable (Lower Byte)
$\overline{WE}$U	Write Enable (Upper Byte)

2713 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2713 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2713 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	30	pF
CIN(A)	Input Capacitance (Address and Control)	VIN = 0V	200	pF
COUT	Output Capacitance	VOUT = 0V	30	pF

2713 tbl 04

NOTE:
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2713 tbl 05

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C + 125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2713 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2713 tbl 07

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

			IDT7M4016[1]		IDT7M4016[2]		
			Max.		Max.		
Symbol	Parameter	Test Conditions	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Current	V_{CC} = Max., CS ≤ V_{IL}, f = 0, Outputs Open	1760	—	1600	1760	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., CS ≤ V_{IL}, f = f_{MAX} Output Open	2560	—	2400	2560	mA
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, f = f_{MAX}, Ouputs Open	560	—	560	560	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or ≤ 0.2V	480	—	480	480	mA

2713 tbl 08

NOTES:
1. 25, 30ns
2. 35, 45, 55ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2713 tbl 09

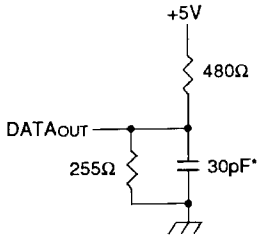


Figure 1. Output Load

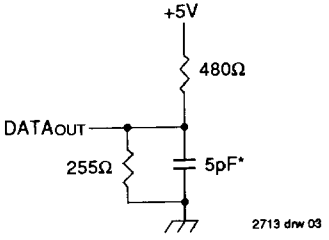


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7M4016S25 Com'l. Only		7M4016S30 Com'l. Only		7M4016S35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	13	—	17	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	25	—	30	—	35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{CW}	Chip Selection to End of Write	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	13	—	15	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2713 tbl 10

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameters	7M4016S45		7M4016S55		7M4016S70 Mil. Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	45	—	55	—	70	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	45	—	55	—	65	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	25	—	25	—	30	ns
t_{DW}	Data to Write Time Overlap	20	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

2713 tbl 11

NOTE:
1. This parameter is guaranteed by design, but not tested.

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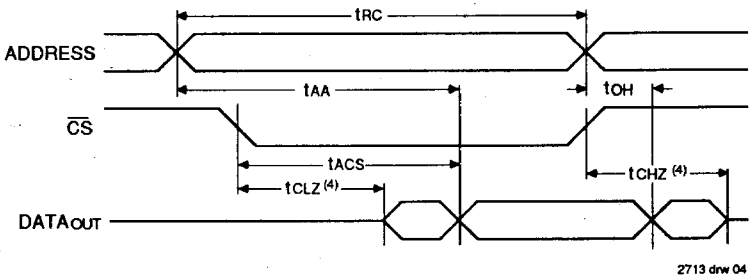
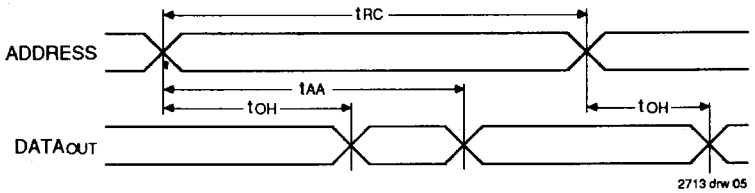
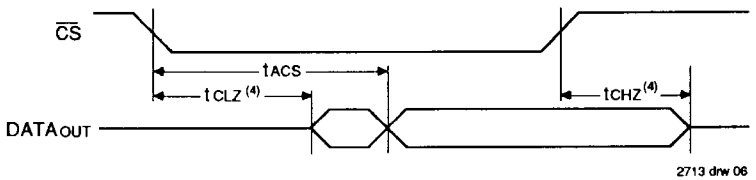
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2]

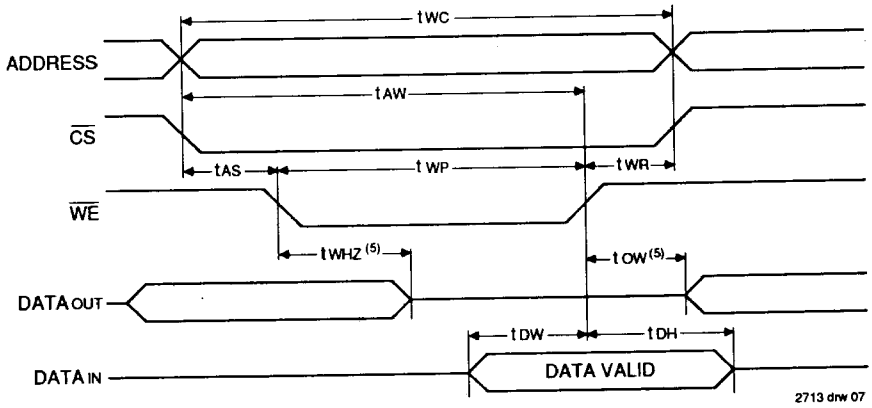


TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3]

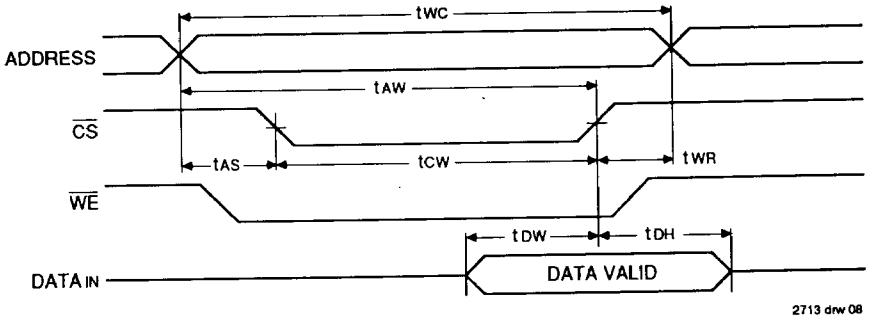


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

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ORDERING INFORMATION