## SPEED/PACKAGE AVAILABILITY

**8262—A,F,W**
**82S62—A,F**

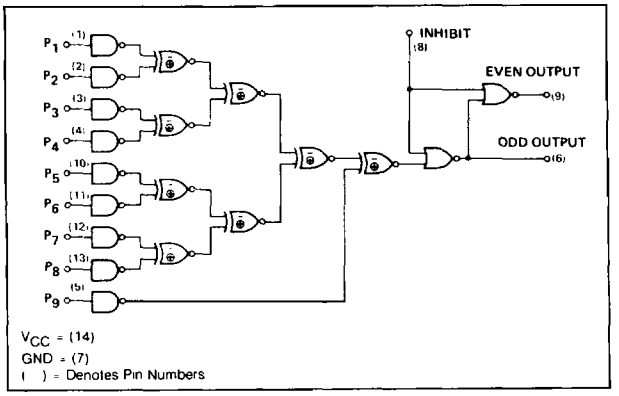
## DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

## LOGIC DIAGRAM




LOGIC EQUATIONS:

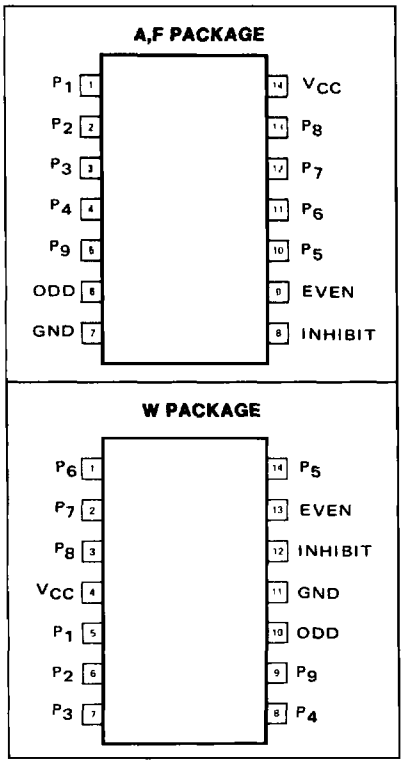
Odd =

$$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

Even =

$$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$$

## PIN CONFIGURATION




## TRUTH TABLE 8262

| MEASURE DELAY FROM | SWITCH POSITION | | | WAVEFORM | |
|---|---|---|---|---|---|
| | INH | $P_8$ | $P_9$ | EVEN | ODD |
| $P_8$ to ODD | 1 | 2 | 1 | | 1 |
| $P_9$ to ODD | 1 | 1 | 2 | | 2 |
| $P_8$ to EVEN | 1 | 2 | 1 | 2 | |
| $P_9$ to EVEN | 1 | 1 | 2 | 1 | |
| INH to EVEN | 2 | 1 | 1 | 2 | |

## SWITCHING CHARACTERISTICS $T_A$=25°C, $V_{CC}$=5V

| | PARAMETER | TEST CONDITIONS | 8262 TYP | 8262 MAX | 82S62 TYP | 82S62 MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on Times | | | | | | |
| | $P_1$-$P_8$ to even | Under test: pulse | 35 | 50 | 17 | 23 | ns |
| | $P_1$-$P_8$ to odd | Under test: pulse | 30 | 45 | 18 | 28 | ns |
| | $P_9$ to even | Under test: pulse | 20 | 35 | 7 | 12 | ns |
| | $P_9$ to odd | Under test: pulse | 15 | 30 | 12 | 18 | ns |
| | Inhibit to even | Inhibit: pulse | 8 | 15 | 7 | 9 | ns |
| | Inhibit to odd | Inhibit: pulse | 8 | 15 | 6 | 9 | ns |
| $t_{off}$ | Turn-off times | | | | | | |
| | $P_1$-$P_8$ to even | Under test: pulse | 38 | 55 | 17 | 23 | ns |
| | $P_1$-$P_8$ to odd | Under test: pulse | 32 | 45 | 18 | 28 | ns |
| | $P_9$ to even | Under test: pulse | 23 | 40 | 7 | 12 | ns |
| | $P_9$ to odd | Under test: pulse | 20 | 35 | 12 | 18 | ns |
| | Ihhibit to even | Inhibit: pulse | 10 | 18 | 7 | 9 | ns |
| | Inhibit to odd | Inhibit: pulse | 10 | 18 | 6 | 9 | ns |

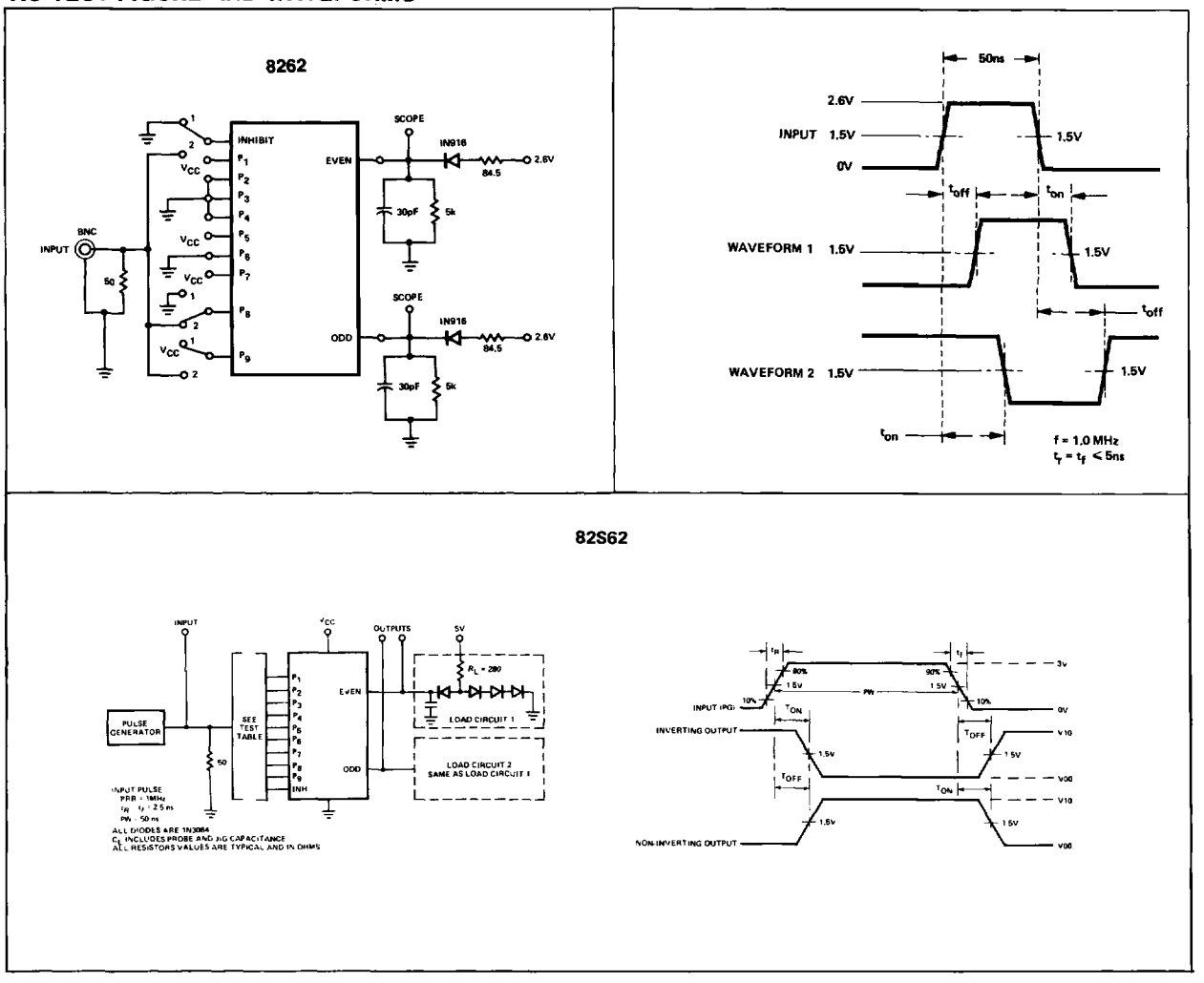
## AC TEST TABLE—82S62

| Test | Inputs | | | | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | P1 | P2 | P3 | P4 | P5 | P6 | P7 | P8 | P9 | INH | Even | Odd |
| 1 | PG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | T | T |
| 2 | 0 | 0 | PG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | T | T |
| 3 | 0 | 0 | 0 | 0 | PG | 0 | 0 | 0 | 0 | 0 | T | T |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | PG | 0 | 0 | 0 | T | T |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PG | 0 | T | T |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PG | T | |
| 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | PG | | T |

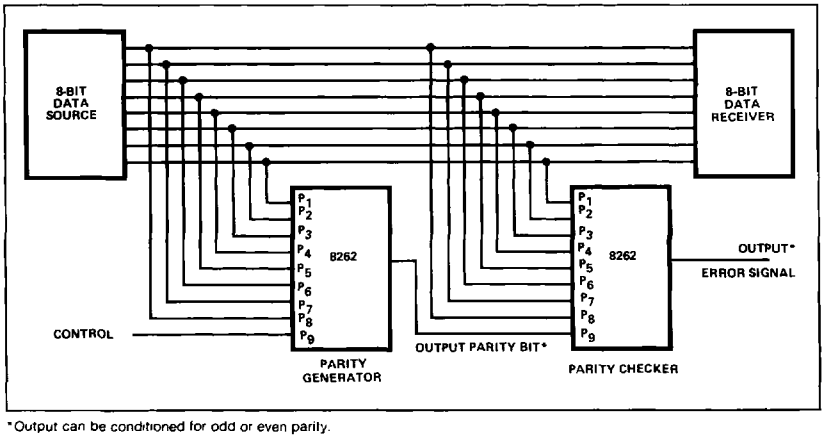
"1" = 2.7V "0" = Ground "T" = Test

NOTE:
1. AC Test Jig Must Not Have Any Switches.
2. AC Test Jigs Must Have Less Than ⅛ Inch Lead Length From Package Pins.

## AC TEST FIGURE AND WAVEFORMS




## TYPICAL APPLICATION




*Output can be conditioned for odd or even parity.

An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.

An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

LOGIC