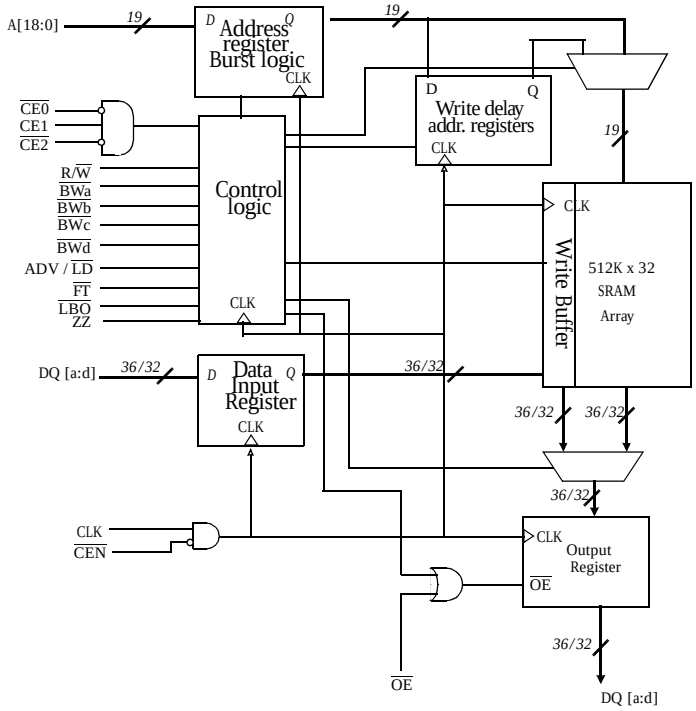
2.5V 512K × 32/36 SRAM with NTD™

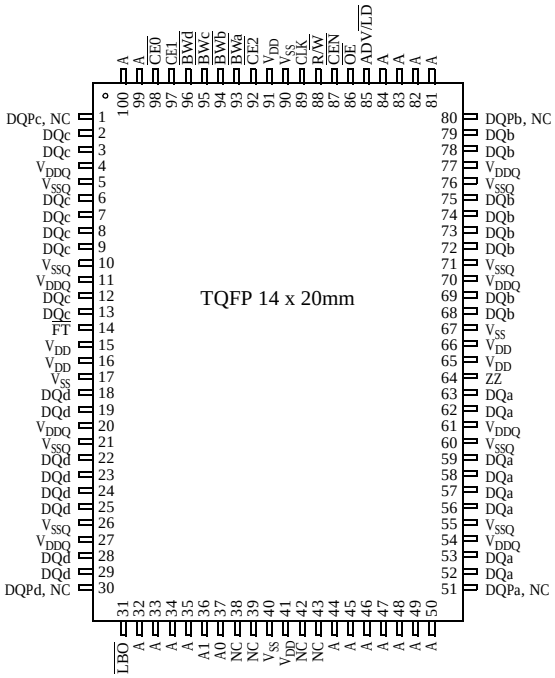
Features

- Organization: 524,288 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 200 MHz in LVTTL/LVCMOS
- Fast clock to data access: 3/3.4/4 ns
- Fast $\overline{OE}$ access time: 3/3.4/4 ns
- Fully synchronous operation
- "Flow-through" or "pipelined" mode
- Asynchronous output enable control
- Economical 100-pin TQFP package
- 119 BGA (7 x 17 Ball Grid Array package)
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 2.5V core power supply
- 2.5V I/O operation
- Self-timed write cycles
- Interleaved or linear burst modes
- Snooze mode for standby operation

Logic block diagram



Pin arrangement for TQFP (top view)



Note: Pins 1,30,51,80 are NC for ×32

Selection guide

	-200	-166	-100	Units
Minimum cycle time	5	6	10	ns
Maximum pipelined clock frequency	200	166	100	MHz
Maximum pipelined clock access time	3.0	3.4	4.0	ns
Maximum operating current	280	230	150	mA
Maximum standby current	100	70	50	mA
Maximum CMOS standby current (DC)	30	30	30	mA

NTD™ is a trademark of Alliance Semiconductor Corporation.

119 BGA Pin Out - Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	A	A	A	V_{DDQ}
B	NC	CE1	A	ADV/$\overline{LD}$	A	$\overline{CE2}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQC	DQPc	V_{SS}	NC	V_{SS}	DQpb	DQb
E	DQC	DQC	V_{SS}	$\overline{CE0}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQC	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQC	DQC	$\overline{BWc}$	A	$\overline{BWb}$	DQb	DQb
H	DQC	DQC	V_{SS}	R/$\overline{W}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{Bwa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CEN}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	NC
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}