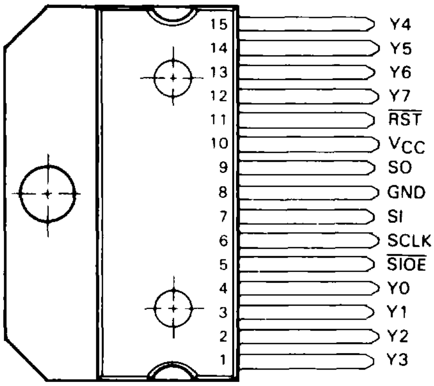
- **8-Bit Serial-In Parallel-Out Driver**
- **1-A Output Current Capability per Channel or 8-A Total Current**
- **Over-Current Limiting and Out-of-Saturation Voltage Protection on Driver Outputs**
- **Contains Eight Open-Collector Saturating Sink Outputs with Low On-State Voltage**
- **High-Impedance Inputs with Hysteresis are Compatible with TTL or CMOS Levels**
- **Very Low Standby Power . . . 20 mW Typical**
- **Status of Output Drivers May Be Monitored at Serial Output**
- **3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections**
- **25-V Transient Clamping with Inductive Switching on Outputs, 40-mJ Rating per Driver Output**

KV PLASTIC PACKAGE
(TOP VIEW)



The tab is electrically connected to pin 8.

description

The TPIC2801 is a monolithic BIDFET† integrated circuit that is designed to sink currents up to 1 A at 30 V simultaneously at each of eight driver outputs under serial input data control. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

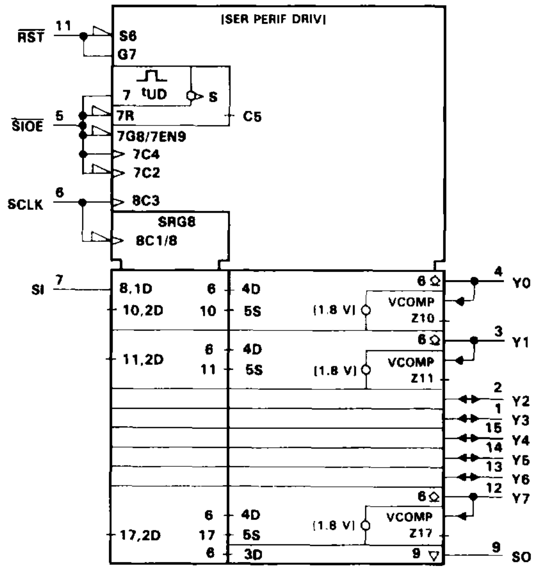
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic high bit at SI_n turns the corresponding output driver (Y_n) off. A logic low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of serial clock (SCLK) input in 8-bit bytes with data for Y7 output (MSB) first and data for Y0 output (LSB) last. Both SI and SCLK are active when serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. An activated driver output will be unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

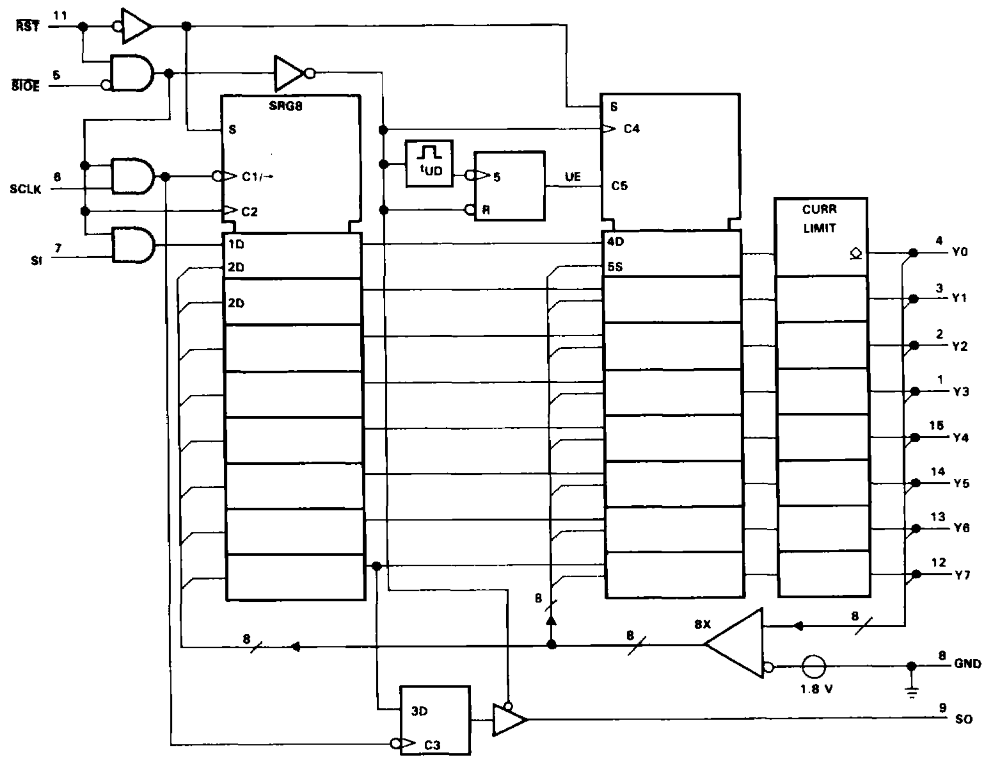
† BIDFET – Bipolardouble-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The current out of this pin is potentially as high as 4 A if all outputs are on. This ground is used for both logic and power circuits
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This pin is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
$\overline{SCLK}$	6	I	Serial Clock. This pin clocks the shift register. The serial output (SO) will change state on the rising edge of this clock and serial input (SI) data will be accepted on the falling edge.
SI	7	I	Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be off and a low will turn it on.
$\overline{SIOE}$	5	I	Serial Input-Output Enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver for the serial output (SO) pin is enabled when this pin is low, provided $\overline{RST}$ is high.
SO	9	O	Serial Output. This pin is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this pin indicates that the corresponding power output (Y_n) is high. This could mean that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage sense indicator. A low on this pin for a data bit indicates that the corresponding power output (Y_n) is low (an "on" output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power Outputs. The outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, but the current limiting is set to a minimum of 1.2 A. The active-low outputs also have voltage clamps set at about 35 V for recirculation of inductive load current. Internal 90-kΩ pull-down resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

PRINCIPLES OF OPERATION

timing data transfer

Figure 1 shows the overall 8-bit data-byte transfer to and from the TPIC2801 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represents the conditions at the Y-driver outputs at time t_0. The data at SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 1 on the SI input, input data DI7 is clocked in at time t_1, DI6 is clocked in at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of $\overline{SIOE}$ parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO) and this allows other devices to be cascaded in a daisy chain with the TPIC2801. Once the last data bit has been shifted into the TPIC2801, the $\overline{SIOE}$ input should be pulled high. The clock (SCLK) input should be low at both transitions of the $\overline{SIOE}$ input to avoid any false clocking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever the $\overline{SIOE}$ is high. At the rising edge of the $\overline{SIOE}$ input, the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 100-μs delay timer is also started on this rising edge. During the time delay, the outputs will be protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions will be inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay has ended, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

PRINCIPLES OF OPERATION

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the the device. If the diagnostic bit for that output comes back as a low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte should be clocked into the TPIC2801. The diagnostic bit clocked back from the TPIC2801 in the subsequent data transfer should indicate a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte. After a sufficient time delay, another control byte (same byte can be used) is clocked in. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high will result.

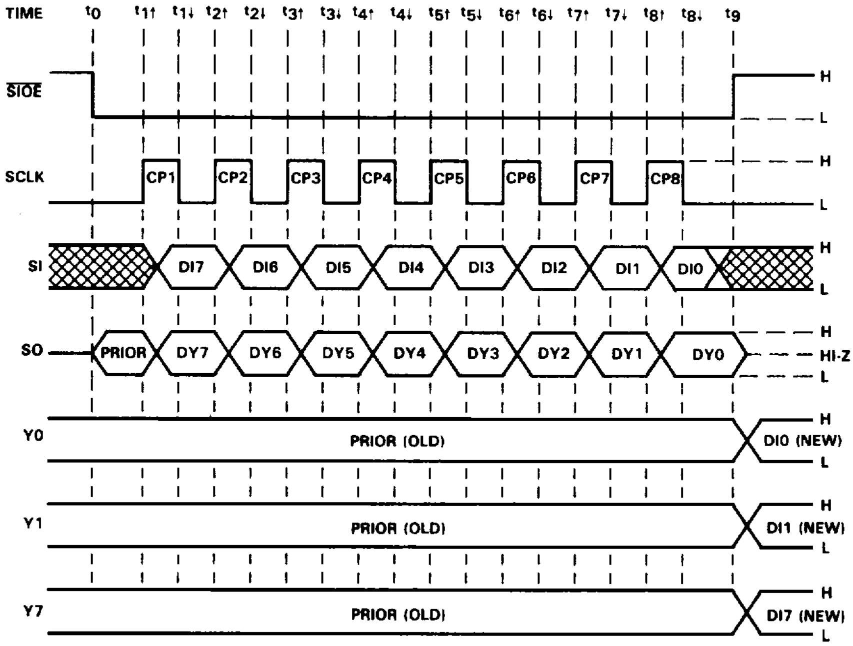
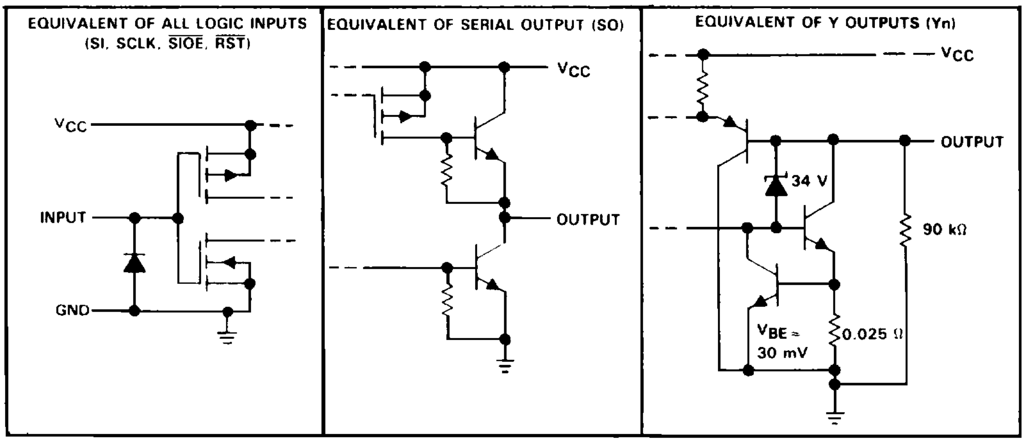


FIGURE 1. DATA-BYTE TRANSFER TIMING

schematics of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Input voltage, V_I	7 V
Output voltage range at SO	−0.3 V to 7 V
Input current, I_I	−15 mA
Peak output sink current at Y, I_O repetitive, t_w = 10 ms, duty cycle = 50%, see Notes 2 and 3	Internally Limited
Continuous output current at Y, I_O (see Note 3)	1 A
Peak current through GND terminal: Nonrepetitive t_w = 0.2 ms	− 8A
Repetitive, t_w = 10 ms, duty cycle = 50%	−6 A
Continuous current through GND terminal	−4.5 A
Output clamp energy, E_{OK} (after turning off $I_{O(on)}$ = 0.5 A)	40 mJ
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4)	3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4)	25 W
Operating case or virtual-junction temperature range	−55°C to 150°C
Storage temperature range	− 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Each Y output is individually current limited with a typical over-current limit of about 1.4 A.
3. Multiple Y outputs of this device may conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND current must fall within the GND-terminal current range.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate lineraly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings must not be exceeded.

TEXAS INSTRUMENTS
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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.7 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	−0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			30	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	−40	25	105	°C

timing requirements (see Figure 2)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Clock frequency				0	500	kHz
t_{wSCLKH}	Pulse duration, SCLK high				840		ns
t_{wSCLKL}	Pulse duration, SCLK low				840		ns
t_{wRST}	Pulse duration, $\overline{RST}$ low				1000		ns
t_{su1}	Setup time	$\overline{SIOE}$↓	SCLK↑		1000		ns
t_{su2}	Setup time	SCLK↓	$\overline{SIOE}$↑		1000		ns
t_{su3}	Setup time	SI	SCLK↓		500		ns
t_{h1}	Hold time	SCLK↓	SI		500		ns
t_r	Rise time (SCLK, SI, $\overline{SIOE}$)					2	µs
t_f	Fall time (SCLK, SI, $\overline{SIOE}$)					2	µs

electrical characateristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A, output programmed off and current shunted to ground		30	36	40	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				1	mA
$I_{O(CL)}$	Output current limit	V_O = 3 V with output programmed on		1.05	1.4		A
$V_{O(on)}$	On-state output voltage	With output programmed on	I_{OL} = 0.5 A		0.4	0.5	V
			I_{OL} = 0.75 A		0.6	1	V
			I_{OL} = 1 A, During unlatch disable		0.8	1.5	V
V_{TOS}	Out of saturation threshold voltage	With output programmed on and an over-current fault condition		1.6	1.8	2	V

shift register (inputs SI, $\overline{SIOE}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.7 V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.2 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.25	V
I_I	Input current	V_I = 0 to V_{CC}		±10	µA
C_i	Inpout capacitance	V_I = 0 to V_{CC}		20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = −0.8 mA		V_{CC} −1.3			V
I_O	Output current	V_O = 0 to V_{CC}, $\overline{SIOE}$ input high				±10	µA
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs	T_J = 105°C			150	mA
			T_J = 25°C			200	
			T_J = −40°C			250	
I_{CC}	Supply current	All outputs off	T_J = 25°C		4	10	mA
C_O	Output capacitance	V_O = 0 to V_{CC}, $\overline{SIOE}$ input high				20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperatures (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}$↓	SO	C_L = 20 pF, R_L = 2 kΩ, See Figure 3		1000	ns
t_{dis}	Disable time	$\overline{SIOE}$↑	SO	C_L = 20 pF, R_L = 2 kΩ, See Figure 3		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF, See Figure 4		740	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}$↑	Y_n	C_L = 20 pF, R_L = 5 Ω, See Figure 5	75	250	µs
$t_{r(so)}$	Rise time, SO			C_L = 200 pF, See Figure 4		150	ns
$t_{f(so)}$	Fall time, SO			C_L = 200 pF, See Figure 4		150	ns
$t_{d(on)}$	Delay time, turn-on	$\overline{SIOE}$↑	Y_n	I_{OL} = 500 mA, C_L = 20 pF, R_L = 28 Ω, See Figure 6		10	µs
$t_{d(off)}$	Delay time, turn-off	$\overline{SIOE}$↑	Y_n	I_{OL} = 500 mA, C_L = 20 pF, R_L = 28 Ω, See Figure 6		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF, See Figure 4	0		ns

PARAMETER MEASUREMENT INFORMATION

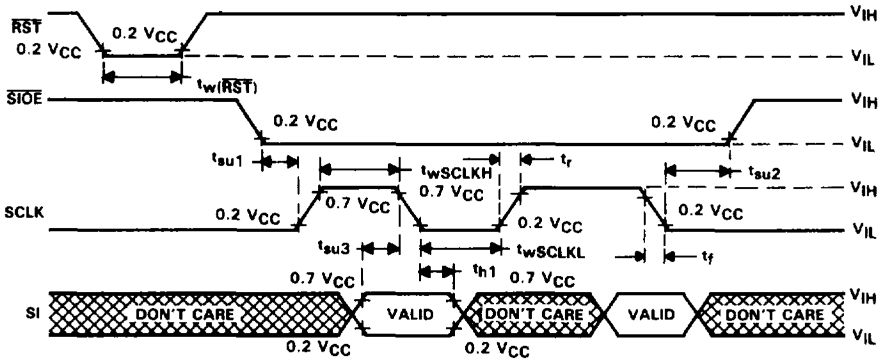
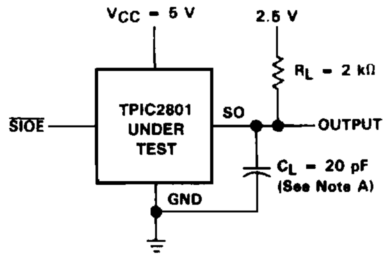
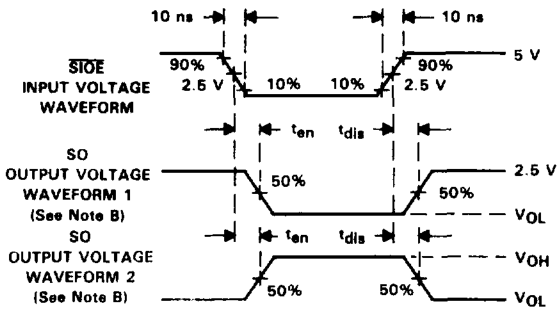


FIGURE 2. INPUT TIMING WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



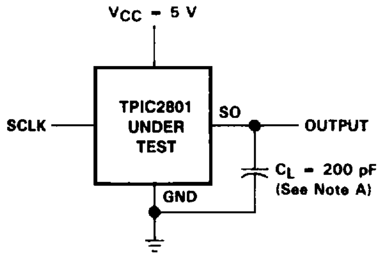
TEST CIRCUIT FOR ENABLE AND DISABLE TIMES



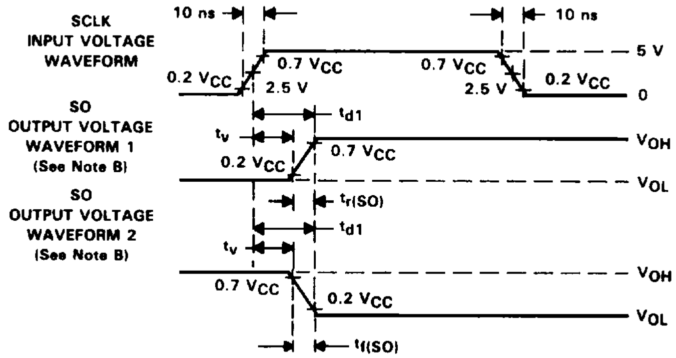
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control when $\overline{SIOE}$ is high.

FIGURE 3. VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



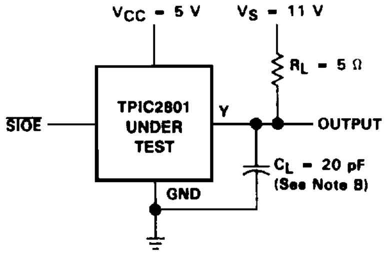
TEST CIRCUIT FOR VALID DATA
DELAY TIME t_{d1} AND VALID TIME t_v



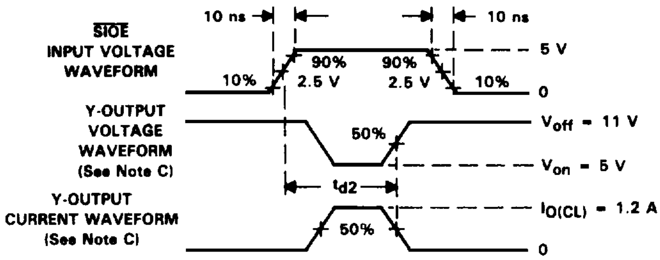
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from low to high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low.

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



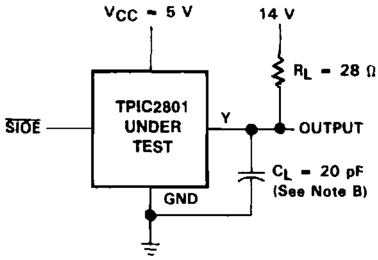
TEST CIRCUIT FOR UNLATCH DISABLE DELAY TIME t_{d2}
(See Note A)



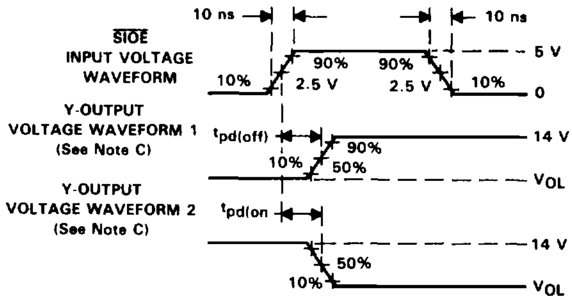
NOTES: A. t_{d2} = delay until Y-output current goes off under fault condition.
B. C_L includes probe and jig capacitance.
C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{\text{SIOE}}$ causes the output to switch from being off to being on.
D. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation threshold voltage, V_{TOS}. Thus, $V_{OL} = V_{on} > V_{TOS(max)} = 1.98$ V.

FIGURE 5. VOLTAGE AND CURRENT WAVEFORMS FOR UNLATCH DISABLE DELAY

PARAMETER MEASUREMENT INFORMATION



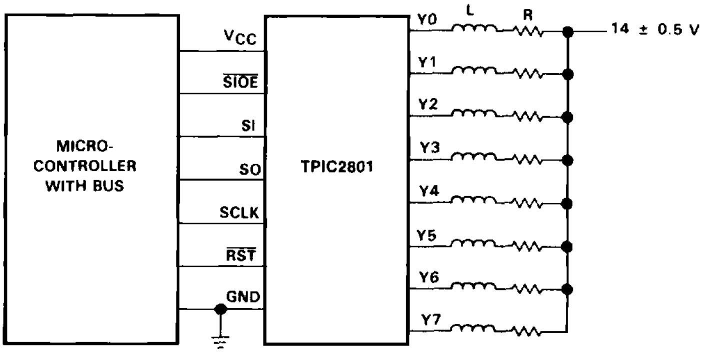
TEST CIRCUIT FOR TURN-OFF $t_{d(off)}$
AND TURN-ON $t_{d(on)}$ DELAY TIMES
(See Note A)



NOTES: A. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$.
B. C_L includes probe and jig capacitance.
C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

FIGURE 6. VOLTAGE WAVEFORMS FOR TURN-OFF AND TURN-ON DELAY TIMES

TYPICAL APPLICATION DATA



V_{CC} = 5 V ± 5%
R = 30 Ω ± 5%
L = 10 mH ± 10%
8 LOADS UP TO 0.5 A EACH

FIGURE 7. MICROCONTROLLER DRIVING EIGHT LOADS USING A TPIC2801 FOR LOAD INTERFACE