40192B

PRESETTABLE UP/DOWN COUNTERS (DUAL CLOCK WITH RESET)
40192B – BCD TYPE 4019B – BINARY TYPE

- INDIVIDUAL CLOCK LINES FOR COUNTING UP OR COUNTING DOWN
- SYNCHRONOUS HIGH-SPEED CARRY AND BORROW PROPAGATION DELAYS FOR CASCADING
- ASYNCHRONOUS RESET AND PRESET CAPABILITY
- MEDIUM-SPEED OPERATION - f_{CL} = 8 MHz (TYP.) @ 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 40192B, HCC 40193B,** (extended temperature range) and the **HCF 40192B, HCF 40193B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 40192B** Presettable BCD Up/Down Counter and the **HCC/HCF 40193B** Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET ENABLE control, individual CLOCL UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided. The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low. The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high. The CARRY and BORROW signals are high when the counter is counting up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the BORROW and CARRY outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding package.

ABSOLUTE MAXIMUM RATINGS

V_{DD} *	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

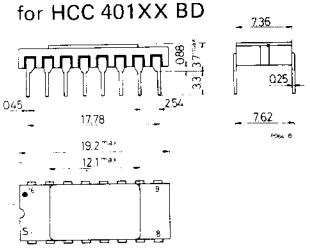
* All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS:

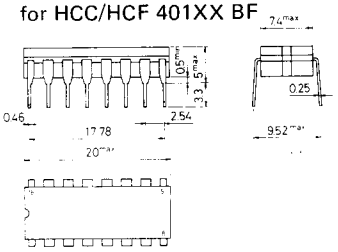
HCC 401XX BD for dual in-line ceramic package
HCC 401XX BF for dual in-line ceramic package, frit seal
HCC 401XX BK for ceramic flat package
HCF 401XX BE for dual in-line plastic package
HCF 401XX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

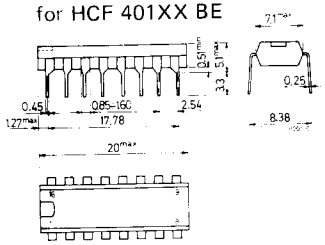
Dual in-line ceramic package
for HCC 401XX BD



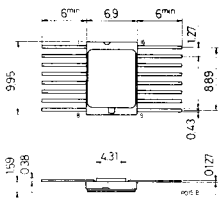
Dual in-line ceramic package
for HCC/HCF 401XX BF



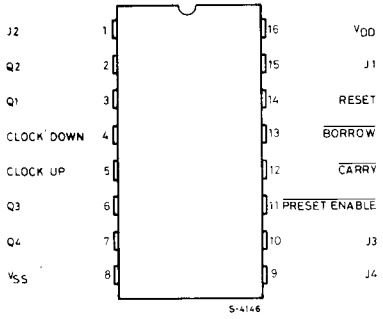
Dual in-line plastic package
for HCF 401XX BE



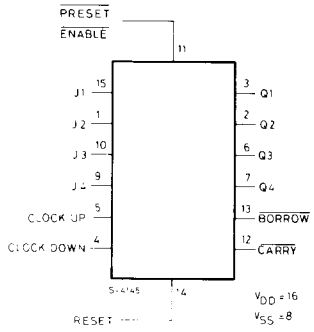
Ceramic flat package
for HCC 401XX BK



PIN CONNECTIONS



FUNCTIONAL DIAGRAM

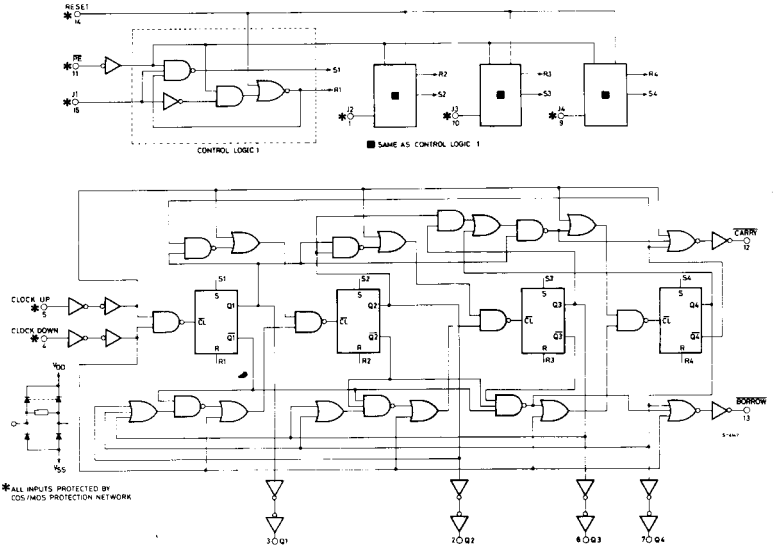


RECOMMENDED OPERATING CONDITIONS

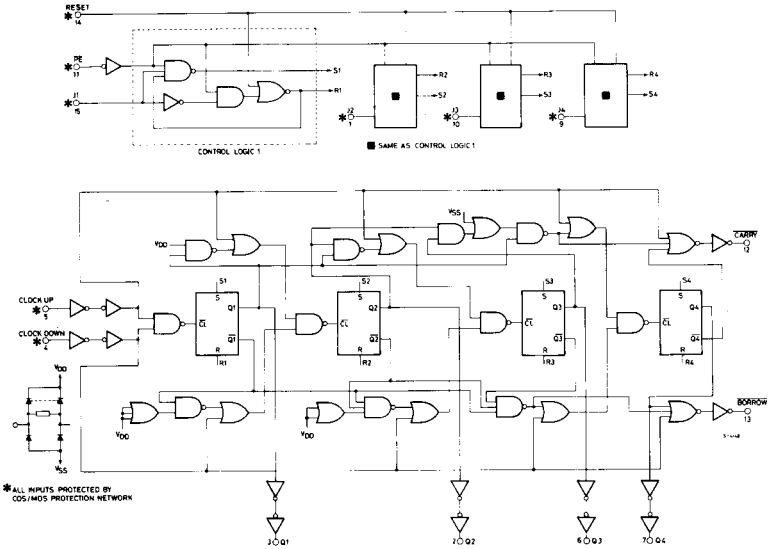
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAMS

For **40192B** (BCD)



For **40193B** (Binary)



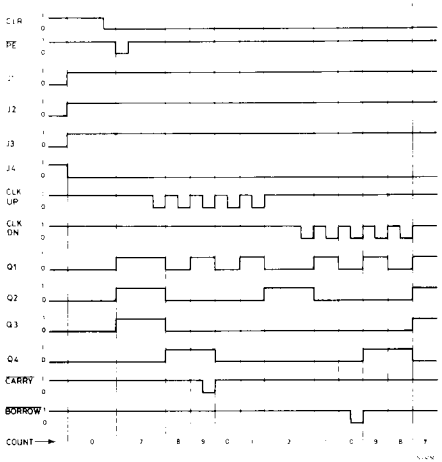
TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$	RESET	ACTION
⌐¬	1	1	0	COUNT UP
¬⌐	1	1	0	NO COUNT
1	⌐¬	1	0	COUNT DOWN
1	¬⌐	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

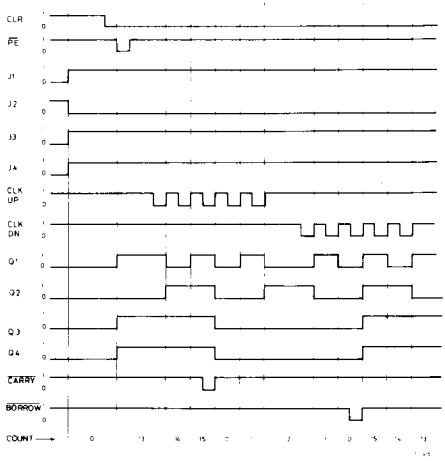
1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

TIMING DIAGRAMS

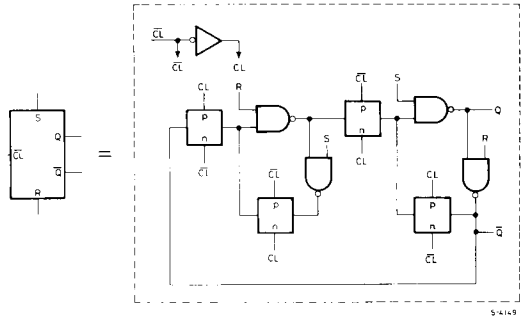
For **40192B** (BCD)



For **40193B** (Binary)



Internal logic of flip-flop



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		$\pm$0.1		$\pm 10^{-5}$	$\pm$0.1		$\pm$ 1	μA
		HCF types	0/15			15		$\pm$0.3		$\pm 10^{-5}$	$\pm$0.3		$\pm$ 1	
C_I	Input capacitance			Any input						5	7.5			pF

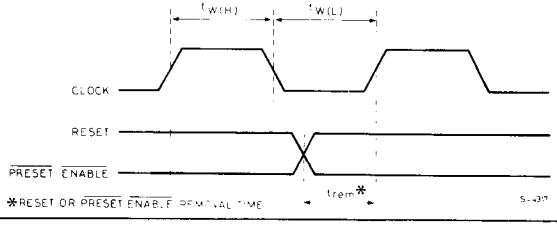
* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values in 0.3%/°C, all input rise and fall time = 20 ns)

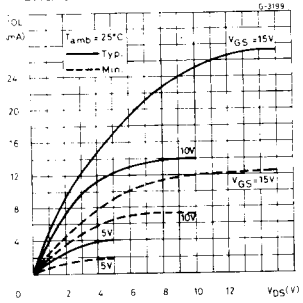
Parameter		Test conditions	Values			Unit
		V_{DD}(V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time Clock up or Clock Down to Q Reset to Q	5		250	500	ns
		10		120	240	
		15		90	180	
	$\overline{PE}$ to Q	5		200	400	ns
		10		100	200	
		15		70	140	
	Clock up to $\overline{Carry}$ Clock Down to $\overline{Borrow}$	5		160	320	ns
		10		80	160	
		15		60	120	
	$\overline{Reset}$ or $\overline{PR}$ to $\overline{Borrow}$ or $\overline{Carry}$	5		300	600	ns
		10		150	300	
		15		110	220	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{rem} *	Removal time Reset or $\overline{PE}$	5	80	40		ns
		10	40	20		
		15	30	15		
t_W	Clock input pulse width Reset	5	480	240		ns
		10	300	150		
		15	260	130		
	$\overline{PE}$	5		120	240	ns
		10		85	170	
		15		70	140	
	Clock	5		90	180	ns
		10		45	90	
		15		30	60	
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			15	
		15			5	
f_{CL}	Maximum clock input frequency	5	2	4		MHz
		10	4	8		
		15	5.5	11		

* The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

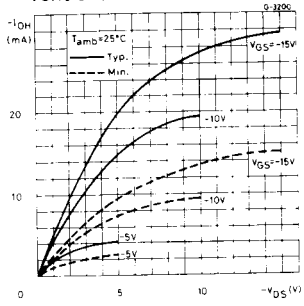
Timing diagram defining t_{rem}



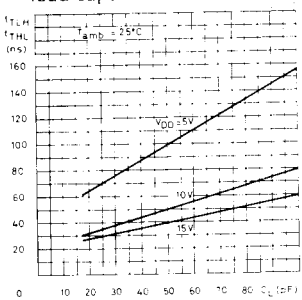
Output low (sink) current characteristics



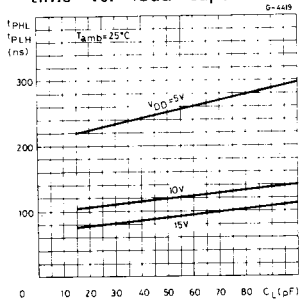
Output high (source) current characteristics



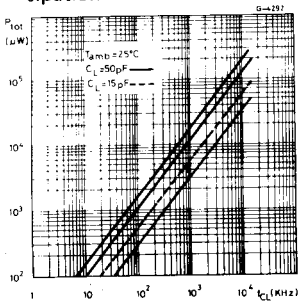
Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance

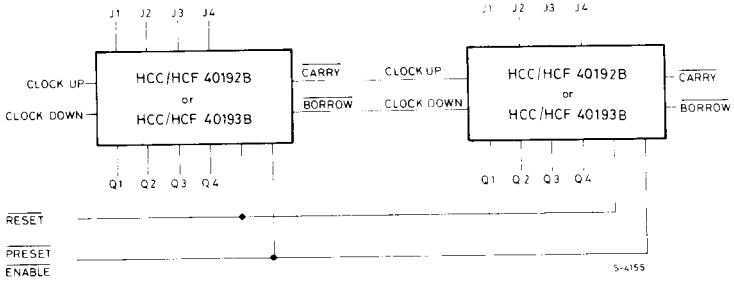


Typical dynamic power dissipation



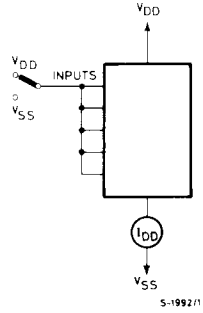
TYPICAL APPLICATION

Cascaded counter packages

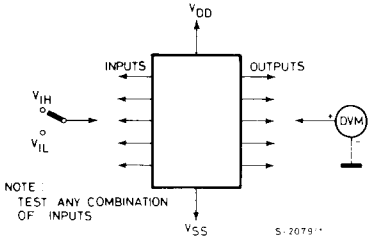


TEST CIRCUITS

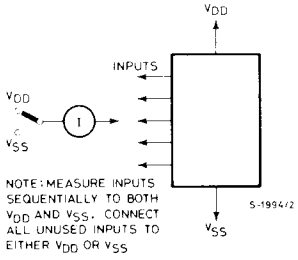
Quiescent device current



Input voltage



Input leakage current



Dynamic power dissipation