# HB56U432B/SB-6BN/7BN/8BN

## 4,194,304-word × 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-558(Z)
Preliminary
Rev.0.0
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## Description

The HB56U432 is a 4M × 32 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117405BS) sealed in SOJ package.

An outline of the HB56U432 is 72-pin single in-line package.

The HB56U432 offers Extended Data Out (EDO) Page Mode as a high speed access mode.

Therefore, the HB56U432 makes high density mounting possible without surface mount technology. The HB56U432 provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ on the module board.

## Features

- 72-pin single in-line package
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: $t_{RAC}$ = 60/70/80 ns (max)
  - — Access time: $t_{CAC}$ = 15/18/20 ns (max)
- Low power dissipation
  - — Active mode: 4.62/4.20/3.78 W (max)
  - — Standby mode (TTL): 84 mW (max)
  - — Standby mode (CMOS): 42 mW (max)
- EDO mode capability
- 2,048 refresh cycle: 32 ms

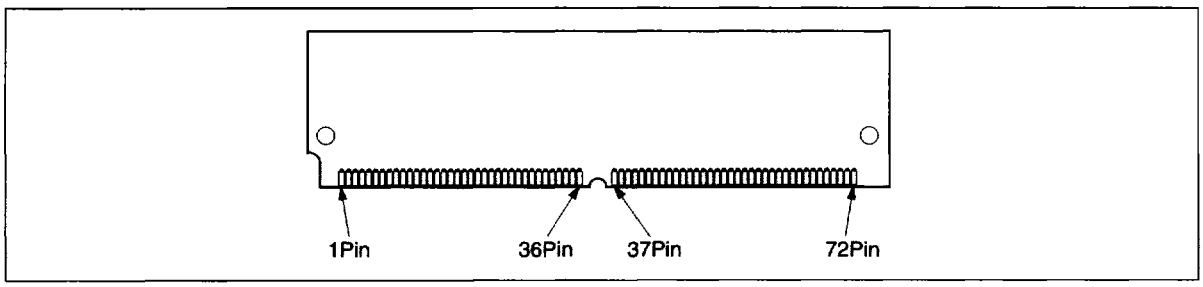
Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

## Ordering Information

| Type No. | Access time | Package | Contact pad |
|---|---|---|---|
| HB56U432B-6BN | 60 ns | 72-pin SIP socket type | Gold |
| HB56U432B-7BN | 70 ns | | |
| HB56U432B-8BN | 80 ns | | |
| HB56U432SB-6BN | 60 ns | 72-pin SIP socket type | Solder |
| HB56U432SB-7BN | 70 ns | | |
| HB56U432SB-8BN | 80 ns | | |

## Pin Arrangement



## Pin Arrangement

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 19 | A10 | 37 | NC | 55 | DQ11 |
| 2 | DQ0 | 20 | DQ4 | 38 | NC | 56 | DQ27 |
| 3 | DQ16 | 21 | DQ20 | 39 | $V_{SS}$ | 57 | DQ12 |
| 4 | DQ1 | 22 | DQ5 | 40 | $\overline{CAS0}$ | 58 | DQ28 |
| 5 | DQ17 | 23 | DQ21 | 41 | $\overline{CAS2}$ | 59 | $V_{CC}$ |
| 6 | DQ2 | 24 | DQ6 | 42 | $\overline{CAS3}$ | 60 | DQ29 |
| 7 | DQ18 | 25 | DQ22 | 43 | $\overline{CAS1}$ | 61 | DQ13 |
| 8 | DQ3 | 26 | DQ7 | 44 | $\overline{RAS0}$ | 62 | DQ30 |
| 9 | DQ19 | 27 | DQ23 | 45 | NC | 63 | DQ14 |
| 10 | $V_{CC}$ | 28 | A7 | 46 | NC | 64 | DQ31 |
| 11 | NC | 29 | NC | 47 | $\overline{WE}$ | 65 | DQ15 |
| 12 | A0 | 30 | $V_{CC}$ | 48 | NC | 66 | NC |
| 13 | A1 | 31 | A8 | 49 | DQ8 | 67 | PD1 |
| 14 | A2 | 32 | A9 | 50 | DQ24 | 68 | PD2 |
| 15 | A3 | 33 | NC | 51 | DQ9 | 69 | PD3 |
| 16 | A4 | 34 | $\overline{RAS2}$ | 52 | DQ25 | 70 | PD4 |
| 17 | A5 | 35 | NC | 53 | DQ10 | 71 | NC |
| 18 | A6 | 36 | NC | 54 | DQ26 | 72 | $V_{SS}$ |

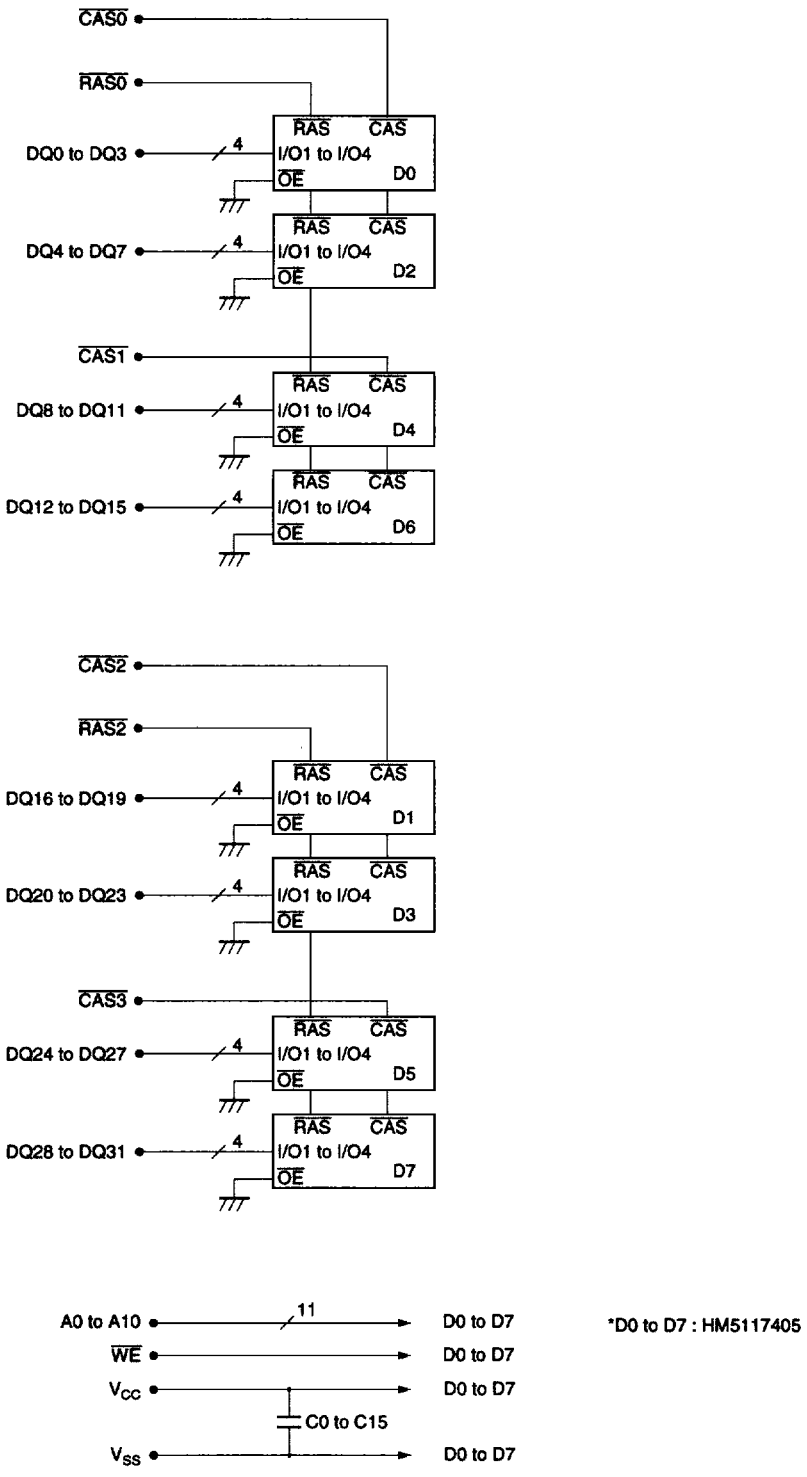
## Pin Description

| Pin Name | Function |
|---|---|
| A0 to A10 | Address Input: A0 to A10<br>Row Address: A0 to A10<br>Column Address: A0 to A10<br>Refresh Address: A0 to A10 |
| DQ0 to DQ31 | Data-in/Data-out |
| $\overline{RAS0}$, $\overline{RAS2}$ | Row Address Strobe |
| $\overline{CAS0}$ to $\overline{CAS3}$ | Column Address Strobe |
| $\overline{WE}$ | Read/Write Enable |
| $V_{CC}$ | Power Supply (+5 V) |
| $V_{SS}$ | Ground |
| PD1 to PD5 | Presence detect pin |
| NC | Non Connection |

## Presence Detect Pin Arrangement

| Pin No. | Pin Name | 60 ns | 70 ns | 80 ns |
|---|---|---|---|---|
| 67 | PD1 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 68 | PD2 | NC | NC | NC |
| 69 | PD3 | NC | $V_{SS}$ | NC |
| 70 | PD4 | NC | NC | $V_{SS}$ |
| 66 | PD5 | NC | NC | NC |

## Block Diagram



## Absolute Maximum Ratings

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | (Input) | Vin | −1.0 to +7.0 | V |
| | (Output) | Vout | −1.0 to +7.0 | V |
| Supply voltage relative to $V_{SS}$ | | $V_{CC}$ | −1.0 to +7.0 | V |
| Short circuit output current | | Iout | 50 | mA |
| Power dissipation | | Pt | 8 | W |
| Operating temperature | | Topr | 0 to +70 | °C |
| Storage temperature | | Tstg | −55 to +125 | °C |

## Electrical Characteristics

**Recommended DC Operating Condition** (Ta = 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{SS}$ | 0 | 0 | 0 | V | |
| | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | 1 |
| Input high voltage | $V_{IH}$ | 2.4 | — | 5.5 | V | 1 |
| Input low voltage | $V_{IL}$ | −1.0 | — | 0.8 | V | 1 |

Note: 1. All voltage referenced to $V_{SS}$.

## DC Characteristics (Ta = 0 to 70°C, $V_{CC}$ = 5 V ± 5%, $V_{SS}$ = 0 V)

| | | 60 ns | | 70 ns | | 80 ns | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Test condition** | **Note** |
| Operating current | $I_{CC1}$ | — | 880 | — | 800 | — | 720 | mA | $t_{RC}$ = min | 1, 2 |
| Standby current | $I_{CC2}$ | — | 16 | — | 16 | — | 16 | mA | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>Dout = High-Z | |
| | | — | 8 | — | 8 | — | 8 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥<br>$V_{CC}$ – 0.2 V<br>Dout = High-Z | |
| $\overline{RAS}$-only refresh current | $I_{CC3}$ | — | 880 | — | 800 | — | 720 | mA | $t_{RC}$ = min | 2 |
| Standby current | $I_{CC5}$ | — | 40 | — | 40 | — | 40 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IL}$<br>Dout = enable | 1 |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 880 | — | 800 | — | 720 | mA | $t_{RC}$ = min | |
| EDO page mode current | $I_{CC7}$ | — | 880 | — | 800 | — | 720 | mA | $t_{HPC}$ = min | 1, 3 |
| Input leakage current | $I_{LI}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 7.0 V | |
| Output leakage current | $I_{LO}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vout ≤ 7.0 V<br>Dout = disable | |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA | |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA | |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected, $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.

## Capacitance (Ta = 25°C, $V_{CC}$ = 5 V ± 5%)

| **Parameter** | **Symbol** | **Typ** | **Max** | **Unit** | **Notes** |
|---|---|---|---|---|---|
| Input capacitance (Address) | $C_{I1}$ | — | 60 | pF | 1 |
| Input capacitance ($\overline{WE}$) | $C_{I2}$ | — | 71 | pF | 1 |
| Input capacitance ($\overline{RAS}$) | $C_{I3}$ | — | 43 | pF | 1 |
| Input capacitance ($\overline{CAS}$) | $C_{I4}$ | — | 29 | pF | 1 |
| I/O capacitance (DQ) | $C_{I/O}$ | — | 17 | pF | 1, 2 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = $V_{IH}$ to disable Dout.

## AC Characteristics (Ta = 0 to 70°C, $V_{CC}$ = 5 V ± 5%, $V_{SS}$ = 0 V) *1, *2

### Test Conditions

- Input rise and fall times: 2 ns
- Input levels: $V_{IL}$ = 0 V, $V_{IH}$ = 3 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + $C_L$ (100 pF) (Including scope and jig)

### Read, Write and Refresh Cycles (Common parameters)

| | | 60 ns | | 70 ns | | 80 ns | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Random read or write cycle time | $t_{RC}$ | 104 | — | 124 | — | 144 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | |
| $\overline{CAS}$ precharge time | $t_{CP}$ | 10 | — | 13 | — | 15 | — | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 60 | 10000 | 70 | 10000 | 80 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 10 | 10000 | 13 | 10000 | 15 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column address hold time | $t_{CAH}$ | 10 | — | 13 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 45 | 20 | 52 | 20 | 60 | ns | 3 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 4 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 15 | — | 18 | — | 20 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 48 | — | 58 | — | 68 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CAS}$ delay time from Din | $t_{DZC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Transition time (rise and fall) | $t_T$ | 2 | 50 | 2 | 50 | 2 | 50 | ns | 5 |
| Refresh period (2,048 cycle) | $t_{REF}$ | — | 32 | — | 32 | — | 32 | ms | |

## Read Cycle

| | | 60 ns | | 70 ns | | 80 ns | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 6, 7 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | 15 | — | 18 | — | 20 | ns | 7, 8, 15 |
| Access time from address | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 7, 9, 15 |
| Read command setup time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 10 |
| Read command hold time from $\overline{RAS}$ | $t_{RCHR}$ | 60 | — | 70 | — | 80 | — | ns | |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 10 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| Column address to $\overline{CAS}$ lead time | $t_{CAL}$ | 18 | — | 23 | — | 28 | — | ns | |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | |
| Output data hold time | $t_{OH}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off time | $t_{OFF}$ | — | 15 | — | 15 | — | 15 | ns | 11 |
| $\overline{CAS}$ to Din delay time | $t_{CDD}$ | 15 | — | 18 | — | 20 | — | ns | |
| Output data hold time from $\overline{RAS}$ | $t_{OHR}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off to $\overline{RAS}$ | $t_{OFR}$ | — | 15 | — | 15 | — | 15 | ns | |
| Output buffer turn-off to $\overline{WE}$ | $t_{WEZ}$ | — | 15 | — | 15 | — | 15 | ns | |
| $\overline{WE}$ to Din delay time | $t_{WED}$ | 15 | — | 18 | — | 20 | — | ns | |
| $\overline{RAS}$ to Din delay time | $t_{RDD}$ | 15 | — | 18 | — | 20 | — | ns | |

## Write Cycle

| | | 60 ns | | 70 ns | | 80 ns | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Write command setup time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| Write command hold time | $t_{WCH}$ | 10 | — | 13 | — | 15 | — | ns | |
| Write command pulse width | $t_{WP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Data-in setup time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 13 |
| Data-in hold time | $t_{DH}$ | 10 | — | 13 | — | 15 | — | ns | 13 |

### Refresh Cycle

| Parameter | Symbol | 60 ns Min | 60 ns Max | 70 ns Min | 70 ns Max | 80 ns Min | 80 ns Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{CAS}$ setup time (CBR refresh cycle) | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CAS}$ hold time (CBR refresh cycle) | $t_{CHR}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ setup time (CBR refresh cycle) | $t_{WRP}$ | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{WE}$ hold time (CBR refresh cycle) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 0 | — | 0 | — | 0 | — | ns | |

### Fast Page Mode Cycle

| Parameter | Symbol | 60 ns Min | 60 ns Max | 70 ns Min | 70 ns Max | 80 ns Min | 80 ns Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Fast page mode cycle time | $t_{HPC}$ | 25 | — | 30 | — | 35 | — | ns | 16 |
| Fast page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | — | 100000 | — | 100000 | — | 100000 | ns | 14 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | — | 35 | — | 40 | — | 45 | ns | 7, 15 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 35 | — | 40 | — | 45 | — | ns | |
| Output data hold time from $\overline{CAS}$ low | $t_{DOH}$ | 3 | — | 3 | — | 3 | — | ns | 7, 15 |
| Read command hold time from $\overline{CAS}$ precharge | $t_{RCHO}$ | 35 | — | 40 | — | 45 | — | ns | |

Notes: 1. AC measurements assume $t_T$ = 2 ns.

2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh).

   If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

3. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.

4. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.

5. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).

6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.

7. Measured with a load circuit equivalent to 1TTL loads and 100 pF.

8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).

9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).

10. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycles.

11. $t_{OFF}$ (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

12. $t_{WCS}$ is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle.

14. $t_{RASP}$ defines $\overline{RAS}$ pulse width in EDO page mode cycles.

15. Access time is determined by the longer of $t_{AA}$ or $t_{CAC}$ or $t_{CPA}$.

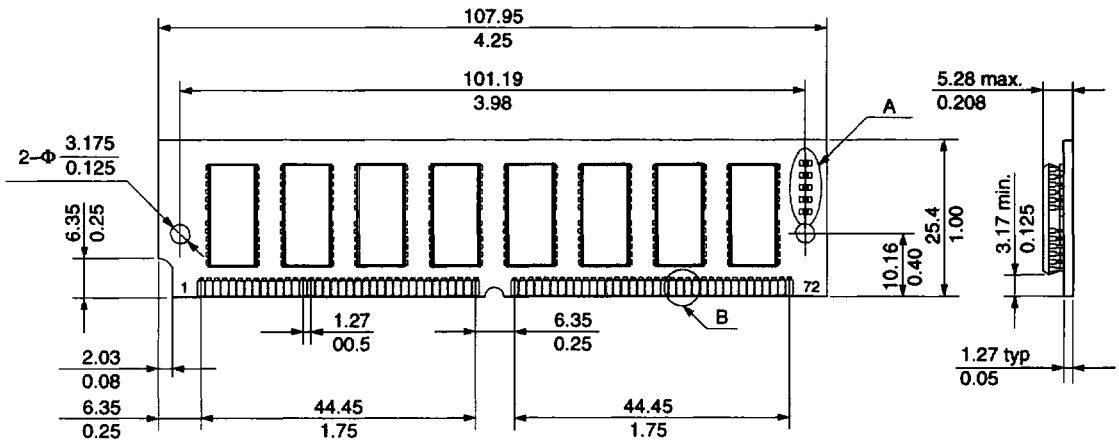
16. $t_{HPC}$ (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles.

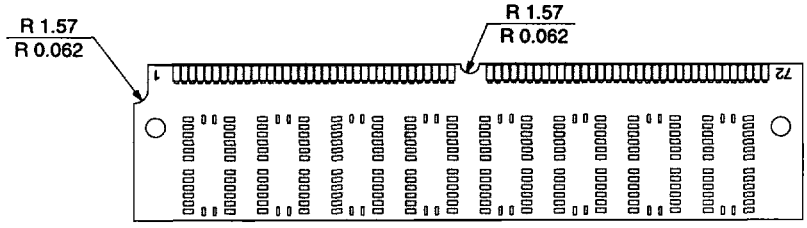
## Timing Waveform

Refer to the HB56E836/HB56E436 Series.

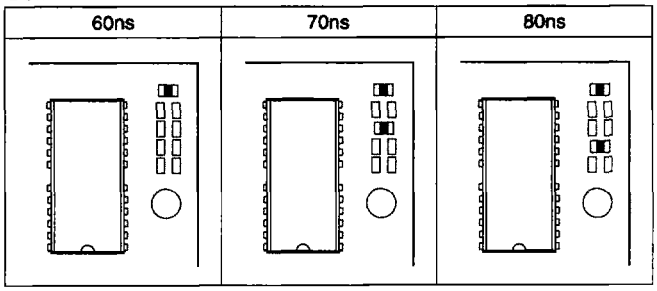
## Physical Outline

Unit: mm/inch

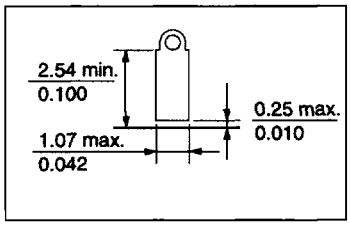



Detail A




Detail A




Note : Following the specification of the contact pads.

| Part No. | Contact pad |
|---|---|
| HB56U432B–XX | gold |
| HB56U432SB–XX | solder |