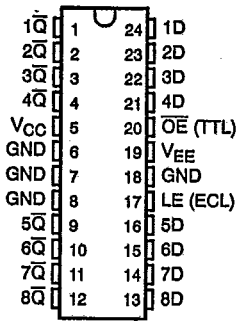
T-52-11

SN10KHT5575, SN100KT5575
OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

D3602, JULY 1990

- ECL and TTL Control Inputs
- Inverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configuration Minimizes High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

The SN10KHT5575 and SN100KT5575 are octal ECL-to-TTL inverting translators designed to provide efficient translation between 10KH or 100K ECL signal environments, respectively, and a TTL signal environment. These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, receivers, and transmitters.

The eight latches of the '5575 are transparent D-type latches. When latch enable (LE) is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverse of the levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive give the device the capability to drive bus lines without need for interface or pullup components. The $\overline{OE}$ input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN10KHT5575 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C. The SN100KT5575 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT (TTL)
$\overline{OE}$	LE	D	$\overline{Q}$
L	L	L	H
L	L	H	L
L	H	X	$\overline{Q}_0$
H	X	X	Z

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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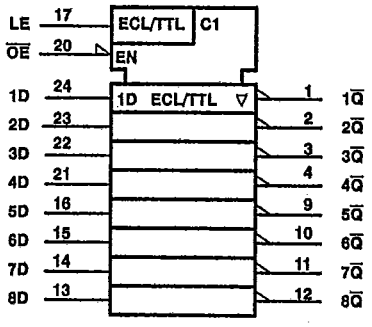
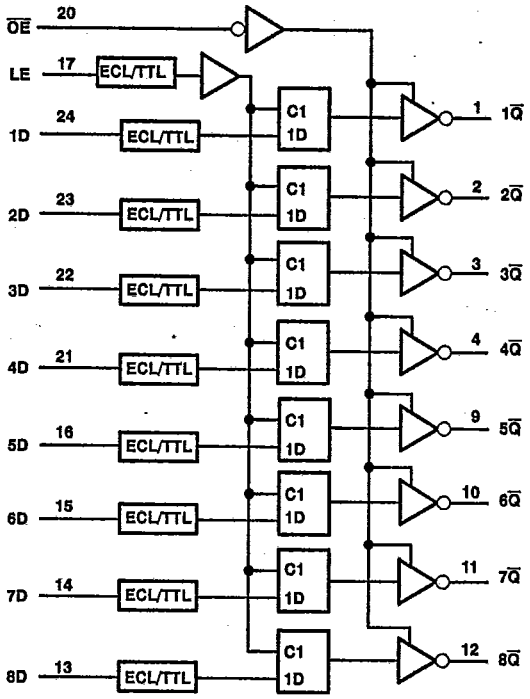
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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