

# Accutek Microcircuit Corporation

## AK594096BS / AK594096BG 4,194,304 Word by 9 Bit CMOS Dynamic Random Access Memory

### DESCRIPTION

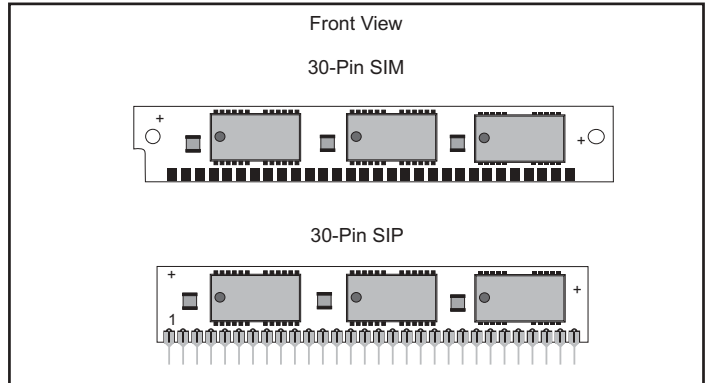
The Accutek AK594096 high density memory module is a CMOS random access memory organized in 4 Meg x 9 bit words. The assembly consists of two 4 Meg x 4 and one 4 Meg x 1 DRAMs, mounted on the front side of a printed circuit board in 30 pad SIM (leadless) or 30 pin SIP (leaded) configuration with JEDEC-standard pinouts. Designed especially for low-height applications such as VMEbus boards, this low profile module is 0.550 inch high.

The operation is identical to nine 4 Meg x 1 DRAMs. For the lower eight bits, data input is tied to data output and brought out separately for each bit, with common  $\overline{RAS}$  and  $\overline{CAS}$  control. This common I/O feature dictates the use of early-write cycles to prevent contention of data in and data out. Since the Write-Enable ( $\overline{WE}$ ) signal must always go low before  $\overline{CAS}$  in a write cycle, Read-Write and Read-Modify-Write operation is not possible. For the ninth bit, data in ( $D_9$ ) and data out ( $Q_9$ ) pins are brought out separately and controlled by a separate  $\overline{PCAS}$  for that bit.

### FEATURES

- 4,194,304 x 9 bit organization
- Low Profile 30 pad (SIM) Single In-Line Memory
- Low Profile 30 pin (SIP) Single In-Line package
- JEDEC standard pinout
- Common  $\overline{CAS}$ ,  $\overline{RAS}$  and  $\overline{WE}$  for the lower eight bits
- $\overline{CAS}$ -before- $\overline{RAS}$  refresh
- Refresh cycle 2048 cycles in 32 mSEC

- Power  
1.450 Watt Max Active, 70 nSEC  
1.610 Watt Max Active, 60 nSEC  
16.5 mWatt Max Standby
- Operating free air temperature  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$
- Downward compatible with AK591024 and AK59256
- Upward compatible with AK5916384
- Fast Page Mode and Static Column Mode versions available, nibble mode is not possible



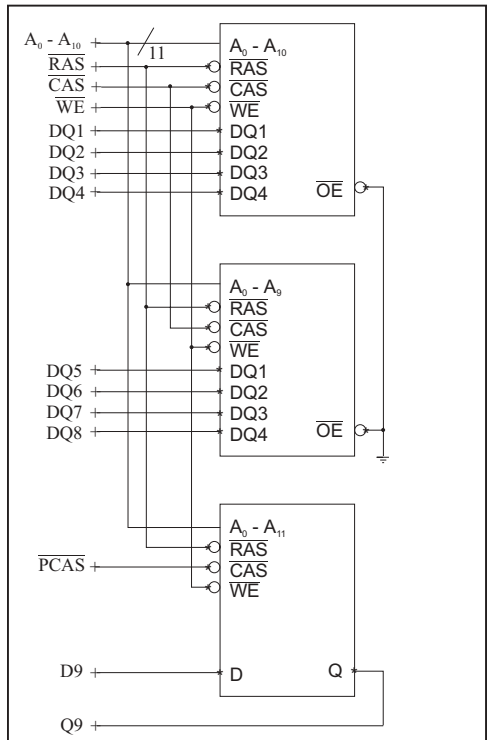
### PIN NOMENCLATURE

$A_0 - A_{10}$	Address Inputs
$\overline{RAS}_0$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$DQ_1 - DQ_8$	Data In/Data Out
$D_9$	Data In
$Q_9$	Data Out
$V_{cc}$	5v Supply
$V_{ss}$	Ground
NC	No Connect

### PIN ASSIGNMENT

1	$V_{cc}$	16	$DQ_5$
2	$\overline{CAS}$	17	A8
3	$DQ_1$	18	A9
4	A0	19	A10
5	A1	20	$DQ_6$
6	$DQ_2$	21	$\overline{WE}$
7	A2	22	$V_{ss}$
8	A3	23	$DQ_7$
9	$V_{ss}$	24	NC
10	$DQ_3$	25	$DQ_8$
11	A4	26	NC
12	A5	27	$\overline{RAS}_0$
13	$DQ_4$	28	NC
14	A6	29	NC
15	A7	30	$V_{cc}$

### FUNCTIONAL DIAGRAM



### MODULE OPTIONS

Leadless SIM: AK594096BS
Leaded SIP: AK594096BG

## ORDERING INFORMATION

### PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8																				
<b>1 Product</b>	<b>AK = Accuthek Memory</b>																											
<b>2 Type</b>	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM																											
<b>3 Organization/Word Width</b>	1 = by 1    16 = by 16 4 = by 4    32 = by 32 8 = by 8    36 = by 36 9 = by 9																											
<b>4 Size/Bits Depth</b>	64 = 64K    4096 = 4 MEG 256 = 256K    8192 = 8 MEG 1024 = 1 MEG    16384 = 16 MEG																											
<b>5 Package Type</b>	G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP)																											
<b>6 Special Designation</b>	P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram																											
<b>7 Separator</b>	- = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In																											
<b>8 Speed (first two significant digits)</b>	<table border="0"> <tr> <td>DRAMS</td> <td>SRAMS</td> <td></td> <td></td> </tr> <tr> <td>50 = 50 nS</td> <td>8 = 8 nS</td> <td></td> <td></td> </tr> <tr> <td>60 = 60 nS</td> <td>10 = 10 nS</td> <td></td> <td></td> </tr> <tr> <td>70 = 70 nS</td> <td>12 = 12 nS</td> <td></td> <td></td> </tr> <tr> <td>80 = 80 nS</td> <td>15 = 15 nS</td> <td></td> <td></td> </tr> </table>								DRAMS	SRAMS			50 = 50 nS	8 = 8 nS			60 = 60 nS	10 = 10 nS			70 = 70 nS	12 = 12 nS			80 = 80 nS	15 = 15 nS		
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The numbers and coding on this page do not include all variations available but are show as examples of the most widely used variations. Contact Accuthek if other information is required.

## EXAMPLES:

### AK594096BGP-70

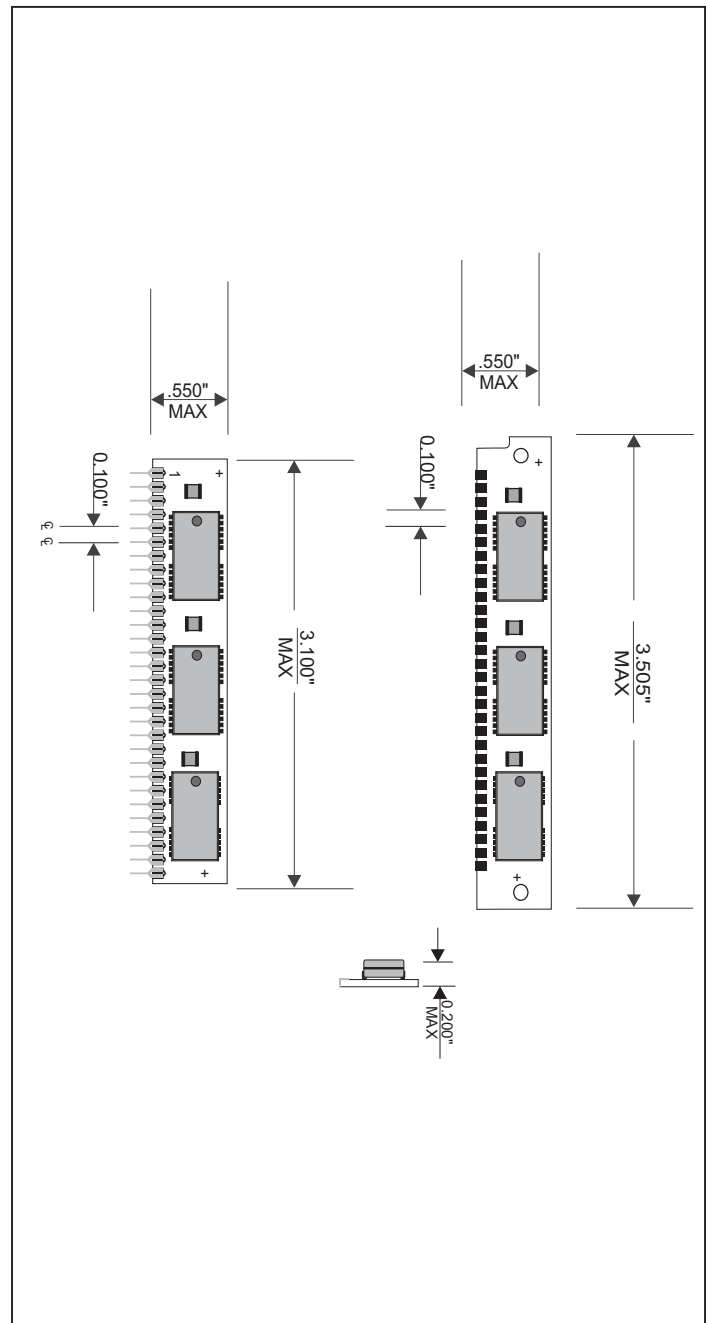
4 Meg x 9, CMOS Dynamic RAM, Leaded SIP, Page Mode, Commercial, 70 nSEC Access Time

### AK594096BSP-60

4 Meg x 9, CMOS Dynamic RAM, Leadless SIM, Page Mode, Commercial, 60 nSEC Access Time

## MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.



**ACCUTEK MICROCIRCUIT CORPORATION**  
 BUSINESS CENTER at NEWBURYPORT  
 2 NEW PASTURE ROAD, SUITE 1  
 NEWBURYPORT, MA 01950-4054  
 VOICE: 978-465-6200 FAX: 978-462-3396  
 Email: sales@accutekmicro.com  
 Internet: www.accutekmicro.com