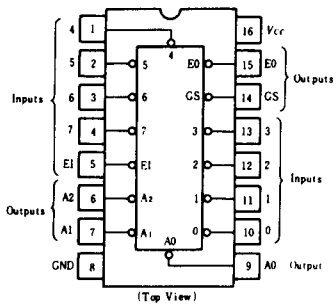
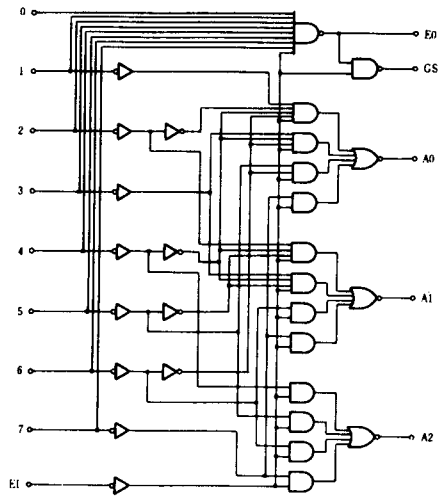
HD74LS148 ●8-line-to-3-line Octal Priority Encoders

The HD74LS148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. The data inputs and outputs are active at the low logic level.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■FUNCTION TABLE

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	×	×	×	×	×	×	×	×	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	×	×	×	×	×	×	×	L	L	L	L	L	H
L	×	×	×	×	×	×	L	H	L	L	H	L	H
L	×	×	×	×	×	L	H	H	L	H	L	L	H
L	×	×	×	×	L	H	H	H	L	H	H	L	H
L	×	×	×	L	H	H	H	H	H	L	L	L	H
L	×	×	L	H	H	H	H	H	H	L	H	L	H
L	×	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H; high level, L; low level, X; irrelevant

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
				$I_{OL}=8mA$	–	–	0.5	
Input current	1~7 Inputs	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	40	μA
	Other inputs				–	–	20	
	1~7 Inputs	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.8	mA
	Other inputs				–	–	−0.4	
	1~7 Inputs	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.2	mA
	Other inputs				–	–	0.1	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current **		I_{CC}	$V_{CC}=5.25V$	Condition 1	–	12	20	mA
				Condition 2	–	10	17	
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

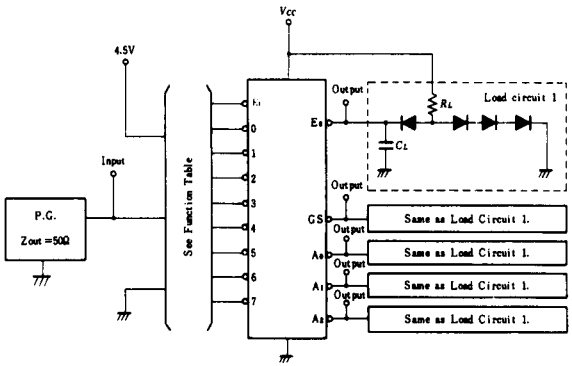
** The condition 1 is measured with inputs 7 and EI grounded, other inputs and outputs open, the condition 2 is measured with all inputs and outputs open.

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

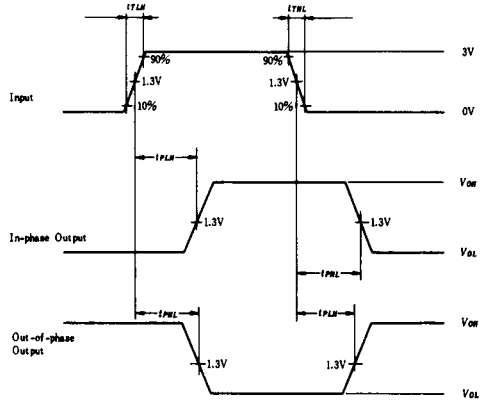
Item	Symbol	Inputs	Outputs	Output Waveforms	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	0~7	A_0, A_1 or A_2	In-phase Output	C_L=15pF, R_L=2kΩ	–	14	18	ns
	t_{PHL}					–	15	25	
	t_{PLH}	0~7	A_0, A_1 or A_2	Out-of-phase Output		–	20	36	ns
	t_{PHL}					–	16	29	
	t_{PLH}	0~7	EO	Out-of-phase Output		–	7	18	ns
	t_{PHL}					–	25	40	
	t_{PLH}	0~7	GS	In-phase Output		–	35	55	ns
	t_{PHL}					–	9	21	
	t_{PLH}	EI	A_0, A_1 or A_2	In-phase Output		–	16	25	ns
	t_{PHL}					–	12	25	
	t_{PLH}	EI	GS	In-phase Output		–	12	17	ns
	t_{PHL}					–	14	36	
	t_{PLH}	EI	EO	In-phase Output		–	12	21	ns
	t_{PHL}					–	23	35	

■TESTING METHOD

1) Test Circuit



Waveform



Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Input pulse; t_{TLH}≦15ns, t_{THL}≦6ns, PRR=1MHz, duty cycle 50%.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

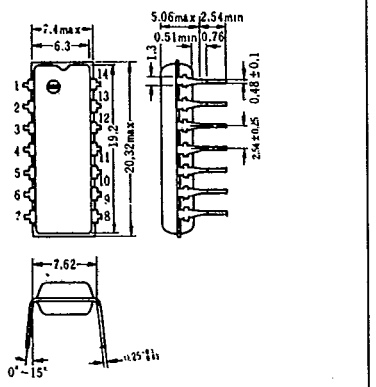
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

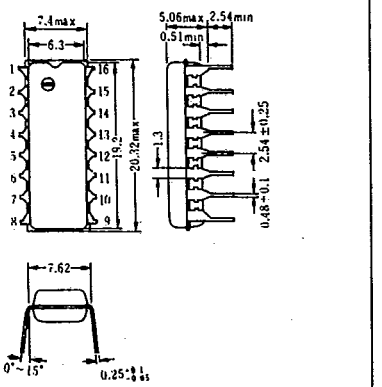
●14 Pin

DP-14



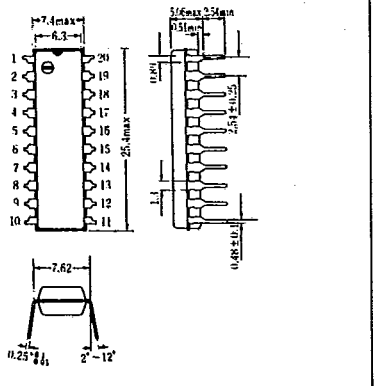
●16 Pin

DP-16



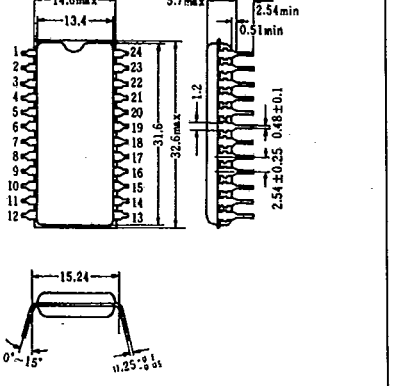
●20 Pin

DP-20



●24 Pin

DP-24

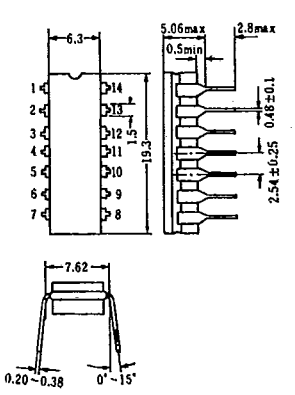


PACKAGING INFORMATIONS

■Cerdip

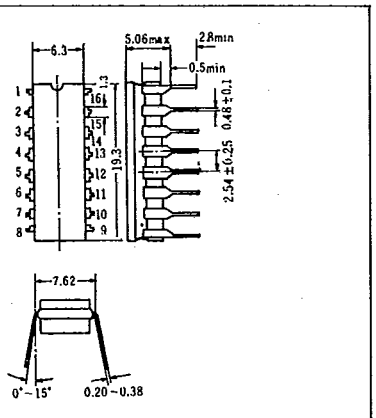
●14 Pin

DG-14



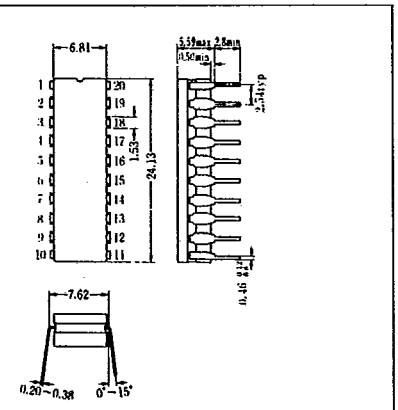
●16 Pin

DG-16



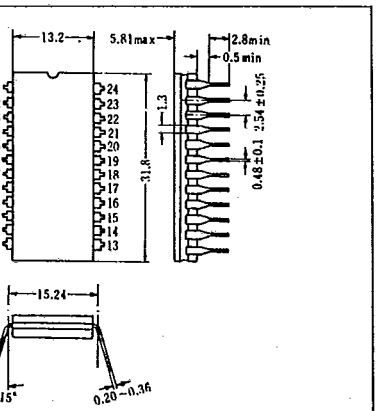
●20 Pin

DG-20



●24 Pin

DG-24



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300