

# UTC7609

# LINEAR INTEGRATED CIRCUIT

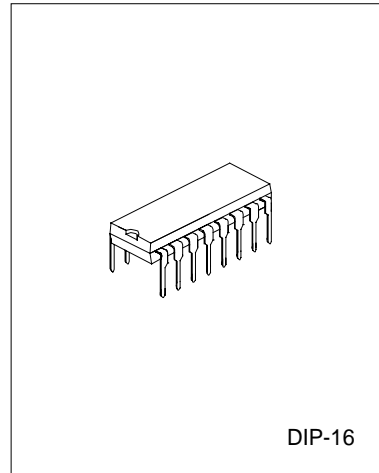
## TV VERTICAL AND HORIZONTAL DEFLECTION CIRCUIT

### DESCRIPTION

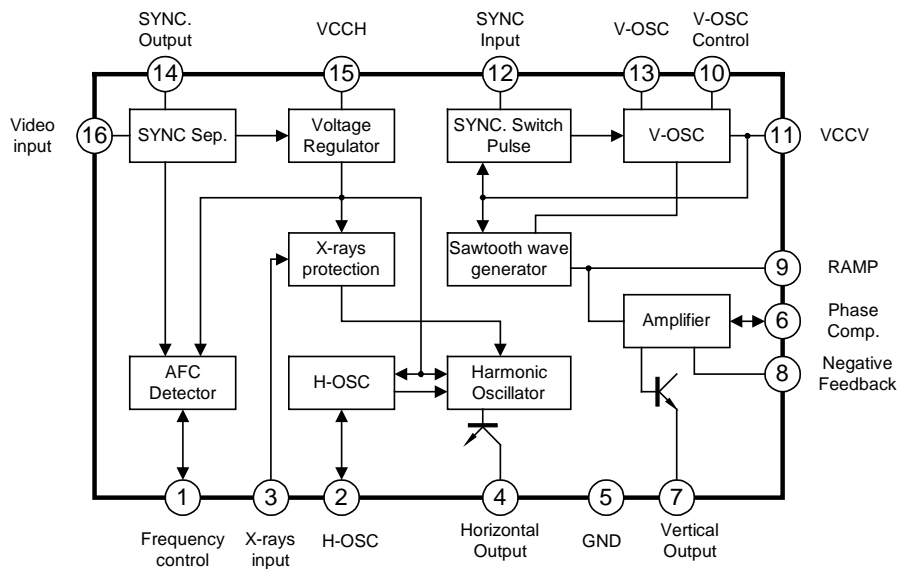
The UTC7609 is a monolithic integrated circuit designed for B.W. and Color TV vertical and horizontal deflection system.

### FEATURES

- \*Excellent temperature stability for the Horizontal Oscillator
- \*Exact 50% Pulse Duty
- \*Excellent Scanning performance



### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**(Ta=25°C)

Characteristic	Symbol	Value	Unit
Horizontal supply current	ICCH	40	mA
Horizontal output current	IOH	60	mA <sub>p-p</sub>
Horizontal output operating current	IOHOP	30	mA <sub>p-p</sub>
Video input voltage	V <sub>IVF</sub>	5	V
AFC input voltage	V <sub>AFC</sub>	8	V <sub>p-p</sub>
Vertical supply voltage	V <sub>CCV</sub>	15	V
Vertical SYNC signal input voltage	V <sub>IS</sub>	5	V <sub>p-p</sub>
Vertical output current	IOV	-5	mA
Operating Temperature	T <sub>opr</sub>	-20 to +70	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C
Power dissipation	P <sub>d</sub>	800	mW

**ELECTRICAL CHARACTERISTICS**

(Ta=25°C, unless otherwise specified)

**STATICS CHARACTERISTICS**

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
<b>Horizontal Section</b>						
Regulator Voltage	V <sub>CCH</sub>	Test Circuit Fig.1	8.9		10.9	V
Supply Current	ICCH	Test Circuit Fig.1	20		30	mA
SYNC High output voltage	VOHS	Test Circuit Fig.3	7.4		9.0	V
SYNC Low output voltage	VOLS	Test Circuit Fig.3			0.5	V
AFC Output Current	I <sub>AFC</sub>	Test Circuit Fig.9	2.15		4.42	mA
AFC Located Voltage	V <sub>CLAFC</sub>	Test Circuit Fig.7	3.9		5.1	V
Minimum Horizontal output voltage	VOHMIN	Test Circuit Fig.8			0.3	V
Supply current	ICCH	Test Circuit Fig.2, V <sub>CCH</sub> =8V	8.4		16	mA
<b>Vertical Section</b>						
Recommended supply voltage	V <sub>CCV</sub>		10.8		13.2	V
Supply current	ICCV	Test Circuit Fig.12	3.4		6.1	mA
Vertical SYNC operating Voltage	V <sub>IS</sub>	Test Circuit Fig.15	0.64		0.80	V
Maximum saw tooth wave output voltage	V <sub>ORAMP</sub>	Test Circuit Fig.17	7.6		8.6	V
Saw tooth wave output current	I <sub>ORAMP</sub>	Test Circuit Fig.18	12.0		35.7	V
Maximum vertical output voltage	V <sub>OV(MAX)</sub>	Test Circuit Fig.19	5.67		7.13	V
Minimum vertical output voltage	V <sub>OV(MIN)</sub>	Test Circuit Fig.20			0.3	V

**DYNAMIC CHARACTERISTICS**

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Horizontal Frequency	f <sub>H</sub>	Test Circuit Fig.6	15125		16125	Hz
Horizontal output Pulse Width	t <sub>WH</sub>	Test Circuit Fig.8	30.01		33.07	μs
SYNC separation sensitivity	I <sub>IVF</sub>	Test Circuit Fig.3		13	56	μA
X-rays protection sensitivity	V <sub>IXP</sub>	Test Circuit Fig.11	0.77	0.91	1.04	V
X-rays protection input impedance	R <sub>IXP</sub>		0.2			MΩ
SYNC SEP. rise time	t <sub>pdR</sub>	Test Circuit Fig.5			100	nS
SYNC SEP. fall time	t <sub>pdF</sub>	Test Circuit Fig.5			100	nS
Horizontal frequency full in range	f <sub>HP</sub>	Test Circuit Fig.10		±600		Hz
		Test Circuit Fig.10		±1000		Hz
Horizontal Osc. Frequency temperature performance	Δf <sub>HT</sub>	Test Circuit Fig.6	0	-100	-350	Hz

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
N.F terminal minimum voltage	V <sub>MIN(N.F)</sub>	Test Circuit Fig.4		2.86	3.7	V
RAMP leak current	I <sub>L(RAMP)</sub>	Test Circuit Fig.21	0.25	0.98	4.5	μA
N.F leak current	I <sub>L(N.F)</sub>	Test Circuit Fig.22	0.18	0.94	6.21	μA
Vertical frequency	f <sub>v</sub>	Test Circuit Fig.13	47	50	54.1	Hz
Vertical frequency pulse width	tw <sub>v</sub>	Test Circuit Fig.14	847	891	933	μS
Vertical frequency full in range	f <sub>vp</sub>	Test Circuit Fig.16		10		Hz
Vertical SYNC input impedance	R <sub>ivs</sub>		400	500	600	Ω

TEST CIRCUIT

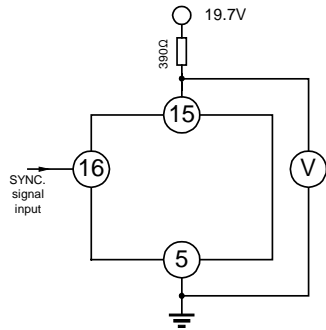


Fig.1

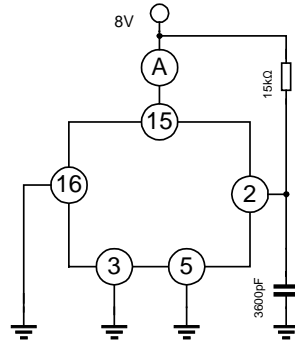


Fig.2

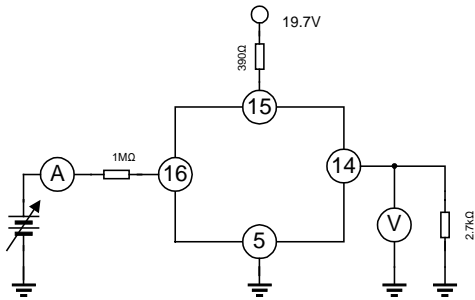


Fig.3

Adjusting the changeable voltage until the pin14 voltage reach to the maximum value, the current of pin 16 is equal to I<sub>lvf</sub>

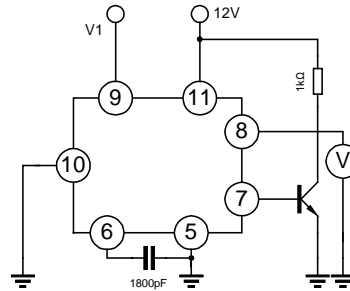


Fig. 4

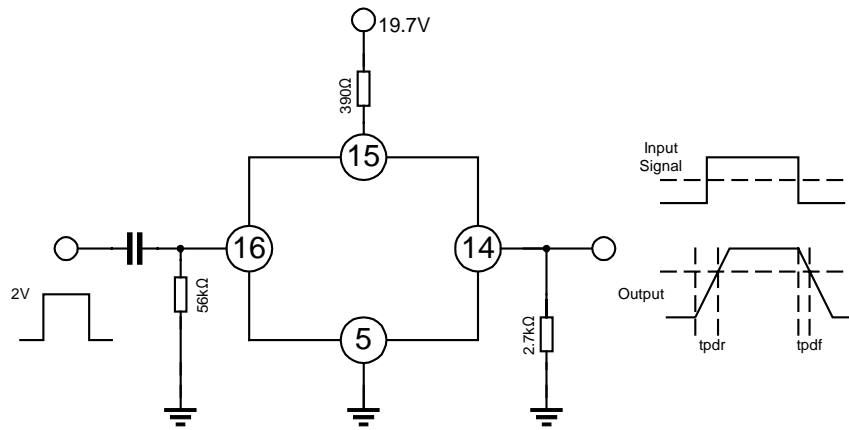


Fig. 5

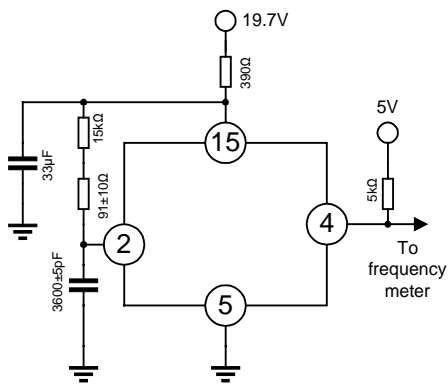


Fig.6

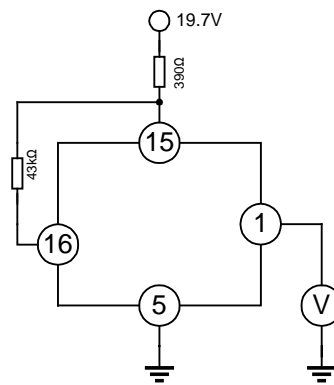


Fig.7

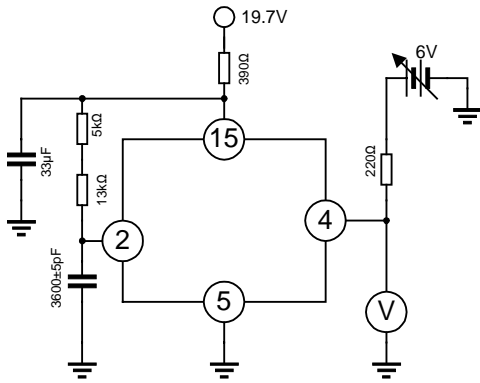


Fig. 8  
Measured at  $f_H=15625\text{Hz}$

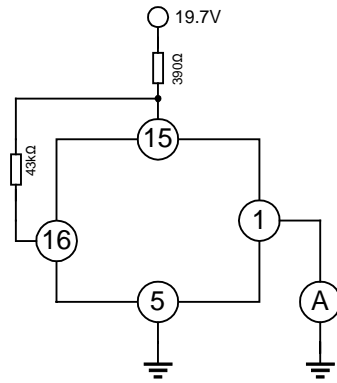


Fig. 9

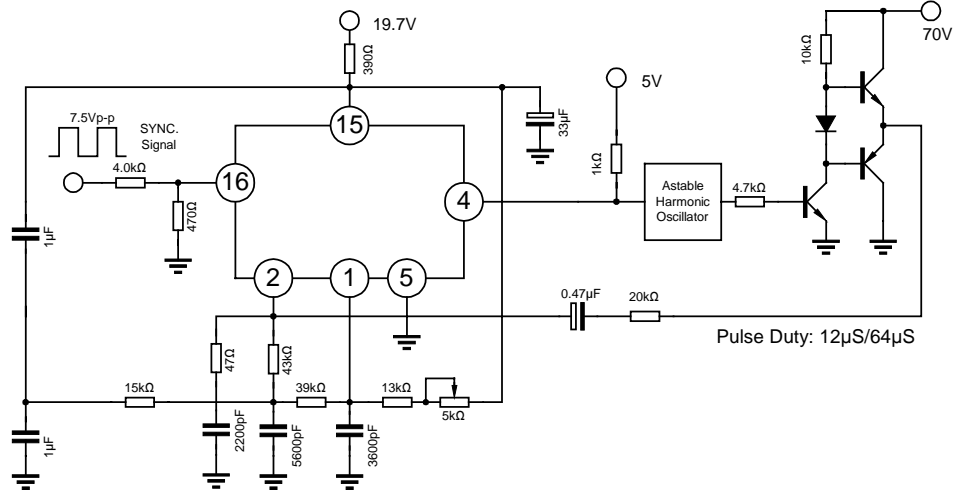


Fig. 10

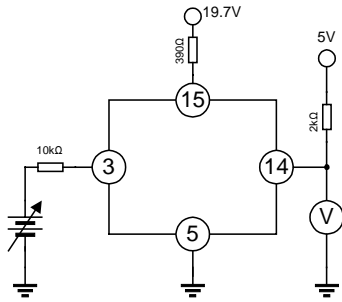


Fig.11

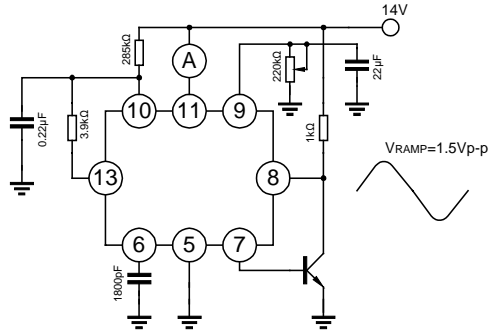


Fig.12

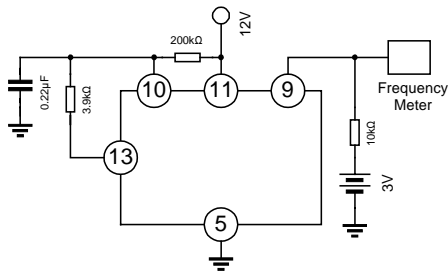


Fig. 13

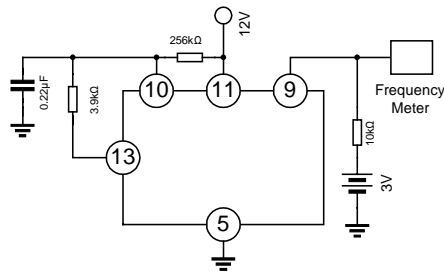


Fig. 14

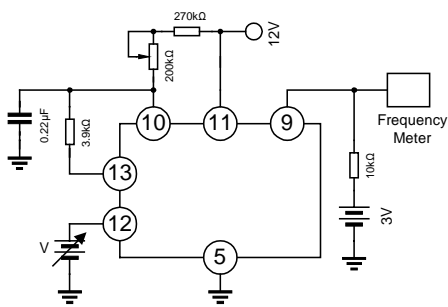


Fig. 15

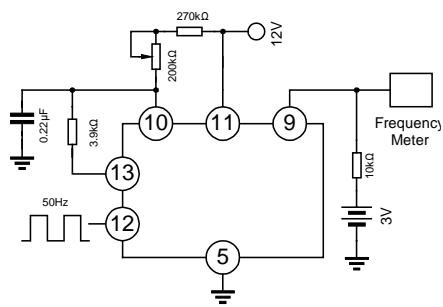


Fig. 16

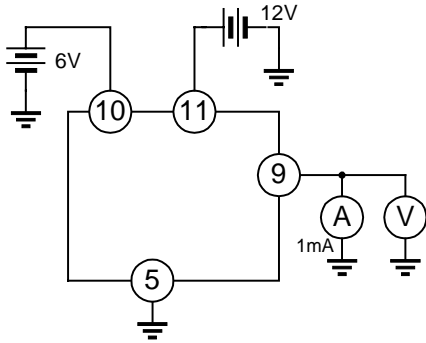


Fig. 17

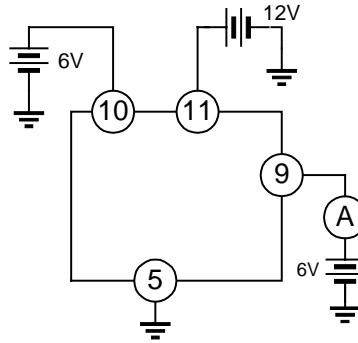


Fig. 18

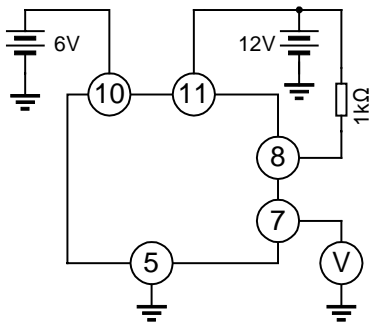


Fig. 19

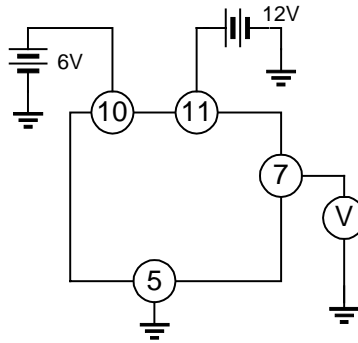


Fig. 20

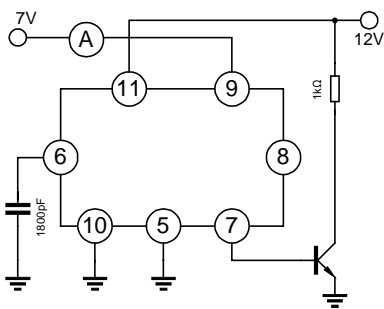


Fig. 21

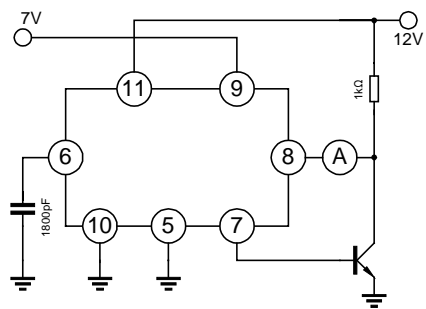


Fig. 22

