

## EPL 20B SERIES

## CMOS ELECTRICALLY PROGRAMMABLE LOGIC

### ■ GENERAL DESCRIPTION

RICOH EPL 20B Series are Field-programmable logic arrays by CMOS EPROM process technology.

Two product groups make up the EPL 20B Series family.

Group I consists of AND-FIXED OR, XOR Arrays. (EPL 10P8, 12P6, 14P4, 16P2)

Group II consists of AND-FIXED OR, XOR Array, (EPL 16P8) and three Registered AND-FIXED OR, XOR Arrays. (EPL 16RP8, 16RP6, 16RP4)

EPL 20B Series allows users to program easily by programming EPROM Memory Cell, available in both plastic packages for one-shot and reprogrammable Cerdip window packages.

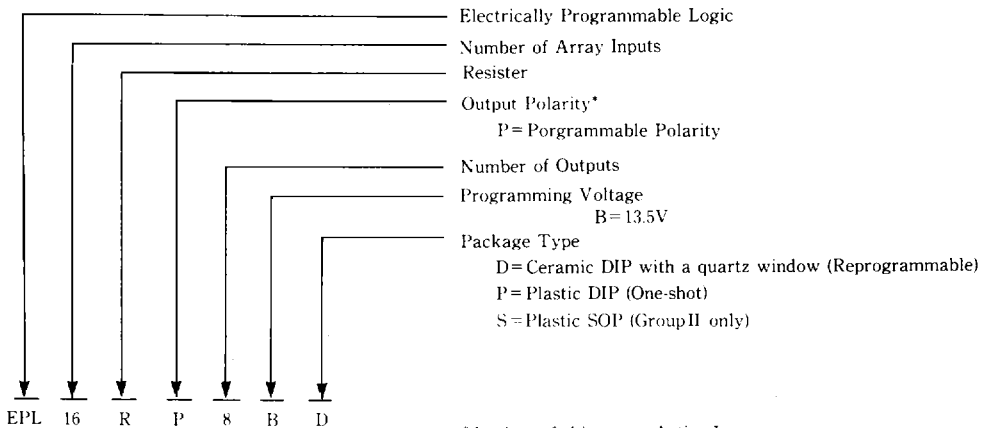
Therefore, it is possible to shorten the development term and check and correct the circuits easily.

### ■ FEATURES

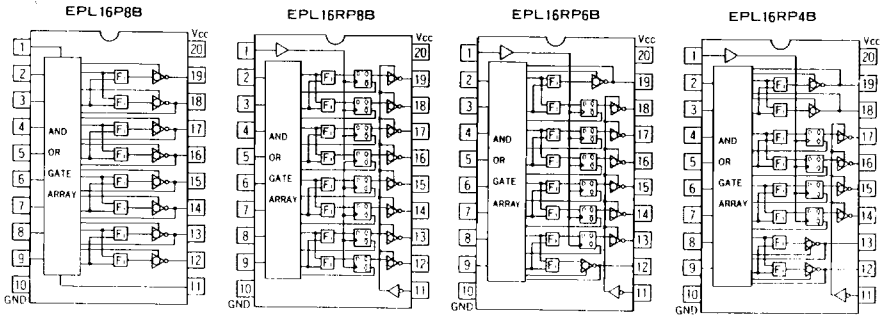
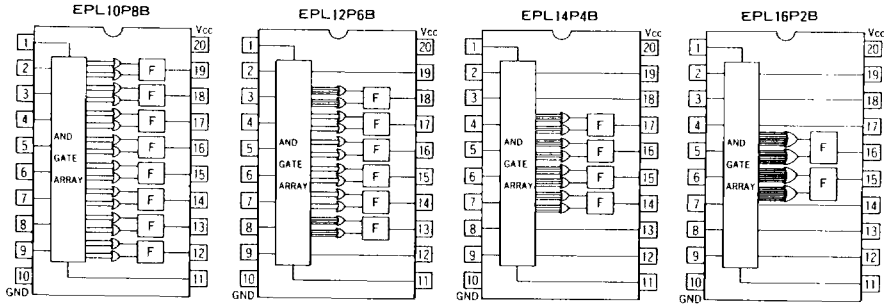
- CMOS process technology ensures the low power consumption, and higher reliability
- Available in both plastic and Cerdip window packages
- Data copying protection
- Flexibility of logic structure
- Package Type
  - 20-pin 300mil Plastic DIP
  - 20-pin 300mil Ceramic DIP with a window
  - 20-pin 300mil SOP (Group II only)
- Product Term : 32 line (Group I)  
: 64 line (Group II)
- Propagation Delay Time  
: 35ns (MAX)
- Each pin has Programmable Polarity
- Up-ward compatibility with MMI PAL

### EPL 20B Series FAMILY

PART NUMBER		CONFIGURATION
GROUP I	EPL 10P8 B	10-INPUT, 8-OUTPUT, AND-OR/XOR ARRAY
	EPL 12P6 B	12-INPUT, 6-OUTPUT, AND-OR/XOR ARRAY
	EPL 14P4 B	14-INPUT, 4-OUTPUT, AND-OR/XOR ARRAY
	EPL 16P2 B	16-INPUT, 2-OUTPUT, AND-OR/XOR ARRAY
GROUP II	EPL 16P8 B	10-INPUT, 6-INPUT/OUTPUT, 2-OUTPUT, AND-OR/XOR ARRAY
	EPL 16RP8 B	8-INPUT, 8-FEEDBACK, 8-OUTPUT, 8-REGISTERED, AND-OR/XOR ARRAY
	EPL 16RP6 B	8-INPUT, 6-FEEDBACK, 2-INPUT/OUTPUT, 8-OUTPUT, 6- REGISTERED, AND-OR/XOR ARRAY
	EPL 16RP4 B	8-INPUT, 4-FEEDBACK, 4-INPUT/OUTPUT, 8-OUTPUT, 4- REGISTERED AND-OR/XOR ARRAY



\*At time of shipment : Active-Low



(Note) F : FEATURE Cell (OR, XOR, POLARITY)  
 F2 : FEATURE2 Cell (POLARITY)  
 F1 : FEATURE1 Cell (OR, XOR)

### ■ Electrical Specifications Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V <sub>cc</sub>	V <sub>cc</sub> supply voltage	With respect to GND	-0.3~ 7.0	V
V <sub>pp</sub>	V <sub>pp</sub> supply voltage		-0.3~14.5	V
V <sub>i</sub>	Input voltage		-0.3~V <sub>cc</sub> +0.3	V
V <sub>o</sub>	Output voltage		-0.3~V <sub>cc</sub> +0.3	V
P <sub>d</sub>	Maximum power consumption	T <sub>a</sub> = 25°C	700	mW
T <sub>opr</sub>	Ambient operating temperature		0~70	°C
T <sub>stg</sub>	Storage temperature		-40~125	°C

### ■ Capacitance

Symbol	Parameter		Condition	Value			Unit
				Min	Typ.	Max	
C <sub>IN</sub>	Input capacitance	2 ~ 9, 11 pin	V <sub>IN</sub> = 0V to V <sub>cc</sub>			6	pF
		1 pin				20	pF
C <sub>OUT</sub>	Output capacitance (12 ~ 19 pin)		V <sub>OUT</sub> = 0V, f = 1MHz			12	pF

### D.C.Characteristics (T<sub>a</sub> = 0 to 70°C, V<sub>cc</sub> = 5V ± 5%)

Symbol	Parameter		Condition	Value			Unit
				Min	Typ.	Max	
I <sub>LI</sub>	Input current leakage		V <sub>IN</sub> = 0V to V <sub>cc</sub>	-20		20	μA
V <sub>IL</sub>	"L" input voltage			-0.3		0.8	V
V <sub>IH</sub>	"H" input voltage			2.0		V <sub>cc</sub> +0.3	V
V <sub>OL</sub>	"L" output voltage		V <sub>cc</sub> = Min, I <sub>OL</sub> = 8mA		0.3	0.5	V
V <sub>OIH</sub>	"H" output voltage		V <sub>cc</sub> = Min, I <sub>OH</sub> = -3.2mA	2.4	4.4		V
I <sub>LO</sub>	Output current leakage in OFF status	Group II	V <sub>o</sub> = 0V to V <sub>cc</sub>	-20		20	μA
I <sub>cc1</sub>		Source current (Stationary status)	Group I	V <sub>cc</sub> = Max, Output = open V <sub>i</sub> = GND or V <sub>cc</sub>			40
	V <sub>cc</sub> = Max, Output = open V = 2.4V					50	mA
	Group II		V <sub>cc</sub> = Max, Output = open V <sub>i</sub> = GND or V <sub>cc</sub>			60	mA
I <sub>cc2</sub>	Source current (Operating status)	Group I	V <sub>cc</sub> = Max, Output = open			50	mA
		Group II	f = 10MHz, V <sub>i</sub> = 0.8V or 2.4V			70	mA

Note 1. Group I is equipped with a power-down circuit. When neither "OR" nor "XOR" in the FEATURE cell is used, current for the unused product term is cut off.

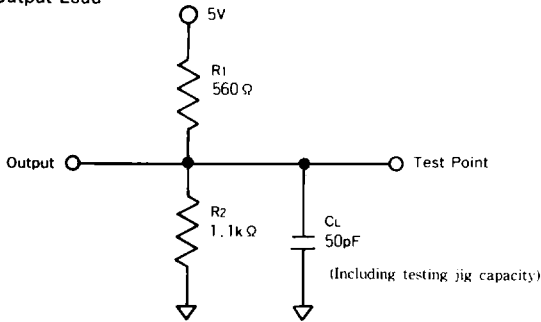
2. Group I has two times as many product terms as PAL<sup>TM</sup>, therefore, Power consumption is reduced to approximately half value when the user replace PAL<sup>TM</sup> with Group I.

(Above mentioned specifications are in the condition of use all product terms.)

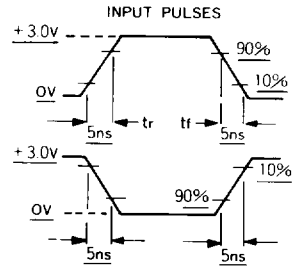
A.C.Characteristics (Ta=0 to 70°C, VCC=5V±5%)

Symbol	Item		Condition	Typical			Unit
				Min	Std	Max	
t <sub>PD</sub>	Propa- gation Delay Time	Input or feedback to output	R <sub>1</sub> = 560Ω R <sub>2</sub> = 1.1kΩ C <sub>L</sub> = 50pF		25	35	ns
t <sub>CLK</sub>		Clock to output or feedback			15	25	ns
t <sub>PZX</sub>		Pin11 to output enable			15	25	ns
t <sub>PXZ</sub>		Pin11 to output disable			15	25	ns
t <sub>PIZ</sub>		Input to output enable			25	35	ns
t <sub>PIX</sub>	Input to output disable			25	35	ns	
f <sub>MAX</sub>	Maximum frequency				20		MHz
t <sub>WL</sub>	Minimum clock time width	Low			20		ns
t <sub>WH</sub>		High			20		ns
t <sub>SU</sub>	Input set-up time				25		ns
t <sub>H</sub>	Input hold time			0		ns	

Output Load

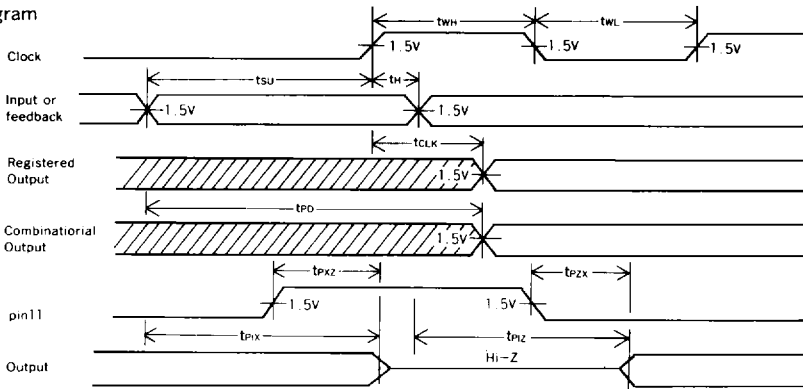


Input Waveform



NOTE : This is the A.C. characteristic measurement with a voltage of 1.5V on both the input and output.

Timing Diagram



Note : Data unknown

■ Configurations of EPL Logic

RICOH EPL 20B Series Group I provides 32 input terms and 32 product terms.

RICOH EPL 20B Series Group II provides 32 input terms and 64 product terms.

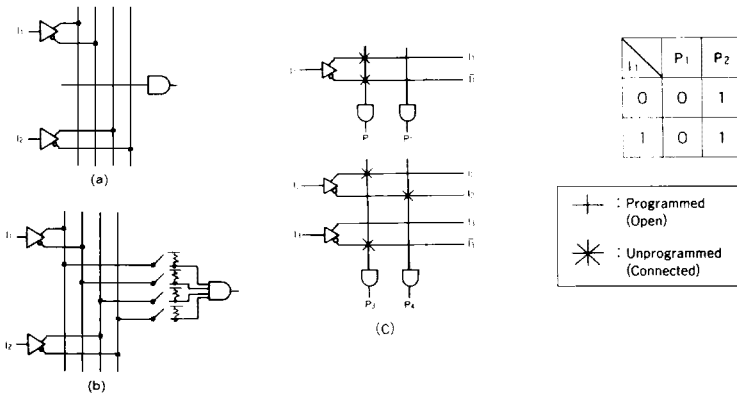
Input pins in both groups are activated for regular logical operation at a TTL level.

All intersection points of the input terms and product terms are provided with an EPROM cell connection. These intersections are connected prior to delivery.

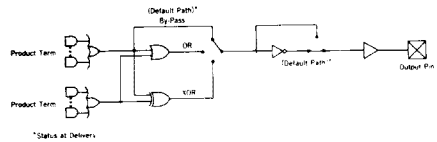
The AND gate are illustrated in logic diagram (a) below. The switches indicated in logic diagram (b) correspond to the EPROM cell connections. All switches are closed when the devices are unprogrammed.

As illustrated in logic diagram (c), when neither positive input (1) nor negative input (T) is programmed, the AND output (P1) becomes "inactive".

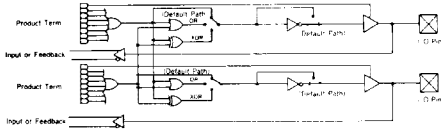
When both positive input (1) and negative input (T) are programmed, the AND output (P2) becomes "don't care" logically. Each output includes a FEATURE cell in addition to the programmable AND-FIXED OR logic. The FEATURE cell enables the user to program the logic polarity (active-high/active low) and the logical OR, Exclusive-OR case.



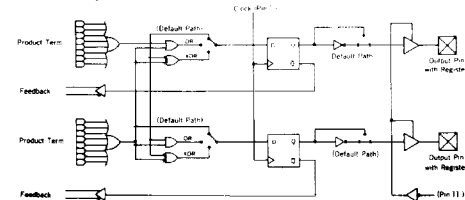
Group I Block Diagram



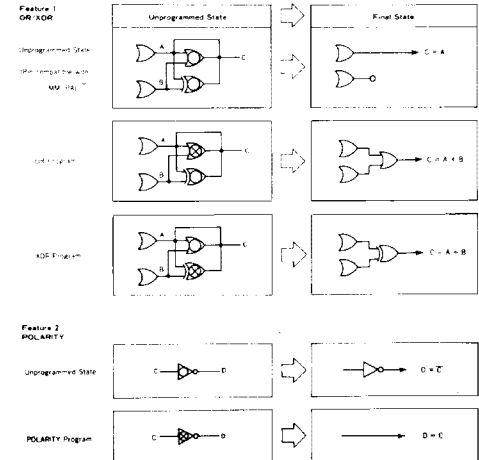
Group II I/O Block Diagram



Group II Registered Block Diagram

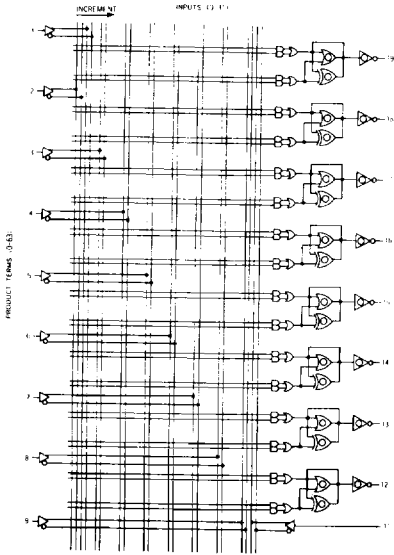


FEATURE CELL



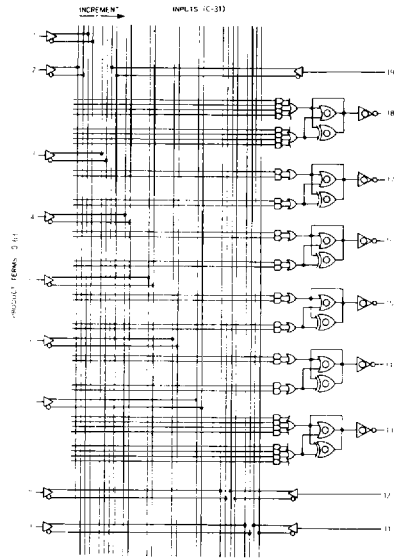
Logic Diagram

EPL10P8B



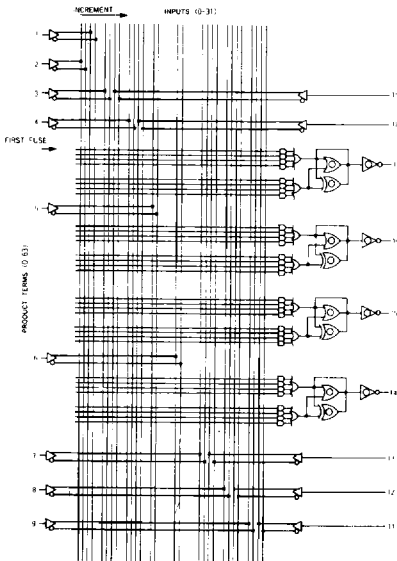
Logic Diagram

EPL12P6B



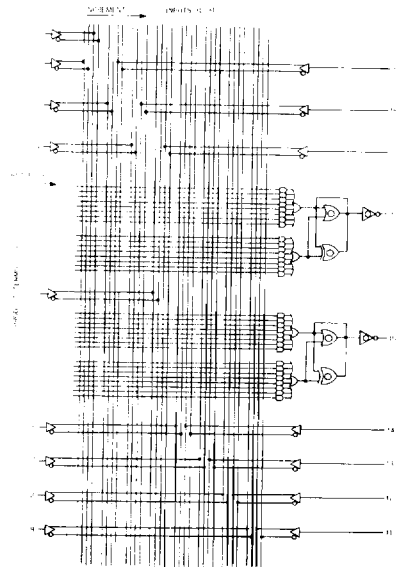
Logic Diagram

EPL14P4B



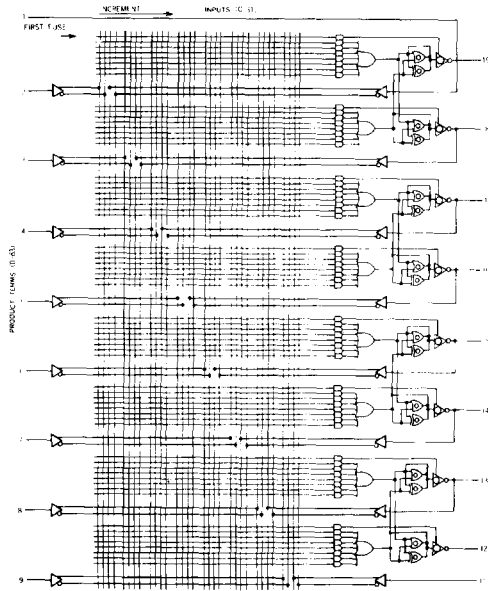
Logic Diagram

EPL16P2B



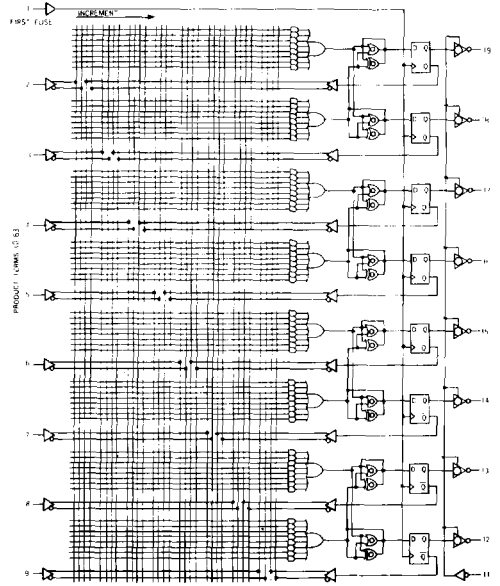
Logic Diagram

EPL16P8B



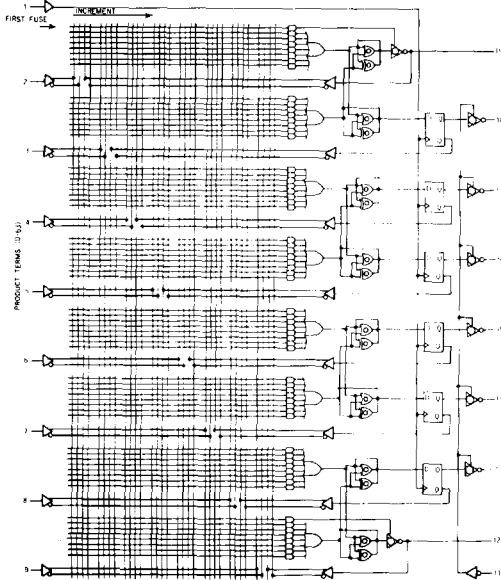
Logic Diagram

EPL16RP8B



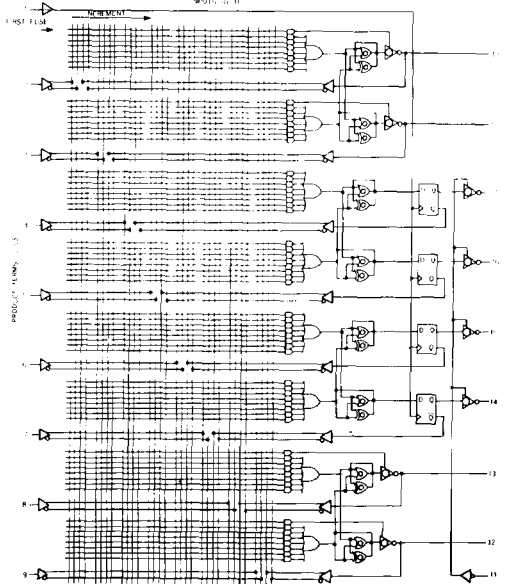
Logic Diagram

EPL16RP6B



Logic Diagram

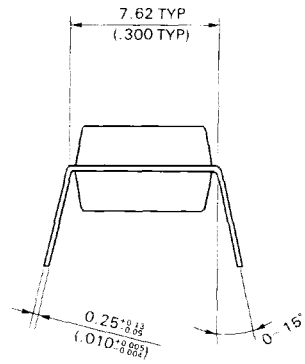
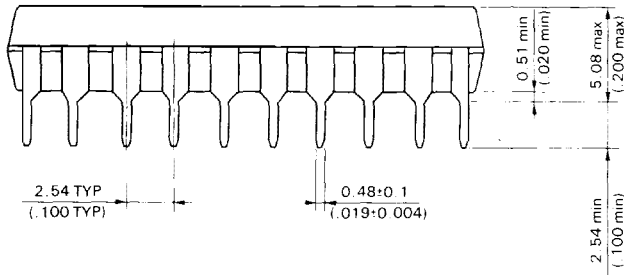
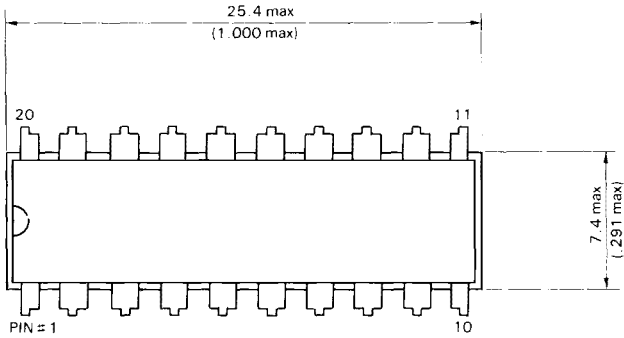
EPL16RP4B



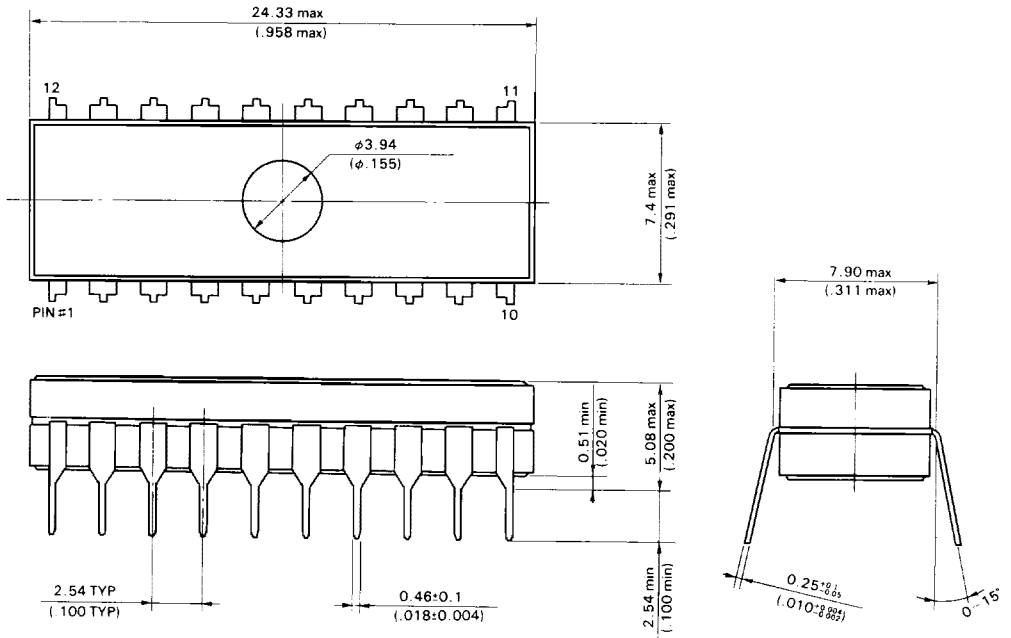
# CMOS EPL 20B

## ■ Package Dimension (unit mm/inch)

- 20 Pin 300 mil Plastic DIP



●20 Pin 300 mil Ceramic (with window)



# CMOS EPL 20B

●20 Pin 300mil SOP (Group II only)

