SP8740 300MHz ÷ 5/6
SP8741 300MHz ÷ 6/7

The SP8740 and SP8741 are ECL counters with ECL 10K compatible output. The SP8740/SP8741 divide by 5 and 6 respectively when either control input is in the high state and by 6 and 7 respectively when both inputs are in the low state (or open circuit). An AC coupled input of 600mV is required.

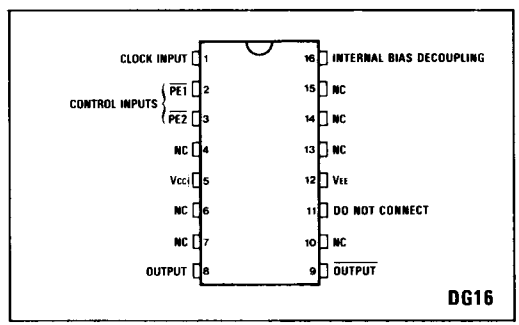


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8740 A DG
SP8740 B DG
SP8740 AB DG
SP8740 AC DG
SP8741 A DG
SP8741 B DG
SP8741 AB DG
SP8741 AC DG

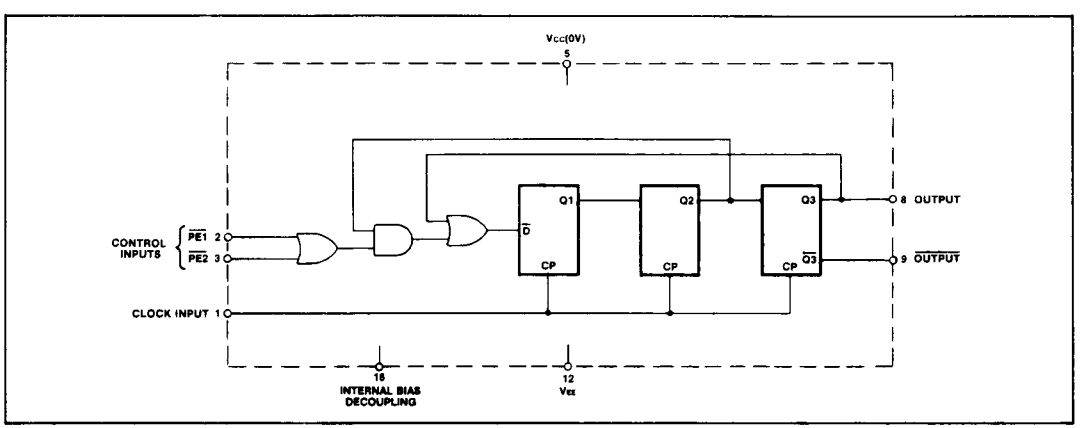


Fig.2 Functional diagram (SP8740)

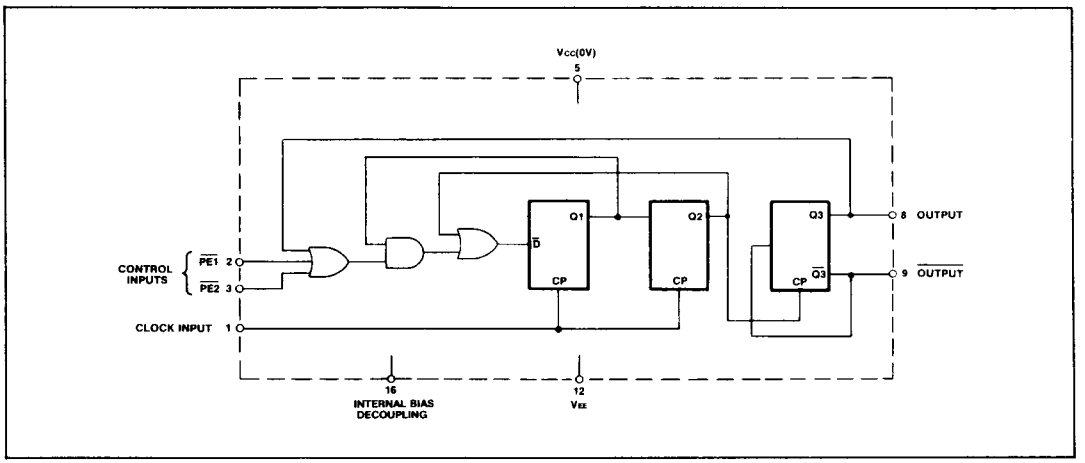


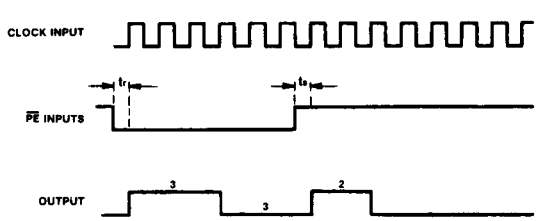
Fig.3 Functional diagram (SP8741)

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		60	mA		Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE}=-5.2V(25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE}=-5.2V(25°C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE}=-5.2V(25°C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE}=-5.2V(25°C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

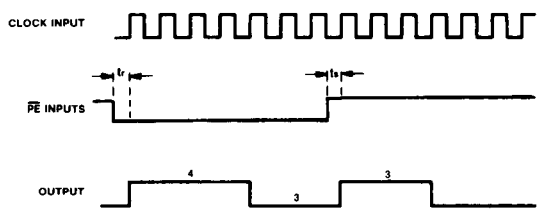
NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over the full specified supply, frequency and temperature range of both SP8740 and SP8741.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and V_{IN} = +1.22mV/°C but these are not tested.
3. SP8740/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Fig.4 Timing diagram SP8740

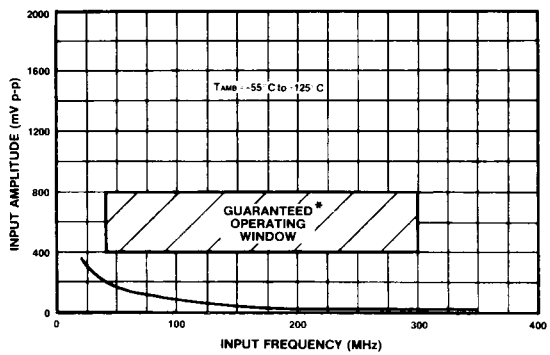


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Fig.5 Timing diagram SP8741

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷5 or 6 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷6 or 7 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.6 Typical input characteristics SP8740/1A

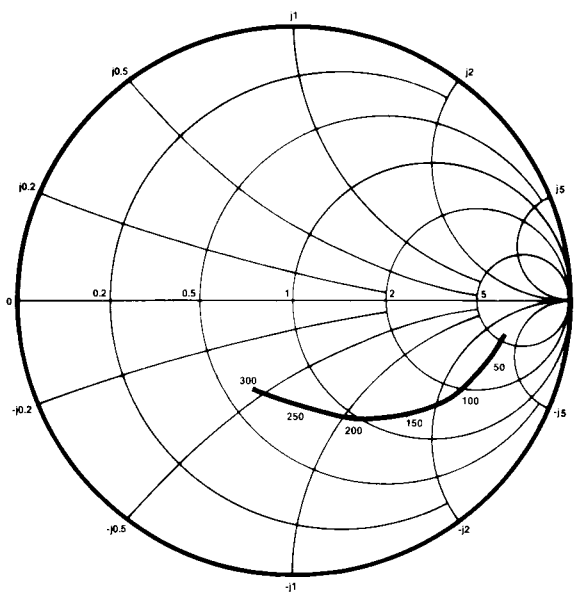


Fig.7 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/us.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 9. There is an internal circuit equivalent to a load of 2k pulldown resistor at load output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8740/1 varies as a function of frequency. See Fig. 7.
7. The SP8740 is not suitable for use in a fixed divide by 6 mode.

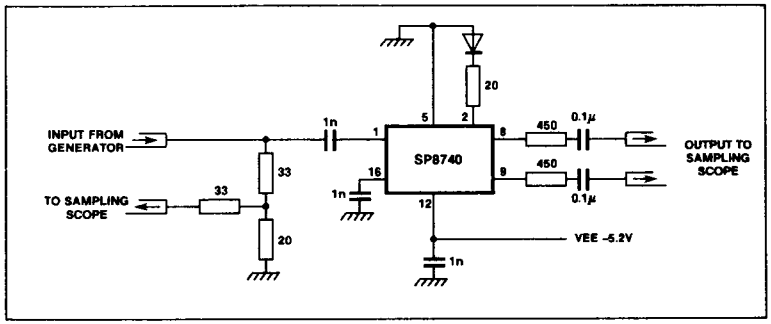


Fig. 8 Test circuit

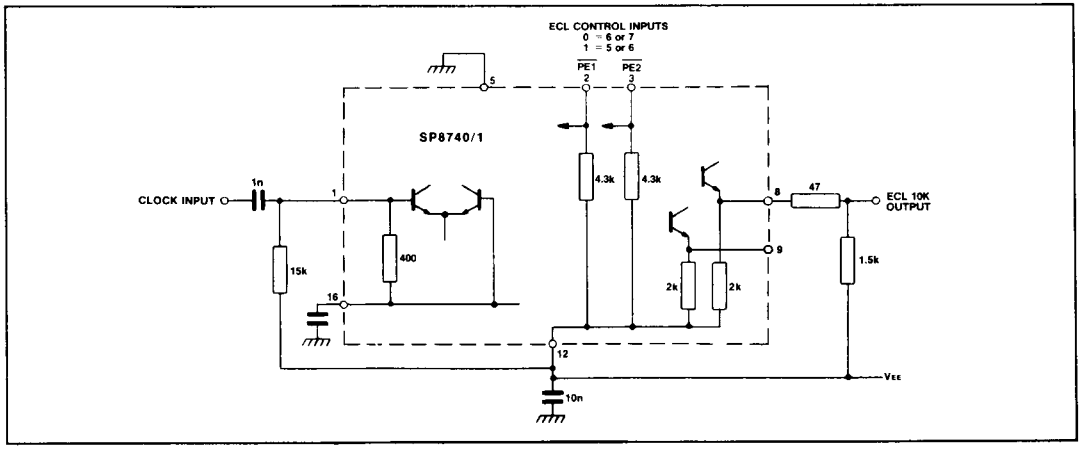


Fig.9 Typical applications circuit showing interfacing