TC74ACT32
Quad 2-Input OR Gate

Features:

- **High Speed:** t_{pd} = 4.5ns (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 4μA (max.) at Ta = 25°C
- **Compatible with TTL Outputs:** V_{IL} = 0.8V (max.) V_{IH} = 2.0V (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Pin and Function Compatible with 74F32**
- **Available in 14-pin DIP and 150 mil SOIC**

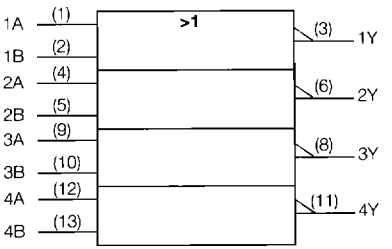
The TC74ACT32 is an advanced high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to high speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

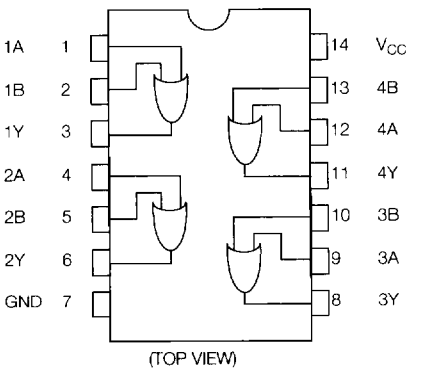
IEC Logic Symbol



Truth Table

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

Pin Assignment



(TOP VIEW)

Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500 (DIP) */180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40~85°C Min.	Ta = -40~85°C Max.	UNIT
High-Level Input Voltage	V_{IH}	—		4.5~5.5	2.0	—	—	2.0	—	V
				4.5~5.5	2.0	—	—	2.0	—	
				4.5~5.5	2.0	—	—	2.0	—	
Low-Level Input Voltage	V_{IL}	—		4.5~5.5	—	—	0.8	—	0.8	V
				4.5~5.5	—	—	0.8	—	0.8	
				4.5~5.5	—	—	0.8	—	0.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	ΔI_{CC}	Per Input: V_{IN} = 3.4V Other Input: V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC Electrical Characteristics (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time	t_{pLH} t_{pHL}	—	5.0±0.5	—	5.2	7.9	1.0	9.0	ns
			5.0±0.5	—	5.2	7.9	1.0	9.0	
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} [1]	—	—	—	22	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\,(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per Gate).