

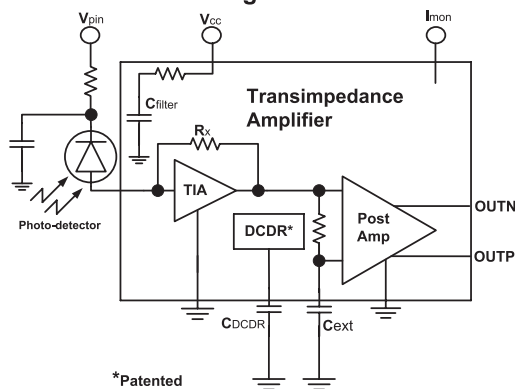
Product Description

RFMD's SFT-9200B is a high performance heterojunction bipolar transistor transimpedance amplifier designed for 43Gb/s SONET/SDH, 40GbE, and 100GbE amplitude, phase, and polarization modulation applications. The SFT-9200B uses high performance Indium Phosphide (InP) device technology that delivers high transimpedance, large dynamic range, and a typical 50GHz 3dB bandwidth. Performance is enhanced through the use of a patented circuit topology that reduces duty cycle distortion under high photocurrent conditions and allows high transimpedance with low DC power to be realized. The SFT-9200B is supplied in bare die form and includes a current monitor feature that can be used for fiber alignment or loss of signal (LOS) detection.

Optimum Technology Matching® Applied

- GaAs HBT
- GaAs MESFET
- InGaP HBT
- SiGe BiCMOS
- Si BiCMOS
- SiGe HBT
- GaAs pHEMT
- Si CMOS
- Si BJT
- GaN HEMT
- InP HBT
- RF MEMS
- LDMOS

Functional Block Diagram



Features

- Low Noise InP HBT Technology
- 1600Ω Diff. Transimpedance
- Supports 43Gb/s Data Rates
- 50GHz Transimpedance Bandwidth
- Low Power Consumption, 200mW
- Linear Current Monitor Output (IMON)
- Die Size 1.0mmx1.0mm

Applications

- OC-768 40Gbps RZ-DPSK Optical Receivers
- 40GbE/40Gbps Optical Receivers
- 100GbE Optical Receivers
- 40, 100, and 160Gbps Transponders
- Test Equipment
- Instrumentation

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					
Differential Transimpedance		1600		Ω	C _{PD} = 50fF, R _D = 15Ω
Transimpedance Bandwidth (3dB)		50		GHz	C _{PAR} = 15fF, L _{INT} = 0.15nH
Gain		24		dB	Single-ended, 50Ω In/Out
Gain Ripple		1.0		dB	Single-ended, 50Ω In/Out
S21 3dB Bandwidth		50		GHz	Single-ended, 50Ω In/Out
Group Delay Deviation		10		ps p-p	Single-ended, 50Ω In/Out, 30kHz - F _C
Optical Sensitivity		-13 ⁽²⁾		dBm	Assuming 0.9A/W responsivity, measured at 10 ⁻¹² BER with 2 ³¹ -1
Optical Overload	2.7	3.2		mA _{p-p}	Assuming 0.9A/W responsivity, measured at 10 ⁻¹² BER with PRBS 2 ³¹ -1
Input Equivalent Noise Current Density		20 ⁽¹⁾		pA/sqrt (Hz)	F = 43GHz
Maximum Output Voltage Swing	250	400	500	mV _{p-p}	Single-ended, 50Ω In/Out
Input DC Voltage		0.8		V	
Output DC Voltage		3.05		V	50Ω termination to V _{CC}
Output Return Loss		-12		dB	Single-ended, 50Ω In/Out
Supply Voltage	3.15	3.30	3.45	V	
Supply Current		58	65	mA	V _{CC1} = 3.3V, V _{CC2} = 3.3V, total current
Power Dissipation		191	228	mW	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Current (I_{CC})	65	mA
Device Voltage (V_{CC})	3.5	V
Voltage Difference ($V_{CC1} - V_{CC2}$)	0.3	V
Max DC Input Current	5.0	mA
Operating Temperature (T_{OP})	0 to +85	°C
Storage Temperature Range	-40 to +150	°C
Operating Junction Temperature (T_J)	+125	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

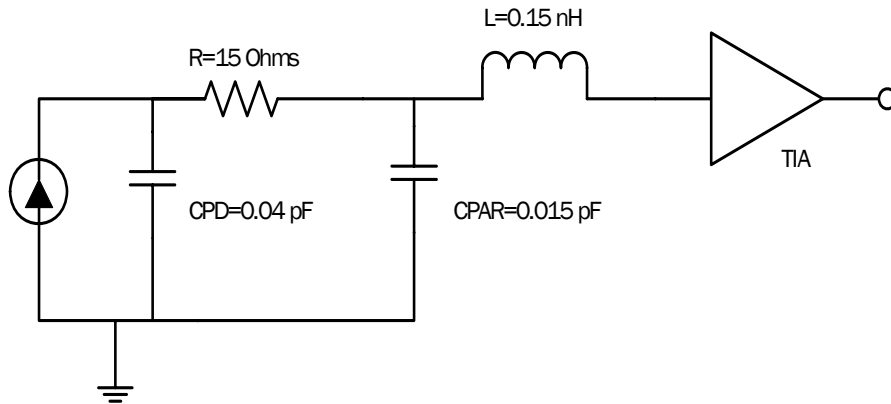
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications, cont.					
Photodiode Current Monitor		Yes			
Dynamic Range Adjust		Yes			

Notes:

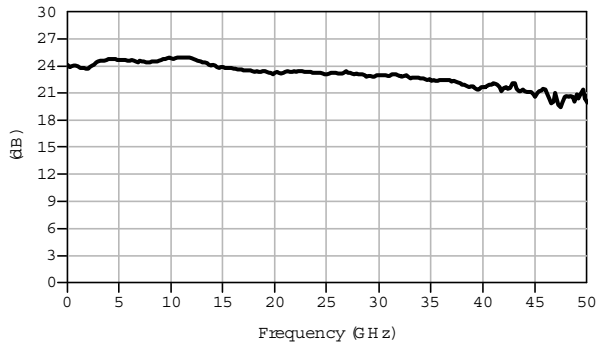
1. Measured value.
2. Calculated from input noise current density.

Model Used For Transimpedance Calculation

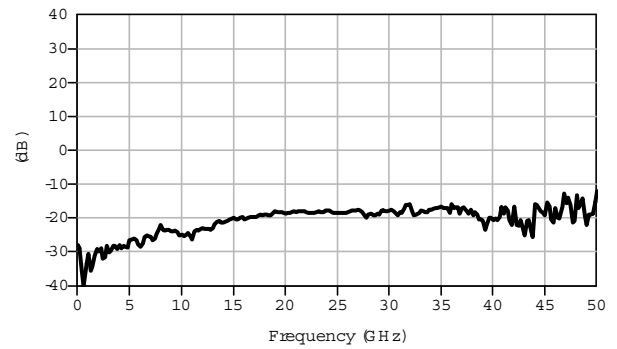


Typical Electrical Performance

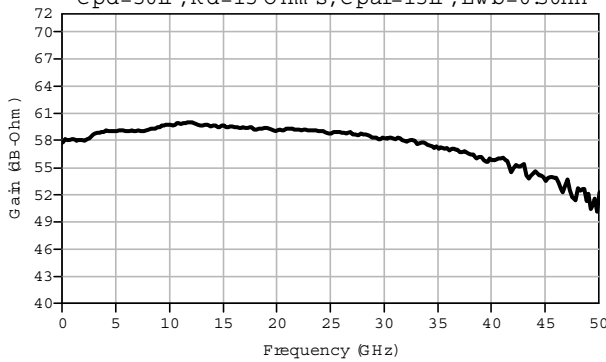
S21 (m easured on wafer)



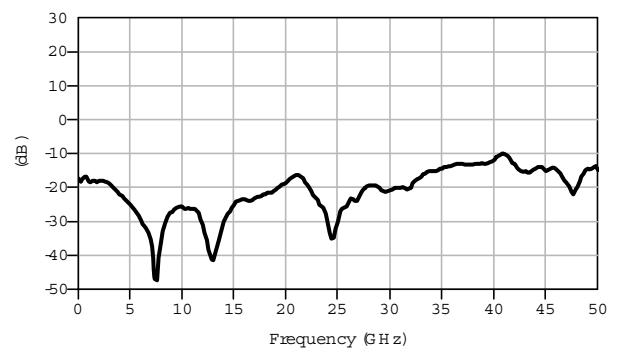
S11 (m easured on wafer)



Transim pedance Gain
Cpd=50fF, Rd=15 Ohm s, Cpar=15fF, Lwb=0.30nH

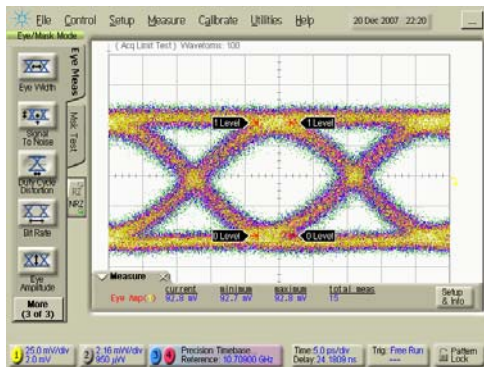


S22 (m easured on wafer)



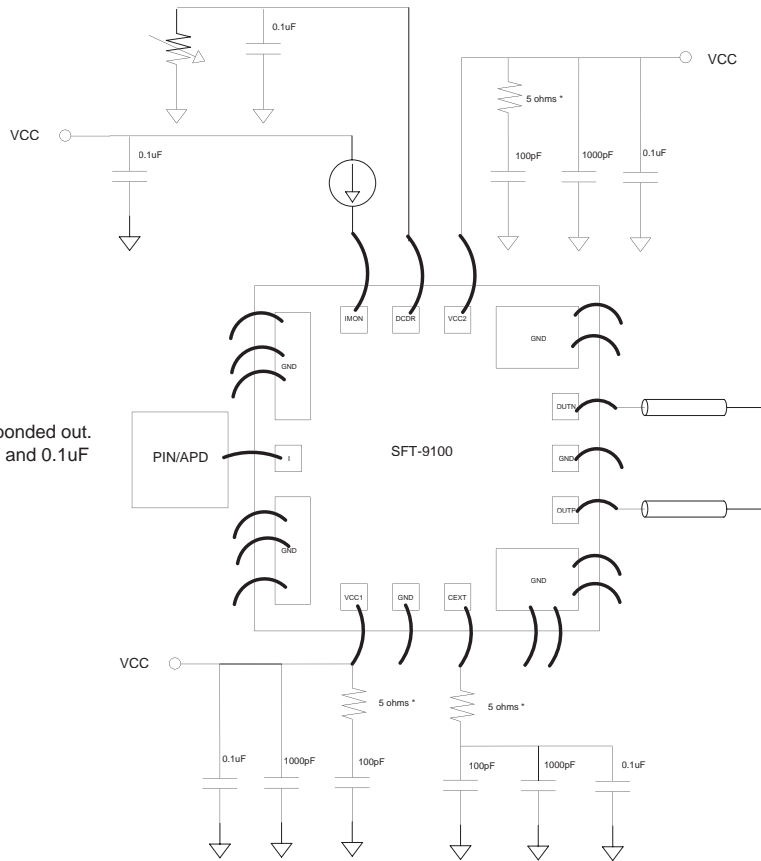
Note: All electrical measurements performed using diode probe station.

Optical Measurement Performance



Typical 43Gb/s Optical Eye Diagram, -10dBm Input
Optical measurements courtesy of Archcom Technology Inc. USA.

Application Circuit



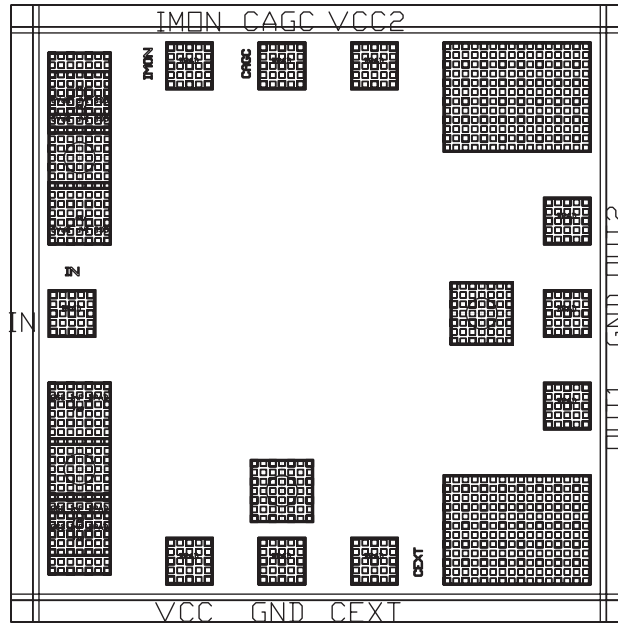
Notes:

1. 3mil ribbon is recommended
2. CPW structure is required for RF outputs
3. GND pad between OUTN/OUTP is required to be bonded out.
4. VCC1 and VCC2 should be bypassed with 1000pF and 0.1uF capacitors.
5. 5 ohm resistors are optional but recommended.

Pad Description Table

Pad Number	Size	Pad Center	
		X Coordinate	Y Coordinate
GND	100umx310um	111	232
IN	75umx75um	98.5	500
GND	100umx310um	111	767
IMON	75umx75um	289	901
CAGC	75umx75um	439	901
VCC2	75umx75um	589	901
GND	237umx176um	820	850
OUT2	75umx75um	901	650
GND	75umx75um	901	500
OUT1	75umx75um	901	350
GND	237umx176um	820	149
CEXT	75umx75um	589	98
GND	75umx75um	439	98

Pad Outline Drawing



Description of External Connections and How They Operate

V_{CC1}/V_{CC2} :

Separate power supply connections are required for the input and output stages of the TIA. Each supply should be bypassed separately with decoupling capacitors. A parallel network of 100pF, 1000pF, and 0.1uF is recommended. V_{CC1} and V_{CC2} should be powered up together and should not differ by more than 0.3V.

I_{mon} :

When tied to the supply voltage through an ammeter, the current through the ammeter “ I_{mon} ” reflects the average photo diode current. The I_{mon} current will be approximately the value of the average photo diode current and will be directly proportional to this quantity. I_{mon} can be used for loss of signal detection or photodiode/fiber alignment in manufacturing. A third function this monitor can provide is the manual adjustment of the DCDR threshold. With no input photocurrent applied to the TIA, the I_{mon} will give a finite quiescent current (uA). The finite current indicates that the automatic circuit has already started to turn on. By employing a shunt resistor (1K-50K) on the DCDR port to ground, this threshold can be reduced (current can be reduced to a few uA) setting the automatic circuit for maximum sensitivity and dynamic range. If I_{MON} is not used, this port can be left unconnected.

DCDR (Duty Cycle Distortion Reduction):

This patented feature compensates for the duty cycle distortion as a result of high input current seen by the amplifier. As the optical input power and induced photo current is increased, an automatic circuit is invoked to prevent distorted operation in the transistors of the TIA. The threshold input current where the circuit turns on can be adjusted by employing a shunt resistor to ground at the DCDR pin. The value of the shunt resistor can be set between 1K and 50K. The lower the value, the higher the input current threshold in which the circuit turns on. In order to optimize for maximum sensitivity and dynamic range, the I_{mon} current can be monitored while tuning this shunt resistor. Optimum sensitivity and dynamic range can be obtained by tuning the resistor value until only a few uA of I_{mon} current is observed when there is no optical input power applied.

C_{DCDR} :

An off chip capacitor is required in order to integrate and produce the automatic circuit control voltage.

C_{EXT} :

An off chip capacitor sets the lower frequency of operation for the amplifier. For 30kHz operation and below, a 0.1uF capacitor is required. Wirebond length is critical and should be minimized.

C_{VCC} :

An off chip bypass capacitor is required. Wirebond length is critical and should be minimized.

Ordering Information

Part Number	Description	Delivery Method	Die/Gel Pak
SFT-9200B-D	55GHz TIA, 1mmx1mm DIE	GelPak	1 to 4
SFT-9200B-DSB	Sample Bag, 55GHz TIA, 1mmx1mm DIE	GelPak	5
SFT-9200B-DSR	Sample Reel, 55GHz TIA, 1mmx1mm DIE	GelPak	100
SFT-9200B-D-MECH	Sample Reel, 55GHz TIA, 1mmx1mm DIE	GelPak	1 to 4
SFT-9200B-D-MS	Mechanical Sample Bag, 55GHz TIA, 1mmx1mm DIE	GelPak	5