USC68HC908

PROGRAMMABLE INTERRUPT CONTROLLER - CMOS

FEATURES

- Interfaces directly to the 68000
- $\overline{\text{DTACK}}$ generated on chip
- No system clock required
- 7 prioritized interrupt channels
  - 4 edge activated
  - 3 level activated
- Interrupts controlled through 5 internal registers
  - Interrupt pending register
  - Interrupt mask register
  - Interrupt enable register
  - Interrupt in service register
  - Interrupt vector register
- Fully TTL compatible
- High speed, low power, CMOS process
- Space savings 24 pin, 300 mil. package

DESCRIPTION

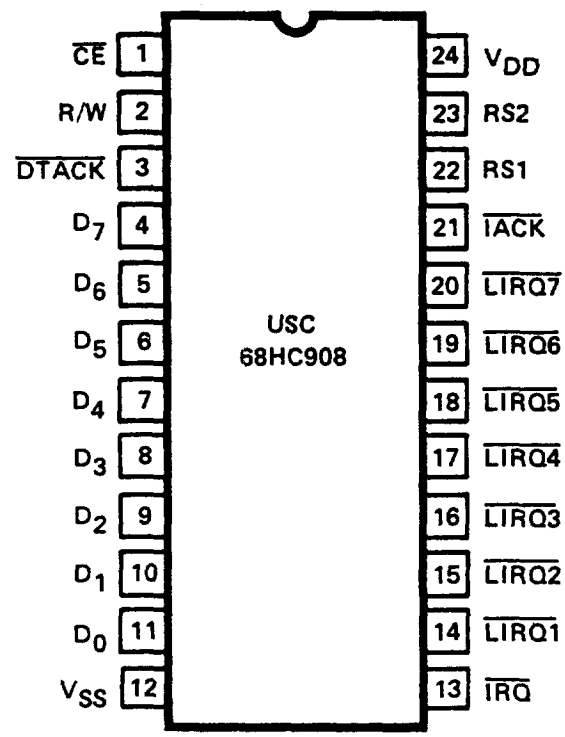
The USC68HC908 is a 7 channel Programmable Interrupt Controller (PIC) that has been designed to interface directly to the 68000 family of microprocessors. This low power CMOS device provides the user with advanced interrupt control features in a space saving 24 pin, slim line package. The on chip $\overline{\text{DTACK}}$ generation enables the PIC to appear to the 68000 in the same manner as memory. The single line chip select minimizes the amount of decode logic required to address the PIC.

Any number of USC68HC908's can be incorporated into a 68000 based system. Each chip is capable of monitoring and prioritizing up to 7 channels of interrupt with automatic nesting. To maximize the versatility of the PIC both edge and level activated inputs are provided. All inputs can be selectively enabled or disabled by programming the internal registers of the chip accordingly. These advanced features allow many interrupt functions normally handled in software to be performed with a single chip. A simplified block diagram of the USC68HC908 is illustrated in figure 1.

ORDERING INFORMATION

Part Number	Operating Temperature	Package
USC68HC908CPD	0°C to 70°C	Plastic
USC68HC908CCD	0°C to 70°C	Cerdip

PIN CONFIGURATION



BLOCK DIAGRAM

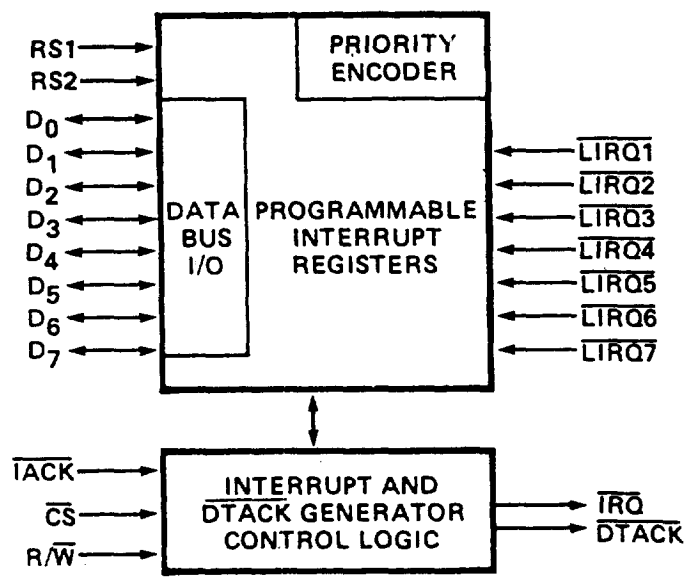


Figure 1. Programmable Interrupt Controller

OPERATION

GENERAL

The USC68HC908 interfaces 7 channels of interrupt directly to the 68000 microprocessor. After the PIC is programmed it continuously monitors all the specified interrupt channels. When an interrupt is received that has a higher priority then any currently pending or in service an interrupt request is transmitted to the processor. When the interrupt is acknowledged the PIC automatically responds by transmitting the interrupt vector number to the processor.

The USC68HC908 has 5 internal registers which control the operation of the PIC. Three of these registers are directly addressable by the 68000 while the other two registers are indirectly addressable through the Indirect Data Register (IDR). These registers contain the current programming and status of the chip. Figure 2 shows the internal registers of the chip.

INTERNAL REGISTERS

Interrupt Mask Register (IMR)

Address : 01
R/W : Read and Write

The interrupt mask register enables the user to selectively control which channels are allowed to generate an interrupt request. Resetting a bit in the IMR allows the USC68HC908 to monitor the Local Interrupt Request (LIRQ) inputs but disables them from causing an interrupt request. When a channel is masked off while it is generating an interrupt request, the interrupt terminates. If no other channels are requesting an interrupt, the IRQ output will be negated. As soon as the channel is unmasked in the IMR, its associated interrupt is allowed to resume its request. Only edge activated interrupts are latched in the Interrupt Pending Register (IPR) therefore any change in level activated channels will not be saved during the time it is masked off with the IMR.

Interrupt Enable Register (IER)

Address : 10
R/W : Read and Write

The IER is a dual function register. Its primary function is to activate an interrupt channel. Resetting a bit in this register will render the corresponding channel completely inactive. Any event that would normally generate an interrupt will be ignored and any pending interrupt on that channel will be cleared. Disabling a channel using the IER does not affect the contents of the interrupt in-Service Register (ISR). If the channel is in-service when it is disabled the corresponding bit will remain set until a "0" is written to its position in the ISR..

A secondary function of the IER is to point to one of two indirect registers accessed through the indirect data register. The least significant bit of the IER is used to perform this function. When the LSB is set to a "1", the Interrupt Vector Register (IVR) is accessed through the IDR. When the LSB of the IER is set to a "0", the in-service register will be accessed.

Interrupt Pending Register (IPR)

Address : 00
R/W : Read only

The IPR contains the state of the local interrupt request inputs. The USC68HC908 is capable of controlling both edge activated and level activated interrupts. For edge activated channels this bit is set when a high to low transition occurs after the channel is enabled in the interrupt enable register. The IPR bit is automatically reset during on interrupt acknowledge cycle, if it has the highest priority, and has not been masked in the interrupt mask register. This indicates that the channels associated vector has been passed to the host processor. On level activated channels, the IPR bit is set to indicate that the channel is enabled in the IER and a low level exists on the LIRQ input. For level activated inputs the IPR bit is not cleared during an interrupt acknowledge cycle and continues to reflect the complemented state of the local interrupt request input. Both edge and level activated interrupts can be masked or disabled by resetting the corresponding bit in either the IMR or the IER.

In-service Register (ISR)

Address : 11— bit 0 of IER = "0"
R/W : Read and Write

The ISR contains information regarding which interrupt channels are currently being serviced. The ISR bit is set and the IPR is reset during an interrupt acknowledge cycle, when the interrupt channels' vector is automatically down-loaded to the host processor. This indicates that the interrupt is in service and no longer pending. The ISR also serves to indicate the interrupt levels that are valid. Due to the multi-level priority scheme in this chip a lower priority interrupt will not be recognized while one of a higher priority is in service unless, the PIC has been programmed accordingly. The total number of bits set in the ISR represents the number of levels the present interrupt is nested. A bit in the ISR can only be reset by writing a "0" to that position from the processor. Resetting a bit in the ISR enables that channel to again recognize interrupts. This is normally performed prior to the execution of a return from interrupt instruction. At all times, regardless of the state of the ISR, the IPR can be accessed and pending interrupts can be checked. If the programmer decides that both interrupts can be serviced at the same time, toggling the corresponding bit in the IER resets the IPR bit. However, this is only true for the edge activated interrupt channels.

Bit 0 of the ISR is the Master Reset operation for the USC68HC908. To initialize the PIC, hex "00" is written to the ISR and is copied to all of the internal registers. For normal resets of the ISR, the user must insure that bit 0 is a "1."

Interrupt Vector Register (IVR)

Address : 11—bit 0 of the IER = "1"
R/W : Read and Write

The IVR contains the offset into any one of 256 interrupt vectors recognized by the 68000. The value contained in the IVR is the 5 most significant bits in the vector number. The other 3 bits are supplied by the local interrupt request number. If, for example the value "00000XXX" is loaded in the IVR and the chip acknowledges the LIRQ7 interrupt, a vector of "00000111" is downloaded to the host processor. ("00000111" = "00000XXX" + "111") In this manner any interrupt vector between hex "00" and "FF" can be generated. The USC68HC908 reserves the "00" internal vector for a phantom interrupt. The phantom interrupt is downloaded when an interrupt acknowledge occurs and there are no interrupts pending in the IPR. The user can thus protect program integrity from "spurious interrupt" possibilities.

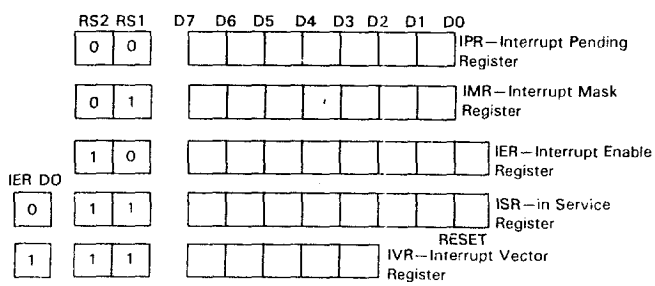


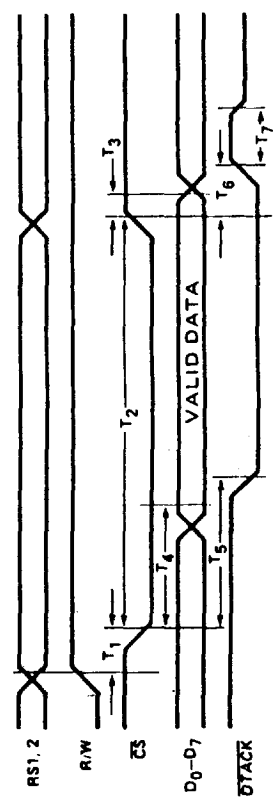
Figure 2. Programming and Data Registers

PIN DESCRIPTION

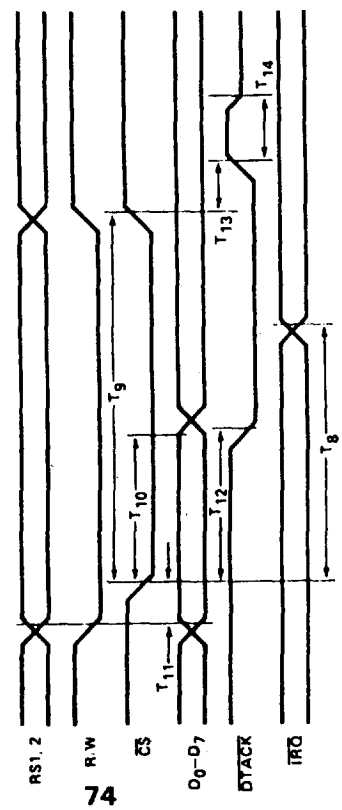
Pin No.	Type	Symbol	Name	Description
1	Input	$\overline{CE}$	Chip Enable	The $\overline{CE}$ pin activates the USC68HC908 for internal register access.
2	Input	R/W	Read/Write	This input defines a data transfer as either a read (high) or a write (low) operation.
3	Output	$\overline{DTACK}$	Data Transfer Acknowledge	This output signals the completion of the data transfer operation of a bus cycle to the processor. $\overline{DTACK}$ is asserted only when $\overline{CE}$ is asserted, or $\overline{IACK}$ is asserted.
11 - 4	I/O	$D_0 - D_7$	Data Bus	This bidirectional bus is used to receive data from or transmit data operation to the USC68HC908's internal registers during a processor read or write cycle.
22, 23	Input	RS1, RS2	Register Select	These 2 bits select one of the internal USC68HC908 registers during a read or write operation.
13	Output	$\overline{IRQ}$	Interrupt Request	This open drain output signals the processor that an interrupt is pending. This pin can be disabled by setting the appropriate bits in the interrupt enable register or the interrupt mask register.
16	Input	$\overline{IACK}$	Interrupt Acknowledge	This input signals the USC68HC908 that the host processor is ready to service a pending interrupt. The USC68HC908 will respond to this signal by downloading an interrupt vector on the data bus.
14 16 18 20	Input	$\overline{LIRQ1}$, $\overline{LIRQ3}$, $\overline{LIRQ5}$, $\overline{LIRQ7}$	Local Interrupt Request (edge)	These inputs are connected to the edge activated interrupt sources that the PIC is to control.
15 17 19	Input	$\overline{LIRQ2}$, $\overline{LIRQ4}$, $\overline{LIRQ6}$	Local Interrupt Request (level)	These inputs are connected to the level activated interrupt sources that the PIC is to control.
24	Supply	V_{DD}	V_{DD}	+5 volts
12	Supply	V_{SS}	V_{SS}	Ground

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



INTERRUPT ACKNOWLEDGE