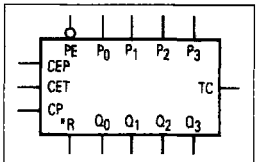
MOTOROLA

MC54F/74F160A
MC54F/74F162A

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

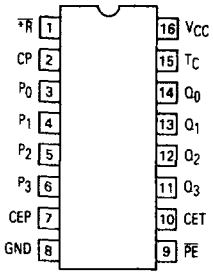
The MC54/74F160A and MC54/74F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC54/74F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC54/74F162A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The MC54 74F160A and MC54/74F162A are high-speed versions of the MC54/74F160 and MC54/74F162.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz



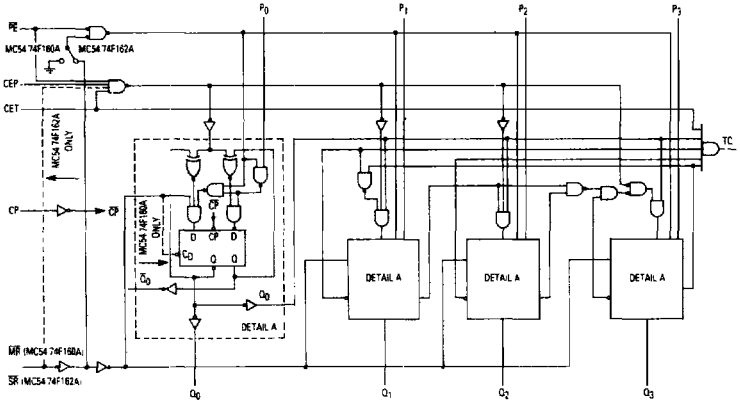
LOGIC SYMBOL

*$\overline{MR}$ for MC54/74F160A
*$\overline{SR}$ for MC54/74F162A



CONNECTION DIAGRAM

J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1	mA
I_{OL}	Output Current — Low	54, 74			20	mA

Functional Description

The MC54/74F160A and MC54/74F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the MC54/74F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC54/74F160A), synchronous reset (MC54/74F162A), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, MC54/74F160A), Synchronous Reset ($\overline{SR}$, MC54/74F162A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (MC54/74F160A) or $\overline{SR}$ (MC54/74F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

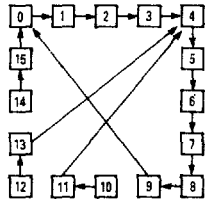
The MC54/74F160A and MC54/74F162A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

TRUTH TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌜)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For MC54/74F162A only H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

State Diagram



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Units	Test Conditions	
V_{IH}	Input HIGH Voltage		2			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current $\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	$\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET				0.1 0.1	mA	V_{CC} = MAX, V_{IN} = 7 V	
I_{IL}	Input LOW Current $\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$				−0.6 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Short Circuit Current		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			37	55	mA	V_{CC} = MAX	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC54/74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the MC54/74F160A and MC54/74F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

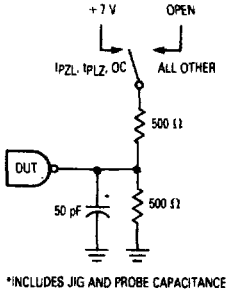
Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$
$TC = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$

AC CHARACTERISTICS See Page 5 for waveforms and load configurations

Symbol	Parameter	54/74F $T_A = +25°C$ $V_{CC} = +5\ V$ $C_L = 50\ pF$		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	100		75		90		MHz
t_{PLH} t_{PHL}	Propagation Delay, Count CP to Q_n ($\overline{PE}$ Input HIGH)	3.5 3.5	7.5 10	3.5 3.5	9 11.5	3.5 3.5	8.5 11	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.5 4	8.5 8.5	4 4	10 10	3.5 4	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5 4.5	14 14	5 5	16.5 15	5 4.5	15 15	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	7.5 7.5	2.5 2.5	9 9	2.5 2.5	8.5 8.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (MC54/74F160A)	5.5	12	5.5	14	5.5	13	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC (MC54/74F160A)	4.5	10.5	4.5	12.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS: See Page 5 for waveforms

Symbol	Parameter	54/74F $T_A = +25°C$ $V_{CC} = +5\ V$ $C_L = 50\ pF$		54F $T_A = -55°C$ to $+125°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		74F $T_A = 0°C$ to $70°C$ $V_{CC} = 5\ V \pm 10\%$ $C_L = 50\ pF$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	5 5		5.5 5.5		5 5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	2 2		2.5 2.5		2 2		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11 8.5		13.5 10.5		11.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2 0		2 0		2 0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP or CET to CP	11 5		13 6		11.5 5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0		0 0		0 0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5 5		5 5		5 5		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	4 6		5 8		4 7		ns
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW (MC54/74F160A)	5		5		5		ns
t_{rec}	Recovery Time $\overline{MR}$ to CP (MC54/74F160A)	6		6		6		ns



*INCLUDES JIG AND PROBE CAPACITANCE

Figure 1. Test Load

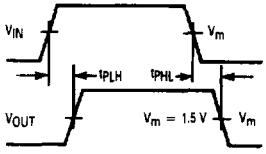


Figure 3. Waveform for Non-Inverting Functions

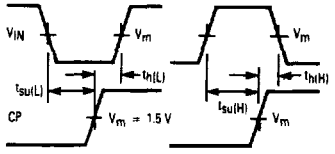


Figure 4. Setup and Hold Times, Rising-edge Clock

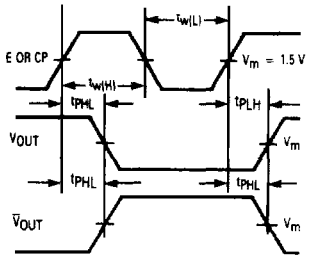


Figure 2. Propagation Delays from Rising-edge Clock or Enable

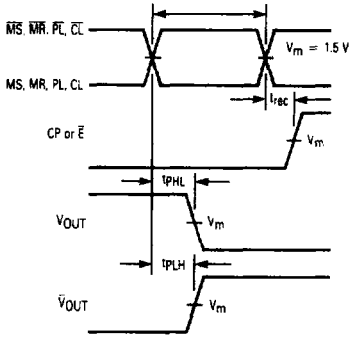


Figure 5. Asychronous Set, Reset, Parallel Load or Clear, Active Rising-edge Clock or Active-LOW Enable