256KB/512KB Neptune Compatible Second Level Cache Modules for Intel Pentium™ CPUs

Features

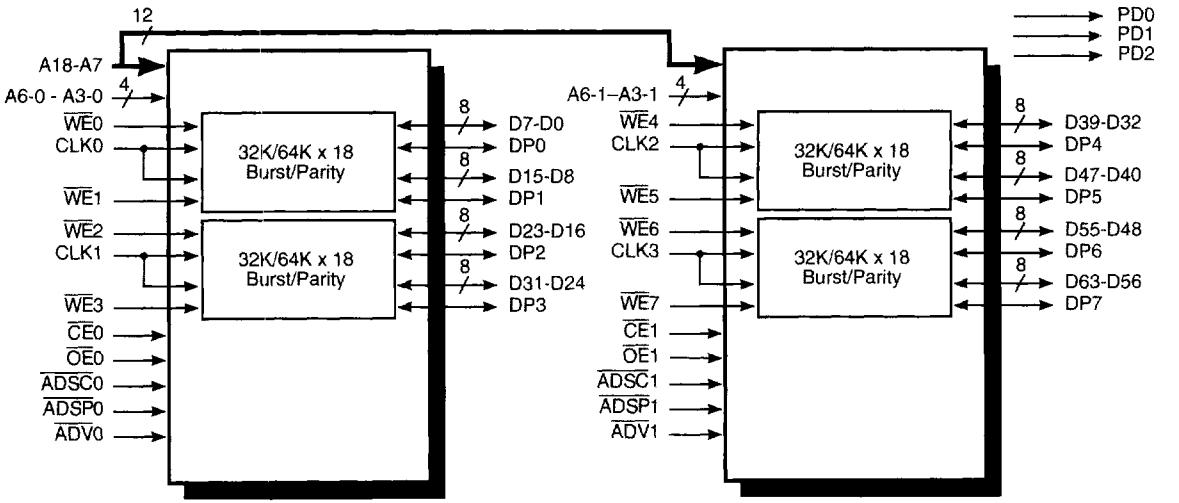
- 256KB and 512KB versions.
- 3.3V I/O compatible.
- Ideal for use with Intel Pentium™ CPU based systems. Especially those using Intel's 82430NX (Neptune) or VLSI 82C590 chipset.
- Supports system speeds up to 66 MHz.
- Uses multiple Vcc and ground pins along with decoupling capacitors for maximum noise immunity.
- Low profile, low cost 160-pin DIMM package.
- Designed for use with Burndy Computerbus™ connector P/N CELP2X80SC-3Z48.

Description

The PDM4M6181 and PDM4M6182 are high-performance CMOS static RAM modules. They are designed for use as second level caches for Intel Pentium™ CPU based systems. The modules are compatible with Intel's 82430NX (Neptune) chipset and VLSI's 82C590 chipset. Using 32K x 18 Burst SRAM, the PDM4M6181 is organized as 32K x 72 providing 256KB of second level cache memory. The PDM4M6182 is based on 64K x 18 Burst SRAM organized as 64K x 72. This provides 512KB of second level cache memory.

Both modules are 3.3V I/O compatible and are available in a 160-pin dual in-line memory (DIMM) package. This low profile package allows for modules with a maximum height of 1.15", a maximum length of 4.35" and a maximum thickness of 0.430". Equal clock line trace lengths are used to allow minimal clock skew. Multiple Vcc and ground pins are used along with on-board decoupling capacitors to ensure maximum protection from noise.

Functional Block Diagram



NOTE: D63-D0 and DP7-DP0 have 25Ω series termination resistors.

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Pin Description[1]

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{SS}	41	V_{SS}	81	V_{SS}	121	V_{SS}
2	D62	42	D10	82	D63	122	D11
3	V_{CC3}	43	V_{CC3}	83	V_{CC5}	123	V_{CC5}
4	D60	44	D8	84	D61	124	D9
5	V_{CC3}	45	DP0	85	V_{CC5}	125	DP1
6	D58	46	V_{CC3}	86	D59	126	V_{CC5}
7	D56	47	D6	87	D57	127	D7
8	V_{SS}	48	D4	88	V_{SS}	128	D5
9	DP6	49	D2	89	DP7	129	D3
10	D54	50	D0	90	D55	130	D1
11	D52	51	V_{SS}	91	D53	131	V_{SS}
12	D50	52	A3-0	92	D51	132	A3-1
13	V_{SS}	53	A4-0	93	V_{SS}	133	A4-1
14	D48	54	A5-0	94	D49	134	A5-1
15	D46	55	A6-0	95	D47	135	A6-1
16	D44	56	A8	96	D45	136	A7
17	D42	57	V_{SS}	97	D43	137	V_{SS}
18	V_{SS}	58	A10	98	V_{SS}	138	A9
19	D40	59	A12	99	D41	139	A11
20	DP4	60	A14	100	DP5	140	A13
21	D38	61	A16	101	D39	141	A15
22	D36	62	A18	102	D37	142	A17
23	D34	63	V_{SS}	103	D35	143	V_{SS}
24	V_{SS}	64	PD0	104	V_{SS}	144	NC
25	D32	65	PD2	105	D33	145	PD1
26	D30	66	CLK1	106	D31	146	CLK0
27	D28	67	CLK3	107	D29	147	CLK2
28	D26	68	V_{SS}	108	D27	148	V_{SS}
29	D24	69	WE6	109	D25	149	$\overline{WE7}$
30	V_{SS}	70	$\overline{WE4}$	110	V_{SS}	150	$\overline{WE5}$
31	DP2	71	$\overline{WE2}$	111	DP3	151	$\overline{WE3}$
32	D22	72	$\overline{WE0}$	112	D23	152	$\overline{WE1}$
33	D20	73	V_{SS}	113	D21	153	V_{SS}
34	V_{CC3}	74	$\overline{ADSC0}$	114	V_{CC5}	154	$\overline{ADSC1}$
35	D18	75	$\overline{CE0}$	115	D19	155	$\overline{CE1}$
36	V_{SS}	76	$\overline{ADV0}$	116	V_{SS}	156	$\overline{ADV1}$
37	D16	77	$\overline{OE0}$	117	D17	157	$\overline{OE1}$
38	V_{CC3}	78	V_{CC3}	118	V_{CC5}	158	V_{CC5}
39	D14	79	$\overline{ADSP0}$	119	D15	159	$\overline{ADSP1}$
40	D12	80	V_{SS}	120	D13	160	V_{SS}

NOTE 1. VCC5 is connected to the burst cache SRAMs for the 6181/82.
2. D63-D0 and DP7-DP0 have 25Ω series termination resistors.

Pin Assignment

Pin	Signal
A18-A3	Address Inputs
D63-D0	Inputs/Outputs
DP7-DP0	Parity Inputs/Outputs
$\overline{CE1}$-$\overline{CE0}$	Chip Enable Inputs
$\overline{WE1}$-$\overline{WE0}$	Byte Write Enable Inputs
$\overline{OE1}$-$\overline{OE0}$	Output Enable Inputs
$\overline{ADSP}$	Address Status Processor Inputs
$\overline{ADSC}$	Address Status Cache Controller Inputs
$\overline{ADV}$	Burst Address Advance Input
CLK1-CLK0	Clock Inputs
PD2-PD0	Presence Detect Pins
NC	No Connect
V_{SS}	Ground
Vcc	Power Supply

Presence Detection Code

Part No	Description	PD2	PD1	PD0
	No Cache Present	NC	NC	NC
PDM6181	256KB Burst	V_{SS}	V_{SS}	NC
PDM6182	512KB Burst	V_{SS}	V_{SS}	V_{SS}

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to+7.0	–0.5 to+7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
T_A	Operating Temperature	0 to +70	0 to +70	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{SS}	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

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DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Address)	V_{CC} = Max., V_{IN} = V_{SS} to V_{CC}	—	40	µA
I_{LI}	Input Leakage Current ($\overline{CE}$, $\overline{OE}$, Control)	V_{CC} = Max., V_{IN} = V_{SS} to V_{CC}	—	20	µA
I_{LI}	Input Leakage Current ($\overline{WE}$, CLK)	V_{CC} = Max., V_{IN} = V_{SS} to V_{CC}	—	5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V

NOTE 1. V_{IL} = –1.0V for pulse widths less than 5 ns, once per cycle.

Power Supply Characteristics

Symbol	Parameter	Max.	Unit
I_{CC}	Operating Current $\overline{CE} \leq V_{IL}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	1000	mA
I_{SB}	Standby Current $\overline{CE} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	400	mA
I_{SB1}	Full Standby Current $\overline{CE}$ > V_{CC} – 0.2V, V_{CC} = Max., f = 0, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V, Outputs Open	120	mA

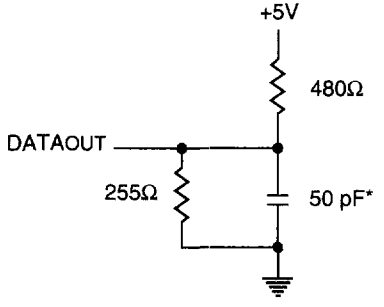
Capacitance[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN1}	Input Capacitance, (Address) V_{IN} = 0V	25	pF
C_{IN2}	Input Capacitance, ($\overline{CE}$, $\overline{OE}$, Control) V_{IN} = 0V	15	pF
C_{IN3}	Input Capacitance, ($\overline{WE}$, CLK) V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance V_{OUT} = 0V	10	pF

NOTE 1. This parameter is determined by device characteristics but is not production tested.

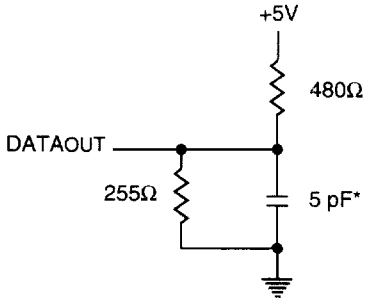
AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig capacitances

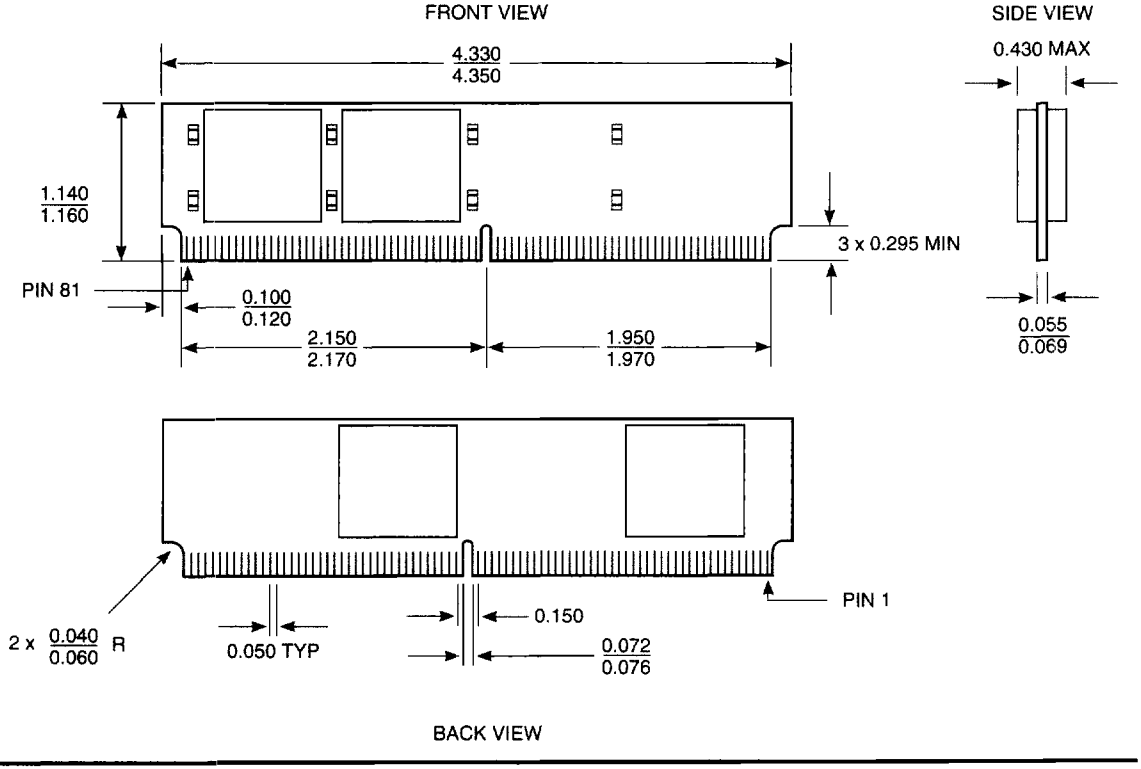
Figure 1. Output Load



* Including scope and jig capacitances

Figure 2. Output Load
(for tOHZ, tCHZ, tOLZ, and tCLZ)

Package Dimensions



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Ordering Information