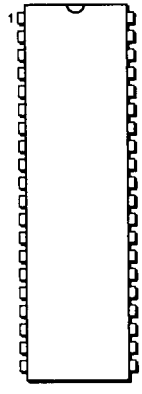
FEATURES

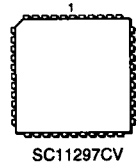
- ☐ ±5 V CMOS technology
- ☐ 7th order receive low-pass filter
- ☐ Adaptive hybrid function for near-end echo cancellation
- ☐ Support multi-mode modems from 300 bit/s to 14.4 kbit/s
- ☐ Serial DSP interface compatible with TMS320-25 series
- ☐ Band split filters for V.22, V.22 bis, V.21, V.23 and 103 modes with 55 dB minimum adjacent band rejection
- ☐ 0–18 dB coarse PGC (programmable gain control) in the receive path
- ☐ 12-bit ADC for echo cancelling and adaptive hybrid training
- ☐ 0–48 dB, 128 step PGC in the receive path
- ☐ 12-bit ADC for receive signal
- ☐ Programmable energy detect circuit
- ☐ 12-bit DAC for transmit and echo canceller
- ☐ 7th order low-pass reconstruction filter with sin x/x correction for the transmit signal
- ☐ 0–15 dB programmable attenuation for the transmit signal
- ☐ Buffer for line audio monitoring
- ☐ Analog and digital loopback

40-PIN DIP PACKAGE



SC11297CN

44-PIN PLCC PACKAGE



SC11297CV

GENERAL DESCRIPTION

This Modem Analog Front End (MAFE) can be used with a Digital Signal Processor (DSP) to implement high speed, 2-wire full duplex, echo cancelling modems based on CCITT V.32bis recommendations. It is also capable of operating in 4-wire full duplex, 2-wire half duplex and 2-wire full duplex modes based on CCITT V.26, V.27, V.27ter/bis, V.29, V.32, V.33, V.22bis, V.22, V.23, V.21 and Bell 212A/103 recommendations.

BLOCK DIAGRAM

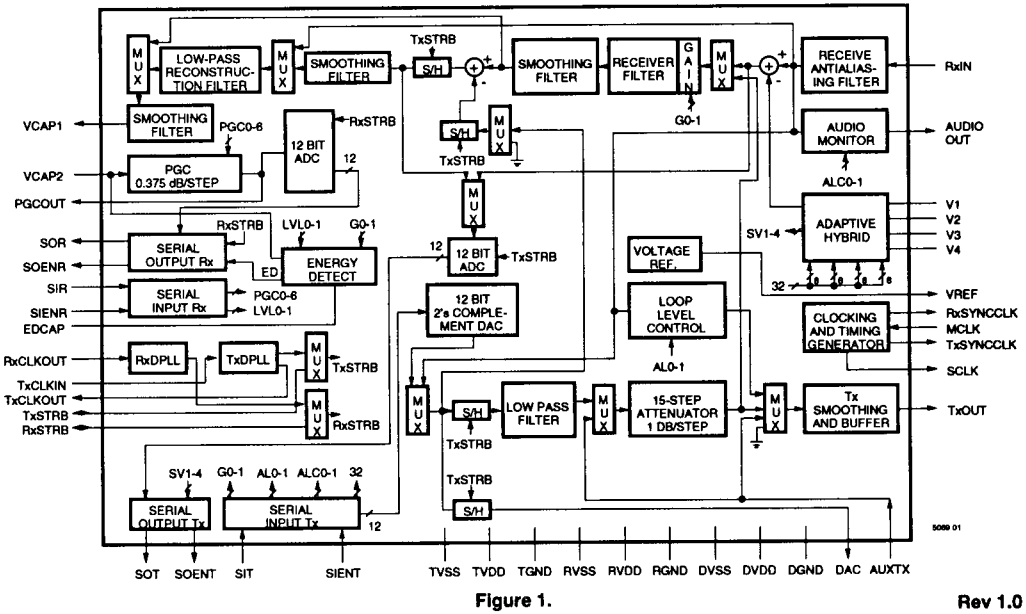


Figure 1.

GENERAL DESCRIPTION (continued)

One of the key features of the MAFE is the inclusion of circuitry to implement an adaptive hybrid. This circuitry, in conjunction with four external RC networks, will cancel the local echo by minimum of 20 dB. The adaptation process for the hybrid takes place during the training period of the echo canceller.

Band-split filters are also included to separate the receive and transmit signals, allowing the simple implementation of the V.22, V.22 bis, V.23, V.21 and Bell 212A/103 modes.

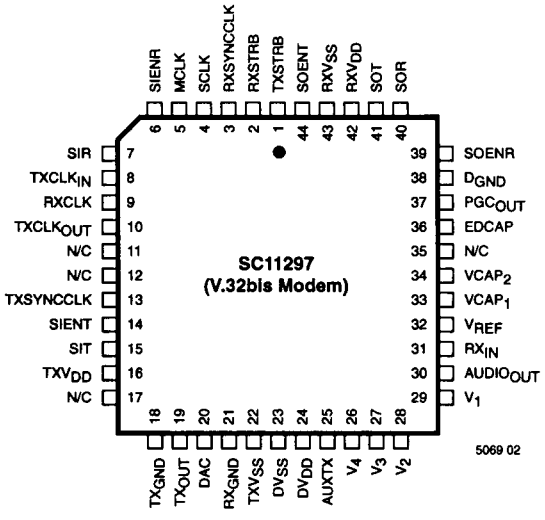
PIN DESCRIPTIONS

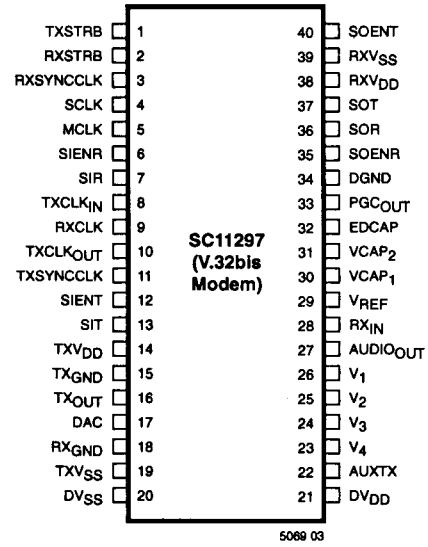
PIN NAME	PIN NUMBER PLCC	PIN NUMBER DIP	DESCRIPTION
$AUDIO_{OUT}$	30	27	Audio output. The analog receive signal is passed through a gain-stage buffer to drive a speaker for line monitoring.
AUXTX	25	22	Transmit auxiliary input; analog signal.
DAC	20	17	Transmit DAC's sampled and held output; analog signal. This auxiliary output is used for trimming the 12-bit transmit DAC output.
D_{GND}	38	34	Digital GND; D_{GND} = 0 V.
DV_{DD}	24	21	Digital V_{DD}; DV_{DD} = +5 V.
DV_{SS}	23	20	Digital V_{SS}; DV_{SS} = –5 V.
EDCAP	36	32	Energy detect capacitor; analog input. An external 0.1 µF capacitor should be connected between this pin and RX_{GND}.
MCLK	5	5	Master clock; TTL input. Must be 9.216 MHz. This clock generates various timing signals for the chip.
N/C	11, 12, 17, 35		Not connected.
PGC_{OUT}	37	33	Programmable gain-control section's sampled and held output; analog signal.
RXCLK	9	9	Receive data clock; TTL output. This signal which is generated internally by receive phase-locked loop provides timing for receive data stream.
RX_{GND}	21	18	Receive analog GND; RX_{GND} = 0 V.
RX_{IN}	31	28	Receive input; analog signal.
RXSTRB	2	2	Receive strobe; TTL input/output. This pin will be input if RSINT in receive interface is low, otherwise it will be an output. The falling edge of this signal will trigger the receive ADC.
RXSYNCCLK	3	3	TTL output. This pin provides a clock frequency which is 1.152 MHz and synchronous to RXCLK.
RXV_{DD}	42	38	Receive analog V_{DD}; RXV_{DD} = +5V.
RXV_{SS}	43	39	Receive analog V_{SS}; RXV_{SS} = –5V.
SCLK	4	4	Shift clock; TTL output and its frequency is 1/4 of the MCLK. This clock is used for serially shifting data in or out of the chip.
SIENR	6	6	Receive serial input enable; TTL input. A positive pulse on this input allows the serial data on SIR pin to enter the receive interface register.
SIENT	14	12	Transmit serial input enable; TTL input. A positive pulse on this input allows the serial data on SIT to enter the transmit interface register.
SIR	7	7	Receive serial input; TTL input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER PLCC	PIN NUMBER DIP	DESCRIPTION
SIT	15	13	Transmit serial input; TTL input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
SOENR	39	35	Receive serial output enable; TTL output. A positive pulse on this pin enables the data stored in receive output register to be serially shifted out through SOR pin.
SOENT	44	40	Transmit serial output enable; TTL output. A positive pulse on this pin enables the data stored in the transmit register to be serially shifted out through SOT pin.
SOR	40	36	Receive serial output; TTL output. Data is shifted in 13-bit blocks. The first 12-bit correspond to ADC data. Bit 13 (ED) indicates the status of energy detect.
SOT	41	37	Transmit serial output; TTL output. During each transmit strobe cycle, this pin outputs two blocks of data. First one carries echo signal information and the second one corresponds to adaptive hybrid output.
$TXCLK_{IN}$	8	8	Transmit clock input; TTL input. This is the external timing source which transmit phase-locked loop locks onto.
$TXCLK_{OUT}$	10	10	Transmit data clock; TTL output. This signal which is generated internally by transmit phase-locked loop provides timing for transmit data stream.
TX_{GND}	18	15	Transmit analog GND; TX_{GND} = 0 V.
TX_{OUT}	19	16	Transmit output; analog signal.
TXSTRB	1	1	Transmit strobe; TTL input/output. This pin will be input if TSIN/$\overline{EX}$ in transmit input interface is low otherwise, it will be an output. Falling edge of this signal triggers the transmit DAC and echo canceller ADC.
TXSYNCCLK	13	11	TTL output. This pin provides a clock frequency which is 1.152 MHz and synchronous to $TXCLK_{OUT}$.
TXV_{DD}	16	14	Transmit analog V_{DD}; TXV_{DD} = +5 V.
TXV_{SS}	22	19	Transmit analog V_{SS}; TXV_{SS} = –5 V.
V_1–V_4	29–26	26–23	Four inputs to the adaptive hybrid; analog signal.
$VCAP_1$, $VCAP_2$	33, 34	30, 31	An external capacitor is required between these two pins. This capacitor together with an internal 25 kΩ resistor forms a high-pass filter that removed the DC component of the signal before entering the PGC. The –3 dB frequency for this high pass filter is given by $f_{-3dB} = \frac{1}{50{,}000\pi\ C_{ext}}$
V_{REF}	32	29	Reference voltage; analog signal.

CONNECTION DIAGRAMS





NOTE: Pinouts subject to change without notice.

GENERAL CHIP DESCRIPTION

A simplified block diagram of the MAFE is shown in Figure 1. The receive signal passes through the antialising filter and is summed with the output of the adaptive hybrid thereby cancelling the near-end echo. The resulting signal is fed to the receive filter. The receive filter block consists of a low-pass, two high-pass, and notch sections. These filters, under the transmit interface control, can be configured in different ways to support the appropriate modes of operation. The output of the receive filter is fed to an analog filter where it is smoothed. The output of the smoothing filter, in the V.32 mode when the echo canceller is active, is sampled by the transmit strobe and summed with the estimated echo signal. This sampled-and-held signal is fed to a 12-bit Analog-to Digital Converter (ADC) and a reconstruction filter. The 12-bit ADC converts the analog signal to a 12-bit 2's complement number then sends it through the transmit serial output interface to the DSP. The reconstruction filter smooths the sampled-and-held signal and compensates for the sin x/x distortion effects. The output signal of the smoothing filter is connected to the VCAP1 pin and AC coupled by an external capacitor to the input (VCAP2 pin) of a 128-step, 0.375 dB/step, Programmable Gain Control (PGC). The output of the PGC is sampled with the receive strobe and converted to a digital signal by a 12-bit 2's complement ADC. This digital signal or word is transferred to the DSP through the receive serial output interface. In all other modes of operation where the echo-canceller is deactivated, the summing circuit, sample-and-hold circuit and reconstruction filters are bypassed and the output of the receive filter is fed directly into the PGC.

The MAFE also includes an energy detect circuit which determines the presence of the signal. The threshold levels of the energy detector are programmable through the receive interface.

The transmit section consists of a 12-bit 2's complement Digital-to-Analog Converter (DAC), a sample-and-hold low pass reconstruction filter, a programmable attenuator and a smoothing filter/buffer circuit. When the echo canceller is active, in each period of the transmit strobe, two 12-bit words are supplied to the 12-bit DAC. The DAC performs two consecutive conversions. The output of the first conversion is the estimated echo sample and is added to the receive signal. The output of the second conversion is the transmit signal which is fed to a sample-and-hold circuit and subsequently to the low pass reconstruction filter with a sin x/x correction for 9.6 kHz sample rate. The output signal from the low pass filter goes through a 15-step, 1 dB/step attenuator and a transmit smoothing filter/buffer which is capable of driving a 600 Ω load.

The MAFE also includes a transmit digital phase-lock loop and a receive digital oscillator that, under

the receive interface control, can be used as a digital phase-lock loop. An audio monitor with a programmable attenuator allows monitoring of the line activities in the call progress monitor mode.

The master clock input to the chip is a 9.216 MHz clock. All necessary timing and filter clocks are internally generated by a timing generator.

The chip has four serial interfaces, two for transmit and two for receive. The subsequent sections will give a more detailed description of the individual blocks.

Receive Filter

The block diagram of the receive filter is shown in Figure 2. The input signal first enters a 2nd order continuous time antialiasing filter and then a cosine filter. The cosine filter is clocked at a 230.4 kHz rate and takes two samples during every clock cycle effectively increasing the sampling rate to 460.8 kHz. The output of the cosine filter is summed with the output of the adaptive hybrid, fed through a summing filter to a 2nd order low-pass smoothing filter. When the adaptive hybrid is disabled, the corresponding signal path is connected to ground. The smoothing filter output drives a 7th order low-pass filter, clocked at 230.4 kHz, with two transmission zeros. The pass band edge of the filter is at 3200 Hz and provides a minimum of 55 dB loss in the stopband region.

The low-pass filter is followed by a high-pass section clocked at 230.4 kHz. The filter has a third order transfer function with the passband edge at 300 Hz. It provides 30 dB loss at 60 Hz. The low-pass, high-pass combination creates a band-pass filter with a passband response from 300Hz to 3200 Hz. The frequency response of this band-pass filter along with the details of the passband and the group delay response are shown in Figures 3a, 3b, and 3c respectively. The high-pass filter is followed by a second order smoothing section which eliminates the clock noise from the output signal. In V.22 bis/V.22/Bell 212A/V.21/V.23 modes, where full duplex operation is achieved by frequency division, the receive filter is configured as a bandsplit section to reject the adjacent band. In the Answer mode, where the modem transmits in the high-band and receives in the low-band, the clock of the Rx low-pass filter is reduced by a factor of two to 115.2 kHz, while the high-pass clock is kept at 230.4 kHz. This moves the low-pass filter passband edge to 1600 Hz and in conjunction with the high-pass, produces a bandpass filter with response from 300 Hz to 1600 Hz. The filter provides a minimum of 55 dB rejection over the high band frequency range. An additional programmable notch filter can be inserted in the signal path to remove the guard tone in the Answer mode. A notch frequency at 550 or 1800 Hz can be selected through the transmit serial interface. In the V.21 mode the same arrangement is used except that the filter clock is reduced by a factor of 2.5. This moves the low-pass filter pass band edge to 1280 Hz.

In the Originate mode, the modem transmits in the lowband and receives in the highband. The receive low-pass filter in this case is clocked at a rate of 230.4 kHz and an additional 7th order high-pass filter is inserted between the low-pass and the 300 Hz high-pass filters. The passband edge of the high-pass filter, which is clocked at 115.2 kHz, is 2000 Hz and introduces a minimum of 55 dB rejection in the low-band frequency range. The combination of the low-pass and high-pass filters produces a band-pass filter with a passband that extends from 2000 Hz to 3200 Hz. In the V.21 mode the filter clock is reduced by a factor of 1.25, which moves the pass band to the 1600 Hz to 2560 Hz range.

In V.23 forward-channel transmission mode the clock of the Rx low-pass filter is kept at 230.4 kHz, while the V.22 bis high-pass clock is reduced to 57.4 kHz. This arrangement produces a bandpass filter that extends from 1000Hz to 3200 Hz and passes the forward channel but rejects the backward channel. In the reverse mode where the receive signal is in the backward channel, the V.22 bis high-pass filter is bypassed and the clock of the Rx low-pass filter is reduced by a

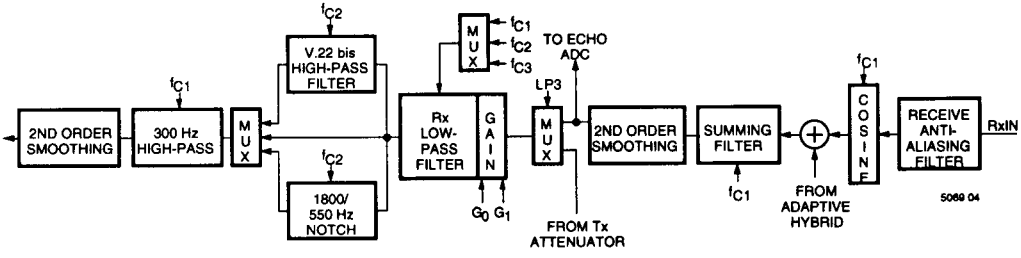


Figure 2. Receive Filter Block Diagram

factor of 5 to 46.08 kHz. The Rx low-pass and the 300 Hz high-pass filter combination produces a bandpass filter which extends from 300Hz to 640 Hz. This filter will pass the backward channel and reject the forward channel.

The overall frequency response and the group delay of the various highband and lowband filters for different modes of operation are shown in Figures 4–7.

A 2-bit programmable gain control is implemented at the input of the receive low-pass filter. Depending on the amount of rejection of the adaptive hybrid and the magnitude of the receive signal, the input gain can be increased to improve the noise performance of the modem.

Receive Reconstruction Filter

In the V.32 mode, when the echo canceller is active, the output of the receive filter is sampled by the transmit strobe and summed with the estimated echo signal. The sampled-and-held signal goes to two blocks. It feeds a 12-bit ADC which converts the analog signal to a 12-bit 2's complement number. It also goes to a reconstruction filter. The first section of this filter is a 2nd order active RC circuit which removes the high frequency components of the signal to allow sampling it with a 230.4 kHz clock. The smoothed signal is subsequently applied to a switched capacitor low-pass filter section which removes the remaining high frequency signal components and also compensates for the sin x/x distortion effects of a 9.6 kHz sampling rate. The output of the low-pass filter is passed through a second order active RC filter, to remove the clock noise, to the VCAP1 pin where it is externally AC coupled to the programmable gain control. The block diagram of the receive reconstruction filter is shown in Figure 8a. The details of the amplitude and delay responses are shown in Figures 8b, 8c and 8d.

Echo Analog-to-Digital Converter

The 12-bit ADC is operational only when the echo canceller is active. The input to the ADC comes from two sources, the echo canceller sample-and-hold (Figure 8a) and the receive input summing filter (Figure 2). The ADC is capable of

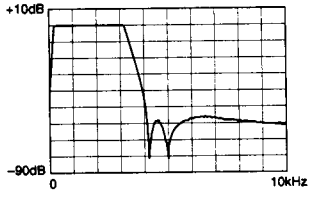


Figure 3a. Overall Frequency Response (Normal Mode)

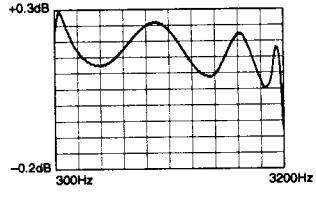


Figure 3b. Details of Passband (Normal Mode)

Figure 3c. Passband Group Delay (Normal Mode)

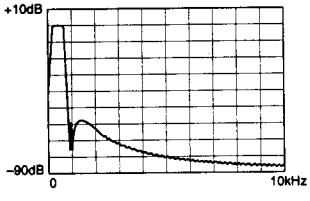


Figure 4.1a. Overall Frequency Response (V.23BC/CPM)

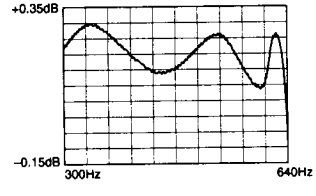


Figure 4.1b. Details of Passband (V.23BC/CPM)

Figure 4.1c. Passband Group Delay (V.23BC/CPM)

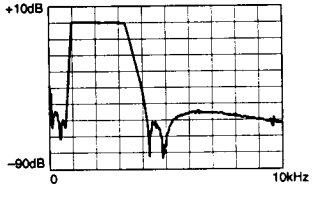


Figure 4.2a. Overall Frequency Response (V.23FC)

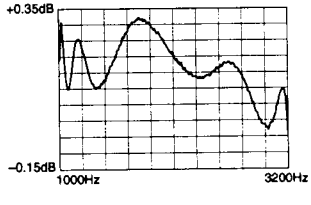


Figure 4.2b. Details of Passband (V.23FC)

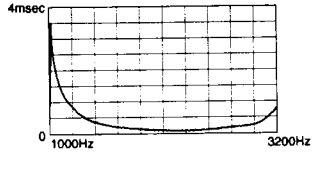


Figure 4.2c. Passband Group Delay (V.23FC)

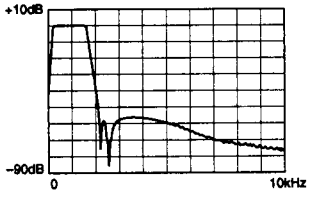


Figure 5.1a. Overall Frequency Response (103A)

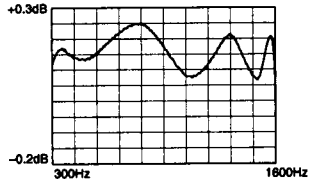


Figure 5.1b. Details of Passband (103A)

Figure 5.1c. Passband Group Delay (103A)

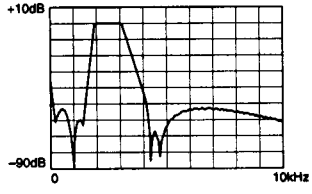


Figure 5.2a. Overall Frequency Response (103O)

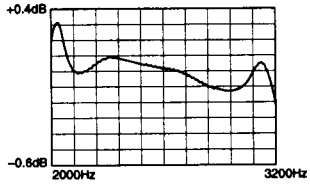


Figure 5.2b. Details of Passband (103O)

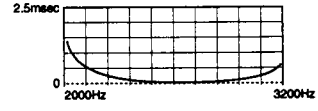


Figure 5.2c. Passband Group Delay (103O)

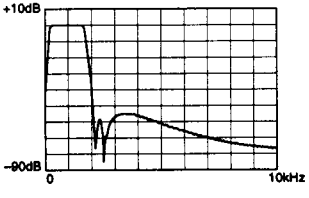


Figure 6.1a. Overall Frequency Response (V.22A)

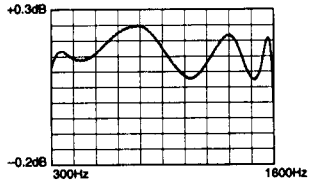


Figure 6.1b. Details of Passband (V.22A)

Figure 6.1c. Passband Group Delay (V.22A)

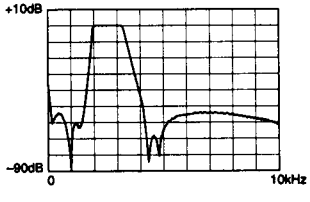


Figure 6.2a. Overall Frequency Response (V.22O)

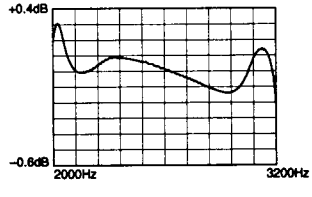


Figure 6.2b. Details of Passband (V.22O)

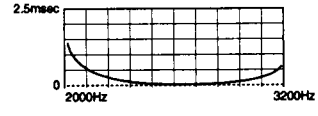


Figure 6.2c. Passband Group Delay (V.22O)

Figure 7.1a. Overall Frequency Response (V.21A)

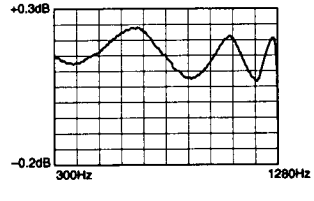


Figure 7.1b. Details of Passband (V.21A)

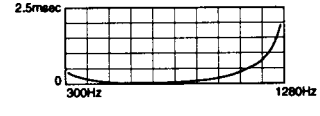


Figure 7.1c. Passband Group Delay (V.21A)

doing two conversions in one period of the transmit strobe. In a typical example of echo cancellation process, adaptive hybrid and echo canceller are enabled at first and their outputs are sampled by two sample-and-hold circuits on the falling edge of transmit strobe signal. The 12-bit ADC converts both samples to digital codes during each strobe period, however, in the beginning echo samples are ignored and digital processor concentrates on adjusting the adaptive hybrid. This phase takes T1 seconds after which both samples will be used to adjust adaptive hybrid and echo canceller. This process takes T2 seconds after which the adaptive hybrid coefficients are frozen and the echo canceller takes over. During the following period, T3, the ADC converts only one sample which is taken from the output of the echo canceller sample-and-hold. It is possible that the overlap time T2, where both the adaptive hybrid and echo canceller are adjusted, can be zero. In this case, the adaptation of the echo canceller starts only after the hybrid adaptation has stopped. Figure 9 shows the internal timing of the 12-bit ADC. In a non V.32 mode, when the echo canceller is deactivated, the 12-bit ADC is disabled and no conversion is made.

Adaptive Hybrid (AH)

The Adaptive Hybrid serves as the front end, local loop, near end echo canceller. Using four RC networks and adjusting their individual attenuations with four 8-bit multiplying DACs to match the inverse of the incoming echo, the echo can be cancelled by a minimum of 20 dB. Figure 10 presents the arrangement of the Adaptive Hybrid where the three networks are simple RC circuits. The actual implementation of the Adaptive Hybrid is shown in Figure 11 with the three external RC networks and one direct connection. The four 8-bit multiplying DACs attenuate the RC network outputs with gains in the range of 0 to ±0.99. The switched-capacitor summer adds the output of the four DAC sets and subtracts it from the echo input. The output of the summer feeds into the 12-bit ADC for conversion. The outputs of the four RC networks are also fed to four comparators for sign extraction. When performing adaptive hybrid cancellation the signal processor reads the magnitude of the echo and the sign of the four individual

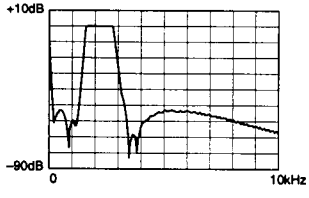


Figure 7.2a. Overall Frequency Response (V.21O)

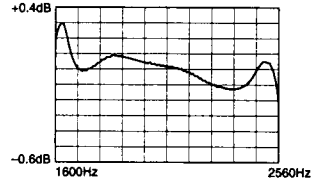


Figure 7.2b. Details of Passband (V.21O)

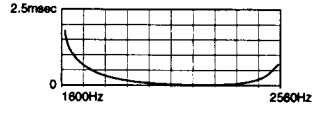


Figure 7.2c. Passband Group Delay (V.21O)

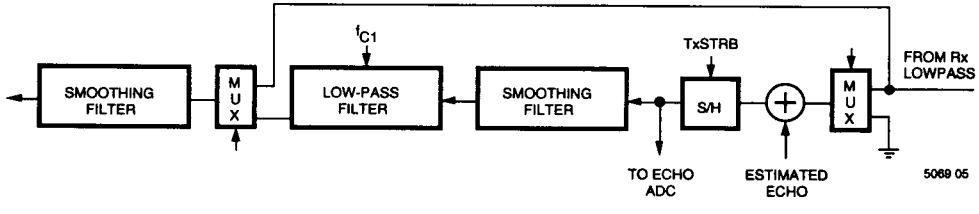


Figure 8a. Receive Reconstruction Filter Block Diagram

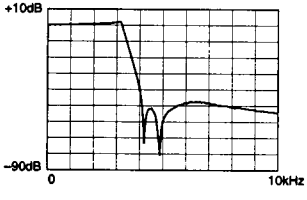


Figure 8b. Overall Frequency Response (RX Reconstruction)

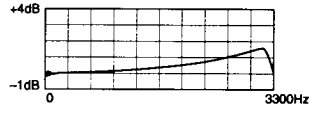


Figure 8c. Details of Passband (RX Reconstruction)

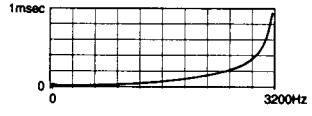


Figure 8d. Passband Group Delay (RX Reconstruction)

RC sections (note that one RC section is just a direct connection). It then calculates the new coefficients for the DACs so as to drive the near end echo magnitude towards zero. A more detailed description of the adaptation algorithm and recommendations for RC networks is presented in Appendix A.

Transmit Section

The transmit section shown in Figure 12 includes a 12-bit DAC, two sample-and-holds, an analog smoothing filter, a switched-capacitor low-pass filter and a programmable 15-step 1 dB/step attenuator. In the V.32 mode, when the echo canceller is active, the signal processor chip supplies two 12-bit digital codes to the DAC during each period of the transmit strobe. The first code is the echo estimate and the other is the transmit signal. The DAC does two consecutive conversions and feeds the analog samples to two sample-and-hold circuits. The echo sample-and-hold output goes to the receive section and cancels the echo from the receive signal. The transmit sample-and-hold output goes to an analog antialiasing filter before it is fed to the low-pass reconstruction filter. This filter has a seventh order transfer function and it compensates for the sin x/x distortion effects due to a 9.6 kHz sample-and-hold. The frequency response of the transmit filter, which has a clock frequency of 230.4 kHz and passband edge of 3200Hz, is shown in Figure 13, where Figure 13a is the overall amplitude response, 13b shows the details of the passband amplitude response, and 13c is the passband group delay response. It is important to mention that the overall transmit amplitude response is achieved by combining the transmit filter response with the $\sin(\omega T/2)/(\omega T/2)$ response of the sample-and-hold circuit.

The transmit filter is followed by a 15 step, 1 dB/step attenuator. The

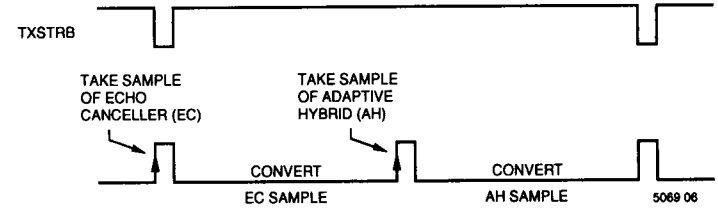


Figure 9. 12 Bit ADC Timing

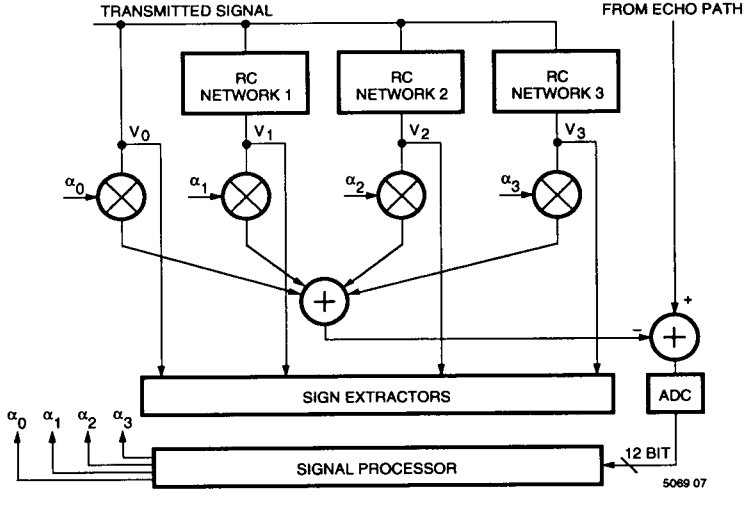


Figure 10. Adaptive Hybrid Block Diagram

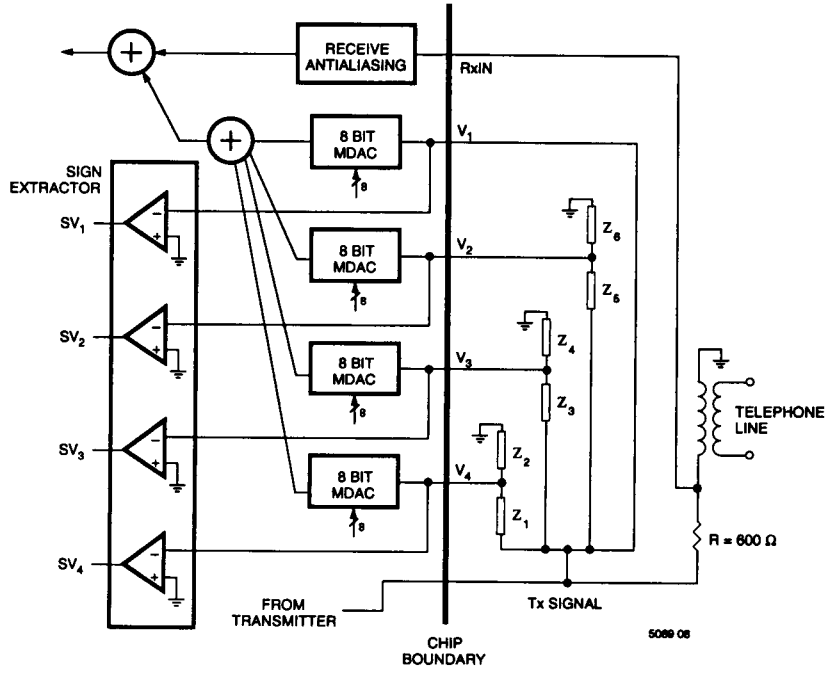


Figure 11. Adaptive Hybrid

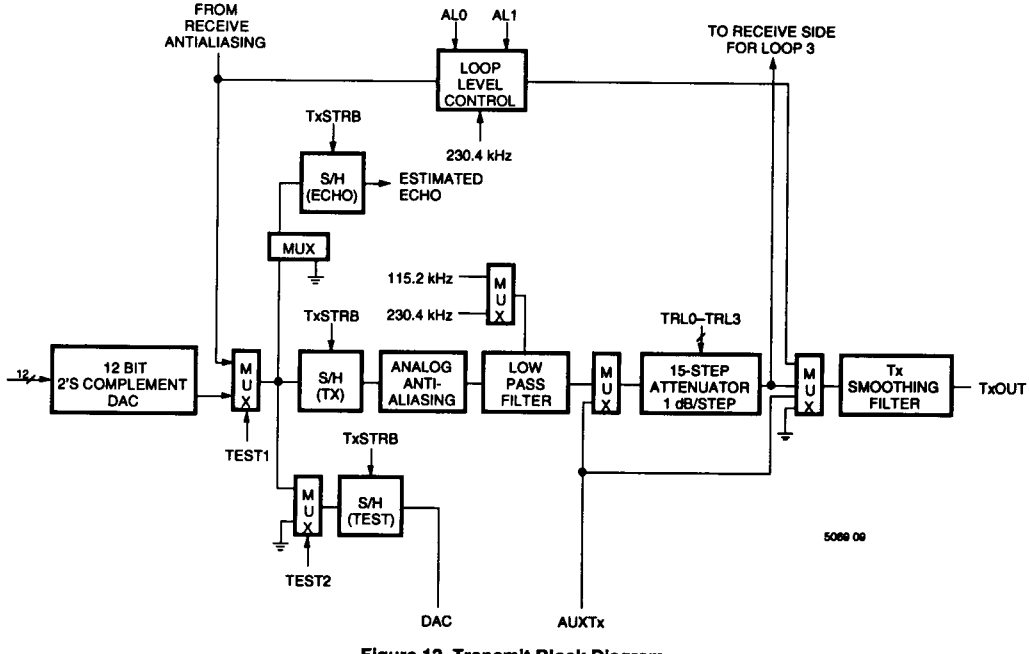


Figure 12. Transmit Block Diagram

output of the attenuator is smoothed by the transmit continuous time smoothing filter which drives the telephone line. An auxiliary input signal can be injected into the chip through the AUXTX pin. This input goes to the line either directly through the transmit smoothing filter or it can be routed through the transmit attenuator for amplitude control.

In those modes of operation when the echo canceller is disabled, the processor will not supply the sample of the echo estimate and the echo sample-and-hold input will be connected to ground. The 12-bit DAC will do one conversion in one period of the transmit strobe.

The clock of the transmit filter can be reduced by a factor of 2 or 2.5 under processor control. For the low sampling clock, the passband edge of the filter moves to 1.6 or 1.28 kHz. This feature is useful in the V.23 backward channel or V.22 bis, Bell 212A or V.21 originate modes when the transmit signal is in the lowband. The filter can be used to eliminate the components of the lowband signal that fall into the highband region. However, since the filter amplitude response is optimized to compensate for a 9.6 kHz sample-and-hold effect, reducing the clock frequency by a factor of 2 or 2.5 will introduce an additional amplitude distortion. In the mode where the transmit signal is in the highband, the transmit filter can be used without reducing the clock frequency. If the adjacent band filtering is done digitally, then it may not be necessary to reduce the transmit filter clock frequency.

Loopback

Two loopback modes are supported by the SC11297. In loop 3 mode, the transmit signal is routed to the input of the receive filter, and the receive input signal is ignored. In loop 4 mode, the analog receive signal is routed to the transmitter through a four level programmable gain control.

Call Progress Tone Monitor

In the Call Progress Mode (CPM), the clock frequency of the receive low-pass filter is reduced to 1/5 of its normal value. This moves the pass-band edge of the low-pass filter to 640 Hz. The low-pass and high-pass combination form a band-pass filter with a pass-band range of 300Hz to 640 Hz. The response of this filter is shown in Figure 4. The received analog signal passes through the band-pass filter and then into the energy detect circuit. The energy detect output can be monitored by the signal processor to indicate the presence of energy.

Audio Monitor

The analog receive signal is passed through a level controller and a buffer to drive a speaker for line audio monitoring.

This circuit is used during call progress detection to monitor call progress tones. The audio signal level can be controlled by ALC1 and ALC0.

Energy Detector

The energy detector monitors the receive signal and indicates the presence of the signal through ED logic output. The detection level is selected between four distinct levels by control bits LVL0 and LVL1 in receive input interface. The energy detector needs one external capacitor.

Serial I/O

The MAFE has four serial input/output ports; two for the transmit and two for the receive strobes. The serial I/O is designed to be compatible with DSP chips such as TMS320-25.

Transmit Serial Input Interface

This block accepts 16-bit serial words that consist of address and control/data bits. The 4 MSB's correspond to the addresses of internal registers and the remaining bits convey the information about transmit signal, echo, adaptive hybrid or SC11297 set up. The data on SIT pin will be shifted in this serial port on the falling edges of the SCLK and must be valid at these time points. Figure 14a shows the timing diagram for the transmit serial input port and timing requirements are given in Table 1. When writing into the 12-bit DAC registers (TX data or echo data), the timing of Figure 14b with respect to TX strobe (TXSTRB) should be followed to ensure proper conversion by DAC. MSB of data is shifted in first. Table 2 shows the register structure of the transmit input interface, followed by bit descriptions.

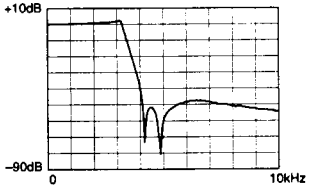


Figure 13a. Overall Frequency Response (TX Reconstruction)

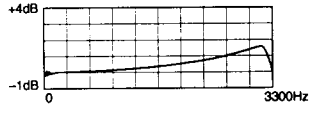


Figure 13b. Details of Passband (TX Reconstruction)

Figure 13c. Passband Group Delay (TX Reconstruction)

Reference Voltage

This section provides a reference voltage with a nominal value of 2.5 V for on chip use. A buffered version of this voltage is provided off chip for external power supply low voltage detect purposes.

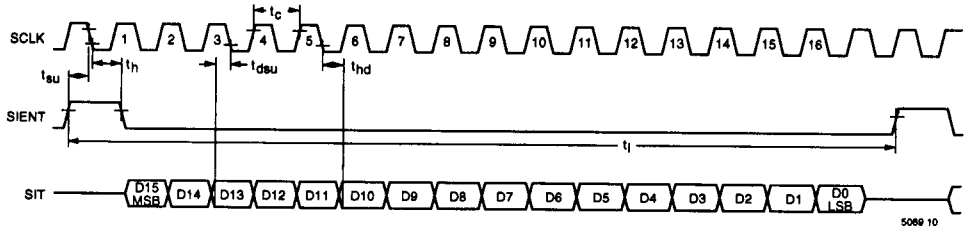


Figure 14a. Tx Serial Input Timing

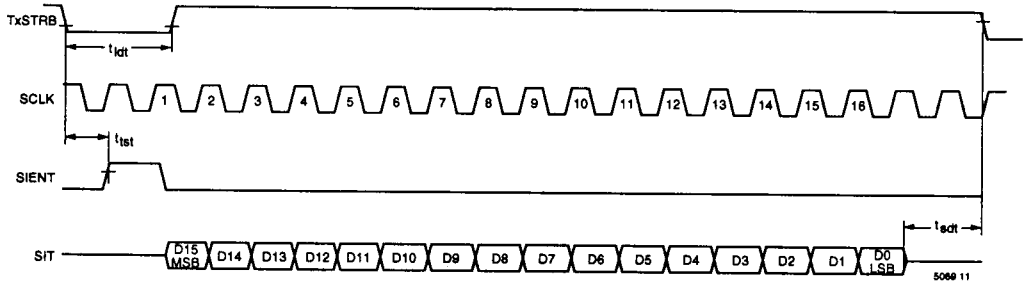


Figure 14b. Tx Serial Input Timing With Respect to TxSTRB (For Tx D/A Only)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{su}	Set up time from SIENT high to SCLK low	80			ns
t_h	Hold time from SCLK low to SIENT low	50			ns
t_{hd}	Hold time from SCLK low to SIT transition	50			ns
t_{dsu}	Data set up time from SIT valid to SCLK low	80			ns
t_i	Interval between consecutive SIENT pulses	5.9			µs
t_{idt}	Low duration of TxSTRB	.2		102	µs
t_{tst}	Set up time from TxSTRB low to SIENT high	0			ns
t_{sdt}	Delay time from last input data to TxSTRB low	2			µs
t_{tso}	Delay time from TxSTRB low to SOENT high	60		425	ns
t_{do}	Delay time from SCLK high to SOENT high			100	ns
t_{ti}	Time interval between two SOENT pulses following a high-to-low transition of TxSTRB		5.9		µs
t_{db}	Delay time from SCLK high to SOT valid			100	ns
t_{hz}	Hold time from SCLK low to SOT high impedance	50			ns
t_C	Serial clock period		325		ns

Table 1. Timing Requirements for Tx Serial Input/Output Interfaces

Register	Add. Bits	DATA/CONTROL BITS											
	D15–D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TxD	0000	TxD11	TxD10	TxD9	TxD8	TxD7	TxD6	TxD5	TxD4	TxD3	TxD2	TxD1	TxD0
ECHO	0001	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
AHDAC1	0010	—	—	—	—	DH17	DH16	DH15	DH14	DH13	DH12	DH11	DH10
AHDAC2	0011	—	—	—	—	DH27	DH26	DH25	DH24	DH23	DH22	DH21	DH20
AHDAC3	0100	—	—	—	—	DH37	DH36	DH35	DH34	DH33	DH32	DH31	DH30
AHDAC4	0101	—	—	—	—	DH47	DH46	DH45	DH44	DH43	DH42	DH41	DH40
CR1	0110	AL1	AL0	TR1	TR0	CLK2	CLK1	CLK0	TPLL Jam	TPLL $\overline{IN}/EX$	TPLL LK/$\overline{FR}$	TS $\overline{IN}/EX$	TxST
CR2	0111	ENAH	ENEC	SQEC	LP3	G1	G0	HYEN	TR3	TRL3	TRL2	TRL1	TRL0
CR3	1000	TEST3	TEST2	TEST1	NSEL	NI	TXFC	MD3	MD2	MD1	MD0	ALC1	ALC0

Table 2. Transmit Input Interface

TX Data Register: Address 0000

TXD0–11	12-bit 2's complement data representing transmit data sample.

ECHO Register: Address 0001

EC0–11	12-bit 2's complement data representing echo estimate sample.

Adaptive Hybrid Registers: Address 0010–0101

DH 10–17	8-bit sign magnitude data representing scale factor for the output voltage of network #1.
DH20–27	8-bit sign magnitude data representing scale factor for the output voltage of network #2.
DH30–37	8-bit sign magnitude data representing scale factor for the output voltage of network #3.
DH40–47	8-bit sign magnitude data representing scale factor for the output voltage of network #4.

CR1 Register: Address 0110

TXST	Determines the rate of the transmit strobe. (See the section corresponding to MD0–MD3.) TXST = 1 9.6 kHz TXST = 0 7.2 kHz
TS IN/$\overline{EX}$	Determines whether the TX strobe is generated internally or supplied externally. TS IN/$\overline{EX}$ = 1 Internal TS IN/$\overline{EX}$ = 0 External In the external mode, the TX DPLL will be disabled, and the TXCLKOUT pin will go to a high or low state.
TPLL LK/$\overline{FR}$	Determines whether the transmit DPLL is in the locked or free run mode. TPLL LK/$\overline{FR}$ = 1 Locked TPLL LK/$\overline{FR}$ = 0 Free Run
TPLL IN/$\overline{EX}$	In the locked mode, this bit determines the signal that the TX DPLL locks to. TPLL IN/$\overline{EX}$ = 1 Locked to RXCLK TPLL IN/$\overline{EX}$ = 0 Locked to TXCLKIN If TPLL LK/$\overline{FR}$ = 0, this bit will be ignored.
TPLL JAM	When this bit is set, the transmit DPLL will reset itself on the next rising edge of the clock that it locks to. Once the DPLL is jammed, the bit will be automatically reset. After the jam is exercised, the distance between the previous and next TX strobe will always be greater or equal to the normal period.
CLK0–2	Register settings for receive bit clock rates. **CLK2 CLK1 CLK0 BIT RATE (KHz)** 0 0 0 1.2 0 0 1 2.4 0 1 0 4.8 0 1 1 7.2 1 0 0 9.6 1 0 1 12.0 1 1 0 14.4 1 1 1 14.4 Register settings for transmit bit clock rates. **CLK2 CLK1 CLK0 BIT RATE (KHz) MD3=0 MD3=1** 0 0 0 1.2 1.2 0 0 1 2.4 2.4 0 1 0 4.8 4.8 0 1 1 7.2 7.2 1 0 0 9.6 9.6 1 0 1 0.6 12.0 1 1 0 0.3 14.4 1 1 1 0.075 14.4
TR0, TR1	These two bits select the transmit signal according to the following table. **TR1 TR0 SIGNAL SELECTED** 0 0 Normal (Transmit Signal) 0 1 Transmit Squelch 1 0 AUXTX 1 1 Loopback (Loop 4)
AL0, AL1	Loop 4 gain control **AL1 AL0 GAIN** 1 1 –6 dB 0 0 0 dB 0 1 6 dB 1 0 15 dB

CR2 Register: Address 0111

TRL 0–3	Determines transmit level according to the following table. RL3 TRL2 TRL1 TRL0 GAIN 0 0 0 0 0 dB 0 0 0 1 –1 dB 0 0 1 0 –2 dB 0 1 0 0 –4 dB 1 0 0 0 –8 dB
TR3	This bit controls the TX attenuator input mux. TR3 = 1 Normal Mode. Connects Transmit Output to the Attenuator. TR3 = 0 Connects AUXTX to the attenuator
HYEN	Enables hybrid HYEN= 1 Enabled HYEN= 0 Disabled
G0, G1	Determines programmable gain at the input of the RX filter after the adaptive hybrid. This gain will be set by evaluating the energy at the output of the adaptive hybrid and setting the gain based on the maximum receive signal level (–12 dBm). G1 G0 GAIN 0 0 0 dB 0 1 6 dB 1 0 12 dB 1 1 18 dB
LP3	Loop 3 control bit. When this bit is set, the transmit signal is looped back to the receiver. LP3= 1 Loop 3 Activated LP3= 0 Loop 3 Deactivated
SQEC	This bit squelches the echo component from the echo summer sample-and-hold. SQEC = 1 Squelch Echo Path SQEC = 0 Enable Echo Path
ENEC	This bit enables and disables the echo canceller. In half-duplex two wire, or full-duplex four wire modes, the echo canceller can be disabled. In such a case, the receive reconstruction filter will be bypassed and both inputs to the echo summer sample-and-hold will be grounded. ENEC = 1 Enable Echo Canceller ENEC = 0 Disable Echo Canceller
ENAH	This bit controls the transfer of the digitized hybrid error signal through the serial interface. ENAH = 1 Enable Data Transfer ENAH = 0 Disable Data Transfer When ENAH and ENEC are both zero, no data will be transferred and the echo ADC will be disabled.

CR3 Register: Address 1000

ALC0, ALC1

These bits control the audio output levels. A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker.

ALC1	ALC0	AUDIO OUTPUT LEVEL ATTENUATION
0	0	Squelch
0	1	12 dB
1	0	6 dB
1	1	0 dB

MD0–MD3

Mode Select bits. These bits control the mode operation according to the following table.

MD3	MD2	MD1	MD0		MODE
1	1	1	1	Voice	TXSTRB & RXSTRB frequencies change to 8 kHz for voice processing
1	X	X	X	Normal	Normal Mode
0	1	1	1	V.23 FC	V.23 Forward Channel
0	1	1	0	V.23 BC/CPM	V.23 Backward Channeled Call Progress Mode
0	1	0	1	103A	103 Answer Mode
0	1	0	0	103O	103 Originate Mode
0	0	1	1	V.22A	V.22 and V.22 bis Answer Mode
0	0	1	0	V.22O	V.22 and V.22 bis Originate Mode
0	0	0	1	V.21A	V.21 Answer Mode
0	0	0	0	V.21O	A.21 Originate Mode

V.22A Mode—This mode supports band split answering modems that operate according to the CCITT V.22 and V.22 bis recommendations. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a low-band filter with a pass band range of 300–1600 Hz.

V.21A Mode—This mode supports a band split answering modem that operates according to the CCITT V.21 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a low-band filter with a pass band range of 300–1280 Hz.

V.22O Mode—This mode supports bandsplit originating modems that operate according to the CCITT V.22 and V.22 bis recommendations. In this mode the receive and transmit signals are separated by passing the composite signal though the receive filter which is configured as a band-pass filter with pass band edges extending from 2000–3200 Hz.

V.21O Mode—This mode supports a band split originating modem that operates according to the CCITT V.21 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a band-pass filter with pass band edges extending from 1600–2560 Hz.

V.23 BC/Call Progress mode (CPM)—In these modes the clock of the receive low-pass filter is reduced by a factor of 5. This moves the pass band edge to 640 Hz. The low-pass and high-pass filters form a band-pass which extends from 300–640 Hz and rejects the V.23 forward channel signal. This filter and the energy detect can be used for call progress monitoring.

V.23FC Mode—In this mode the clock of the receive V.22b bis high-pass filter is reduced to 57.6 kHz. This moves the pass band edge down to 1000 Hz. The low-pass and high-pass filters form a band pass which extends from 1000–3200 Hz. This filter passes the V.23 forward channel and rejects the backward channel.

103A Mode—This mode supports band split answering modems that operate according to the Bell 103 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a low-band filter with a pass band range of 300–1600 Hz.

103O Mode—This mode supports a band split originating modem that operates according to the Bell 103 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a band-pass filter with pass band edges extending from 2000–3200 Hz.

Normal mode—In this mode the receive filter consisting of the low-pass/high-pass combination form a band-pass which extends from 300–3200 Hz. This mode supports modems that operate according to the CCITT V.26, V.27, V.27 ter/bis, V.29, V.32, V.32bis and V.33 recommendations. It can also be used for voice processing.

NOTE 1: In all the above modes, the echo canceller can still be operational and the filtered signal can go through the reconstruction filter unless it is independently disabled by the (ENEC) bit.

NOTE 2: In the Bell 103 and V.21 modes the receive signal should be sampled by a free running RxSTRB at the specified rate. This can be achieved by putting the RxDPLL in the free run mode. The TxDPLL should be placed in the free run mode due to the same reason.

TXFC	Transmit filter clock control. This bit controls the clock frequency for the transmit low-pass filter. If MD3=0, MD2=X, MD1=X, MD0=0 and TxFC=1 the transmit filter clock is cut to 1/2 of its nominal value. This moves the pass-band edge from 3.2 kHz to 1.6 or 1.28 kHz. In V.22/V.21/103 modes when the modem is set to operate as the originating modem the low-pass filter will clean the transmit spectrum in the high-band region. It is important to note that the transmit low-pass filter has a x/sin(x) shape in the pass band which is optimized for a 9.6 kHz sampling rate. If the clock frequency is cut into half, the x/sin(x) compensation will correspond to a 4.8 kHz sampling rate. This will put an additional 1 dB slope in the pass band of the low band signal. TXFC=1 TX filter clock cut into half TXFC=0 Normal operation (The above condition is only valid when the modem operates in the originating mode.)
NI	This bit (Notch Insert) controls the insertion of the 1800/550 Hz notch in the V.22 bis and answer mode. NI = 1 Notch Inserted NI = 0 Notch Bypassed
NSEL	This bit (Notch Select) selects the frequency of the notch. NSEL = 1 1800 Hz NSEL = 0 550 Hz
TEST1	This bit puts the chip in the test mode. When activated, the transmit sample-and-hold will be disconnected from the 12-bit DAC and will be connected to the output of the receive antialiasing filter. TEST1 = 1 Activate Test Mode TEST1 = 0 Deactivate Test Mode
TEST2	This bit activates a S/H circuit that is connected to the TX DAC output and is strobed by the TX STRB. This mode makes the output of the TX DAC accessible from outside and can be used to calibrate the 12-bit DAC. TEST2 = 1 Activate Test Mode TEST2 = 0 Deactivate Test Mode When the test mode is deactivated, the input of the S/H will be connected to ground.
TEST3	This bit activates a test mode which allows the testing of SCF2. In this mode, the input of SCF2 is connected to the output of the receive antialiasing filter and the output can be monitored at pin C1. TEST3 = 1 Activate Test Mode TEST3 = 0 Deactivate Test Mode

Transmit Serial Out Interface

This block converts the digital output of the 12-bit echo cancelling ADC to 16-bit serial words. Data transmission will start with a pulse on SOENT pin within 1 µsec after the falling edge of TxSTRB signal. A 16-bit word will be shifted out on the rising edges of SCLK, the 12 MSBs correspond to echo sample. This will be followed by another pulse on SOENT pin and a second 16-bit word corresponding to adaptive-hybrid output sample. The latter will not be generated if adaptive-hybrid is disabled (ENAH=0). If echo canceller is disabled there will not be any output on this port. Figure 15 shows the timing diagram of transmit serial output, with values specified in Table 1. The bit structure of output words are shown below:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT
EB11	EB10	EB9	EB8	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	—	—	—	—	ECHO Error Sample
HB11	HB10	HB9	HB8	HB7	HB6	HB5	HB4	HB3	HB2	HB1	HB0	SV4	SV3	SV2	SV1	AH Error Sample

EB0–11	12-bit 2's complement data representing the echo error sample. EB11 is the sign bit.
HB0–11	12-bit 2's complement data representing the error output from the adaptive hybrid. HB11 is the sign bit.
SV1–SV4	Sign of the signals V1–V4 sampled at the transmit strobe. SVi = 0 Vi Positive SVi = 1 Vi Negative

NOTE: MSB (D15) is shifted out first in time. The output digital words correspond to the samples taken on the falling edge of previous TxSTRB signal.

Receive Serial IN Interface

This block accepts 16-bit serial words consisting of address and control bits. MSB is the address bit and identifies one of the two internal registers. Following a pulse on SIENR, the data one SIR pin will be shifted in on the falling edges of SCLK (with MSB first in time) as shown in Figure 16a. The timing requirements are given in Table 3. When updating PGCR register the timing of Figure 16b should be followed which will result in implementation of new gain value on the next falling edge of RXSTRB.

The bit structure of receive serial input interface is shown below and is followed by bit definitions.

REG. NAME	ADD. BITS	CONTROL BITS														
	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PGCR	0	DPLL2	DPLL1	DPLL0	RDPF	RDPR	RDPA	PGC6	PGC5	PGC4	PGC3	PGC2	PGC1	PGC0	—	—
LVLR	1	—	—	—	—	—	—	—	—	—	RxST	RSINT	LV1	LVO	—	—

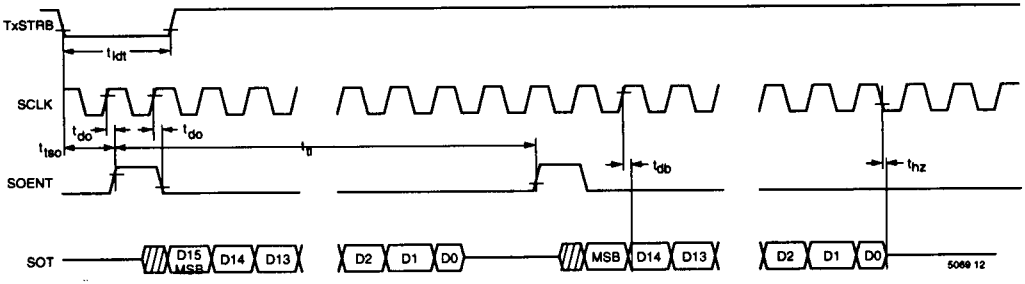


Figure 15. Tx Serial Output Timing With Respect to TxSTRB (For Echo/AH A/D)

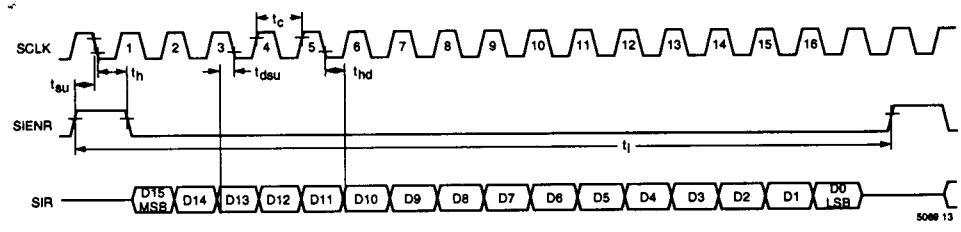


Figure 16a. Rx Serial Input Timing

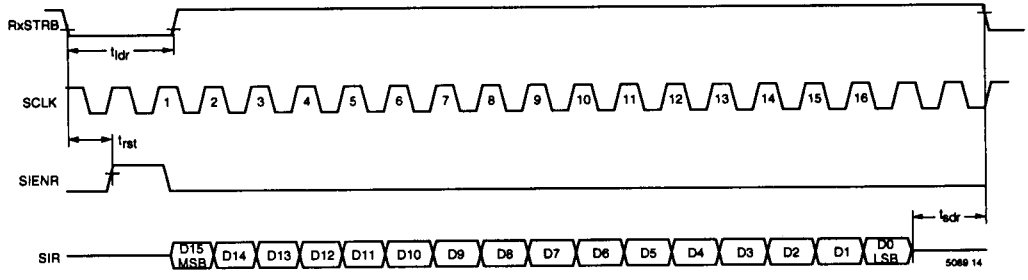


Figure 16b. Rx Serial Input Timing With Respect to RxSTRB (For Rx PGC Register)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{su}	Set up time from SIENR high to SCLK low	80			ns
t_h	Hold time from SCLK low to SIENR low	50			ns
t_{hd}	Hold time from SCLK low to SIR transition	50			ns
t_{dsu}	Data set up time from SIR valid to SCLK low	80			ns
t_i	Interval between consecutive SIENR pulses	6.0			µs
t_{ldr}	Low duration of RxSTRB	.2		102	µs
t_{rst}	Set up time from RxSTRB low to SIENR high	0		92	µs
t_{sdr}	Delay time from last input data to RxSTRB low	0			ns
t_{rso}	Delay time from RxSTRB low to SOENR high	60		425	ns
t_{do}	Delay time from SCLK high to SOENR high			100	ns
t_{db}	Delay time from SCLK high to SOR valid			100	ns
t_{hz}	Hold time from SCLK low to SOR high impedance	50			ns
t_c	Serial clock period		325		ns

Table 3. Timing Requirements for Rx Serial Input/Output Interfaces

PGCR Register:

PGC0–PGC6

These bits control the programmable gain stage according to the following table:

PGC6	PGC5	PGC4	PGC3	PGC2	PGC1	PGC0	GAIN (dB)
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	.375
0	0	0	0	0	1	0	.75
0	0	0	0	1	0	0	1.5
0	0	0	1	0	0	0	3
0	0	1	0	0	0	0	6
0	1	0	0	0	0	0	12
1	0	0	0	0	0	0	24

RDPA, RDPR, RDPF

These bits control the receive DPLL as follows:

RDPA = 1 Advance Phase by Inserting Pulse(s)
RDPA = 0 No Operation
RDPR = 1 Retard Phase by Deleting Pulse(s)
RDPR = 0 No Operation
RDPF = 1 Fast Correction Mode
RDPF = 0 Slow Correction Mode

In slow correction mode, only one pulse (217 ns) will be inserted or deleted (per RDPA and RDPR state), whereas in fast mode the phase correction will be 8 times faster. Bits RDPA and RDPR will reset automatically after performing their correction.

DPLL0–2

These bits determine the mode of operation for receive DPLL. When all three are zero, then, DPLL will be controlled by RDPA, RDPR and RDPF bits. If any of DPLL0–2 bits is one, then, register bits RDPA, RDPR and RDPF will be ignored and DPLL will enter the coarse mode where its operation is determined according to the following table:

DPLL2	DPLL1	DPLL0	OPERATION
0	0	0	See RDPA, RDPR, RDPF bits
0	0	1	Delete 16 pulses
0	1	0	Delete 32 pulses
0	1	1	Delete 64 pulses
1	0	0	Delete 128 pulses
1	0	1	Delete 256 pulses
1	1	0	Delete 512 pulses
1	1	1	Delete 1024 pulses

LVLR Register:

LVL1

The contents of these registers set the carrier detect level threshold.

LVL1	LVL0	Off-to-On	On-to-Off
0	0	–43 dBm	–48 dBm
0	1	–33 dBm	–38 dBm
1	0	–26 dBm	–31 dBm
1	1	–16 dBm	–21 dBm

RSINT

This bit determines whether the RX strobe is generated internally or supplied externally.

RSINT = 1 Internal
RSINT = 0 External

In the external mode the RX DPLL will be disabled and the RXCLK will go to a high or low state.

RXST

Determines the rate of receive strobe. (See the section corresponding to MD0–MD3.)

RXST = 1 9.6 kHz
RXST = 0 7.2 kHz

Receive Serial Out Interface

This block generates a 13-bit serial word on SOR pin, following a pulse on SOENR pin. Data is shifted out on the rising edges of the shift clock as shown in Figure 17 which also illustrates the relationship with strobe. Timing specifications are given in Table 3. The bit structure of output word and their definition is as follows:

D12 (MSB)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	ED

ED	This bit indicates the status of energy detect circuit. ED = 1 Energy Detected ED = 0 Energy not Detected
RD0–11	12-bit, 2's compliment data representing the receive signal sample. RD11 is the sign bit.

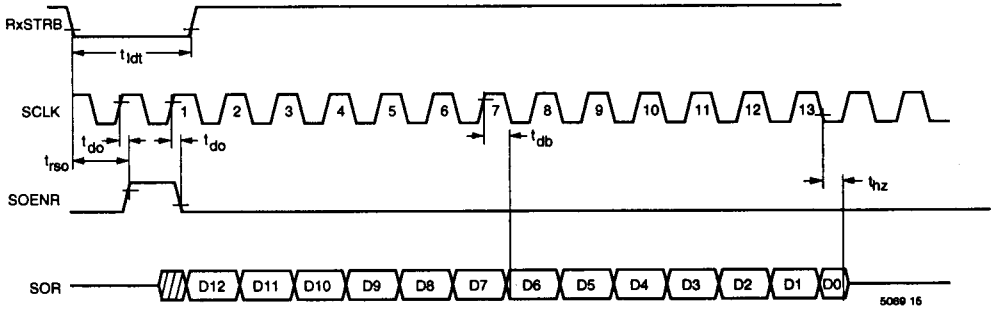


Figure 17. Rx Serial Output Timing With Respect to RxSTRB (For Rx A/D)

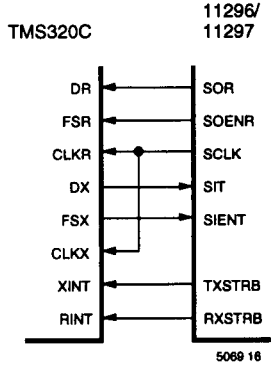


Figure 18. Interface to TMS320C25

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{DD}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS} – 0.6 to V_{DD} + 0.6 V
DC Input Voltage (Digital Signals)	V_{SS} – 0.6 to V_{DD} + 0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Unless otherwise specified, all voltages are referenced to ground.
NOTE 3: Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{DD}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
MCLK	Clock Frequency		9.2151	9.2160	9.2169	MHz
T_R, T_F	Input Rise or Fall Time	All Digital inputs except MCLK			50	ns
T_R, T_F	Input Rise or Fall Time	MCLK			30	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = +5 V ± 10 %, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Quiescent Current			25	50	mA
I_{SS}	Quiescent Current			25	50	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
V_{OM}	Maximum Peak Output Level on TxOUT Pin	R_L = 1 kΩ	±2.5			V
V_{IM}	Maximum Peak Output Level on RxIN Pin				±2.5	V

Powerup sequence: To prevent the device from going into latch up at power-up, theTXV_{SS} plus RXV_{SS} voltage must be available before the DV_{SS} voltage.

Appendix A
Applications Aspects of the Adaptive Hybrid

Overview

An adaptive hybrid has been devised to significantly attenuate the near-end echoes. For example, Figure A.1 shows how the adaptive hybrid fits into a V.32bis modem. A four stage correction network provides versatile correction of echoes with various characteristics. The echo reduction, by this network, consistently exceeds 20 dB, and is higher in most cases. In the V.32bis modem application, this echo reduction makes it feasible to provide high performance without requiring the following:

1. A precision (14-bit) ADC.
2. 24-bit digital words in part of the echo canceller.

By reducing the echo by about 20 dB in the worst case, the word accuracy requirements are reduced by about 4 bits.

Correction Network

Figure A.2 shows the correction network without the learning. The four a's are learned during training. Then, in the V.32bis modem, t h e a's are fixed, although they could adjust continually in some applications.

The following shows the basis of the correction. Let the echo path characteristic be $R(\omega) + jI(\omega)$. Each corrector stage has a characteristic $R_n(\omega) + jI_n(\omega)$. The overall corrector has the characteristic $R_C(\omega) + jI_C(\omega)$, where:

$$R_C(\omega) = \alpha_0 + \alpha_1 R_1(\omega) + \alpha_2 R_2(\omega) + \alpha_3 R_3(\omega) \quad \text{A2.1}$$

$$I_C(\omega) = \alpha_1 I_1(\omega) + \alpha_2 I_2(\omega) + \alpha_3 I_3(\omega) \quad \text{A2.2}$$

The objectives are to:

1. Select RC values for the individual stages such that various realistic echoes can be corrected.
2. Adapt to each echo path by selecting the a's to obtain $R_C(\omega) \approx R(\omega)$ and $I_C(\omega) \approx I(\omega)$.

The versatility is indicated by Equations A2.1 and A2.2, which show that we can exactly obtain any two desired points on each of the curves $R(\omega)$ and $I(\omega)$, although this would be generally suboptimum. The smoothness of all curves involved indicates that we can obtain fairly accurate approximations of the realistic characteristics.

One recommendation for the RC values are:

$R_1C_1 = 50$ µsec;
$R_2C_2 = 20$ µsec; and
$R_3C_3 = 150$ µsec.

These RC selections were based upon trade-offs involving the following conflicting considerations. The capability to correct echo paths with large bends in the frequency domain characteristics can be enhanced by using stages that have large bends in their characteristics. Also, the stages need to substantially differ from each other to enhance versatility and to avoid excessive inter-stage inter-dependence in learning. Further, to avoid implementation complexity, it is desirable to constrain the a values to $-1<\alpha_n<1$. All of these considerations call for large RC values as well as using one high-pass stage and two low-pass stages. However, when the echo path frequency domain characteristic has small bends, these characteristics can be more accurately matched by stages with small RC values. The RC values were selected to enable us to meet the various objectives, including coverage of wide ranges and shapes of characteristics without using excessive RC values, which would degrade performance against moderately distorted echoes.

After preliminary estimates, we refined the RC selection by computer. First we selected some approximately worst case echo paths, which are typified by:

1. Large bends in the curves $R(\omega)$ and $I(\omega)$
2. Large ratios of $I(\omega)$ and $R(\omega)$

Then, we tried combinations of RC values to obtain a set of values that is approximately optimum, considering the stated objectives.

The Algorithm for Learning

Figure A.2 shows the meaning of symbols below. In a simple version of the learning, each coefficient, α_n,

$$(\Delta\alpha)_{m,n} = k\, E_m\, \mathrm{Sgn} V_n = \pm k\, E_m \quad \text{A3.1}$$

$$\alpha_{m,n} = \alpha_{m-1,n} + (\Delta\alpha)_{m,n} \quad \text{A3.2}$$

Where

m refers to the mth sample;
E_m = output Error;
k = constant; and
V_n = nth stage signal at input α_n.

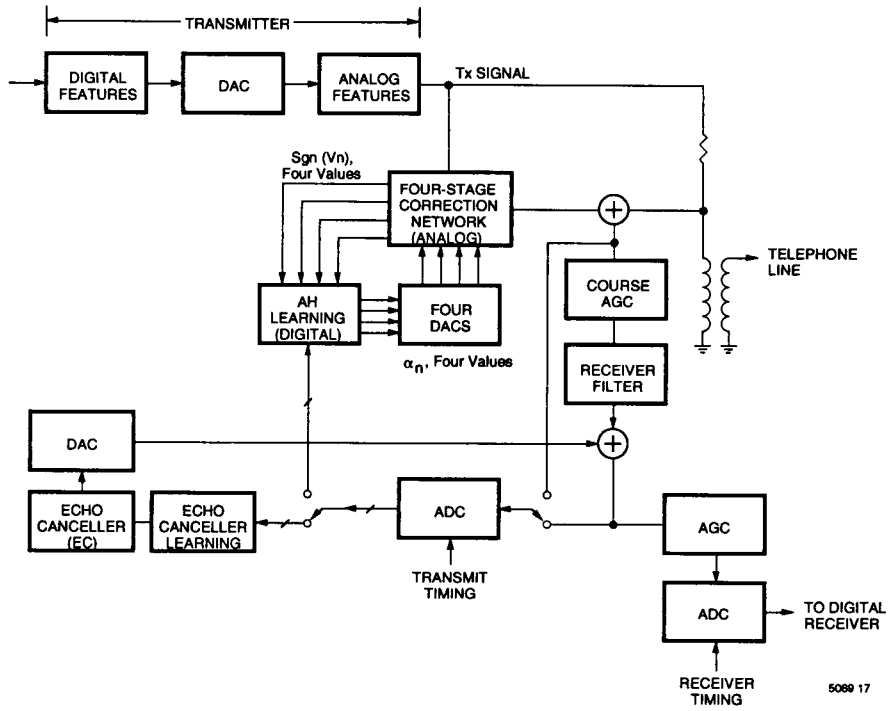


Figure A.1. Overview of Adaptive Hybrid and How it Fits Into A V.32 Modem

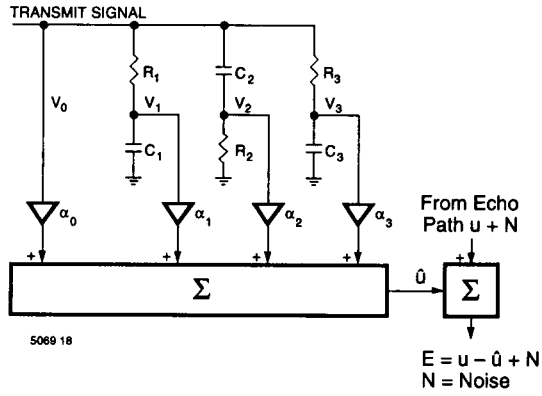


Figure A.2. Correction Network

is updated once each sample time as follows:

If U_m represents the mth echo sample, and $\hat{U}_m$ is the echo correction sample, and N_m is random noise, we have:

$$E_m = U_m - \hat{U}_m + N_m = U_m - \Sigma(a_{m,n} V_n) + N_m \qquad \text{A3-3}$$

For voiceband channels, practical sampling rates are in the range of 7200 to 9600 sps. Initially, $\alpha_0 = 0.5$, $\alpha_n = 0$ for n = 1–3 in the simplest case.

Let q_p be the optimum α_p, then neglecting noise,

$$E_m \, Sgn(V_n) = \sum_{p} [(q_p - \alpha_{m,p}) V_p] \, Sgn(V_n) \qquad \text{A3-4}$$

For the case of p = n, $V_n Sgn(V_n)$ is always positive. In the case of a random data signal for example, the effects of terms where $p \neq n$ tend to average to near zero. Thus, the $(q_n - \alpha_{m,n})V_n Sgn(V_n)$ always tries to drive α_n in the direction to reduce $(q_n - \alpha_n)$, and from Equation A.1, Δa has the right polarity to reduce the error most of the time. Since the increments, the $[\Delta\alpha]$, are very small, each α is driven generally in the correct direction, although a small percentage of the increments will be in the wrong direction.

If we had used V_n instead of $Sgn(V_n)$, this algorithm would have closely resembled the "Least-Mean-Square", LMS, algorithm often used for adaptive equalization and echo cancellation. For any particular E_m, at an arbitrary stage of the learning process, $E_m Sgn(V_n)$ will have the same polarity as $E_m V_n$. Therefore, at any particular error value, E_m, the proposed algorithm drives each α_n in the same direction as the LMS algorithm.

From Figure A.1 we see that use of the $\{Sgn(V_n)\}$ instead of the $\{V_n\}$ eliminates the need for four ADCs that would otherwise be needed.

Actually, we use a refined version of the algorithm described above. This version is given by:

$$(\Delta a)_{m,n} = k_q \sum_{p=m}^{m-31} [E_p Sgn(V_{p,n})] \text{ for } m = 0, 4, 8, \text{ etc.}$$

Updating occurs once every four sample times and each update is based upon the last 32 values of $E_p Sgn(V_{p,n})$. This version improves each updating loop characteristic. Also, it reduces the digital word size requirement, compared to the simple version, because it allows the error E_m to become smaller before Δa becomes smaller than the least significant bit.

Also, instead of a constant, k_q is reduced once every 32 sample times as follows:

$$k_q = 0.05(0.96)^q, \; q = m/32$$

and m = 0 at the start of training. This procedure allows the training to proceed rapidly at first, then slow down for higher precision.

Adaptation Procedure

The following general procedure is recommended for training the Adaptive Hybrid (See Figure A.3):

1. Train the Adaptive Hybrid (AH) from the same signal as the Echo Canceller (EC). However, some coarse training of the AH from earlier signals (with only a few frequency components) can be considered.
2. Use the total time duration allowed for the EC training signal, 8192/2400 = 3.413 sec.
3. Start the AH training at the beginning of this signal and finish it at about the middle.
4. At the end of the AH training, freeze the coefficients and leave them frozen until the next train or retrain. It is better not to have both the AH and EC adapting during data reception. Also, the EC can finish the last (precise) part of its training better if the AH is not fluctuating concurrently.
5. Start the EC training about 0.4 seconds after the AH training starts.

During the AH and EC training, no signal from the far end is present; and no AGC action occurs. When signal from the far end arrives, the AGC that precedes the EC is coarsely trained while the EC is temporarily frozen. The EC adaptation continues after the AGC is trained. However, the AGC gain should be automatically considered in selecting the coefficients that determines the echo estimates.

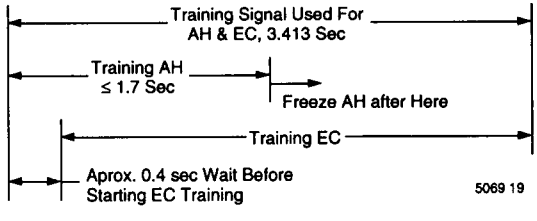


Figure A.3. AH & EC Training Procedure