BURST EDO DRAM MODULE

1, 2, 4 MEG x 64

8, 16, 32 MEGABYTE, 3.3V, BURST EDO

FEATURES

- 168-pin, dual-in-line memory module (DIMM)
- Buffered and non-buffered versions
- Burst EDO order, interleave or linear, programmed by executing WCBR cycle after initialization
- High-performance CMOS silicon-gate process
- Single +3.3V ±5% power supply
- All inputs and outputs are LVTTL-compatible with 5V input/output tolerance
- Refresh modes: $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) or $\overline{\text{RAS}}$ ONLY
- 1,024-cycle refresh (10 row-, 10 column-addresses) [MT4LD(T)164 B(N)]
  2,048-cycle refresh (11 row-, 10 column-addresses) [MT8LD264 B(N)]
  2,048-cycle refresh (11 row-, 11 column-addresses) [MT16LD464 B(N)]
- Four cycle Extended Data-Out (EDO) burst accesses

OPTIONS

OPTIONS	MARKING
• Timing	
52ns access; 15ns cycle	-52
60ns access; 16.6ns cycle	-60
70ns access; 20ns cycle	-70
• Components	
SOJ	D
TSOP (1 Meg x 64 only)	DT
• Packages	
168-pin DIMM (gold)	G
• Buffered Inputs	
Buffered	B
Non-Buffered	BN

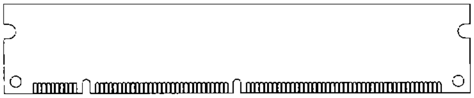
KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-52	90ns	52ns	15ns	25ns	10ns	5ns
-60	110ns	60ns	16.6ns	28.2ns	11.6ns	5ns
-70	130ns	70ns	20ns	35ns	15ns	5ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(BD-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ33	129	NC
4	DQ2	46	$\overline{\text{CAS4}}$	88	DQ34	130	$\overline{\text{CAS5}}$
5	DQ3	47	$\overline{\text{CAS6}}$	89	DQ35	131	$\overline{\text{CAS7}}$
6	Vcc	48	$\overline{\text{WE2}}$	90	Vcc	132	$\overline{\text{PDE}}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{\text{WE0}}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{\text{CAS0}}$	70	DQ26	112	$\overline{\text{CAS1}}$	154	DQ58
29	$\overline{\text{CAS2}}$	71	DQ27	113	$\overline{\text{CAS3}}$	155	DQ59
30	$\overline{\text{RAS0}}$	72	DQ28	11	NC	156	DQ60
31	$\overline{\text{OE0}}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC*/A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

*1 Meg x 64 version only

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT4LD164G-xx B	1 Meg x 64 Burst EDO, Buffered, SOJ
MT4LD164G-xx BN	1 Meg x 64 Burst EDO, Non-buffered, SOJ
MT4LDT164G-xx B	1 Meg x 64 Burst EDO, Buffered, TSOP
MT4LDT164G-xx BN	1 Meg x 64 Burst EDO, Non-buffered, TSOP
MT8LD264G-xx B	2 Meg x 64 Burst EDO, Buffered, SOJ
MT8LD264G-xx BN	2 Meg x 64 Burst EDO, Non-buffered, SOJ
MT16LD464G-xx B	4 Meg x 64 Burst EDO, Buffered, SOJ
MT16LD464G-xx BN	4 Meg x 64 Burst EDO, Non-buffered, SOJ

GENERAL DESCRIPTION

The MT4LD(T)164 B(N), MT8LD264 B(N) and MT16LD464 B(N) are randomly accessed 8MB, 16MB and 32MB solid-state memories organized in a x64 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20/21/22 address bits, which are entered 10/11 bits (A0 /B0-A10) at $\overline{RAS}$ time and 10/11 bits (A0/B0-A10) at $\overline{CAS}$ time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.

These DIMMs are burst access DRAM modules in which all READ and WRITE cycles occur in bursts of four. The bursts wrap around on a 4-byte boundary. This means only the two least significant bits of the $\overline{CAS}$ address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with $\overline{WE}$ LOW), with address A0/B0 set to either HIGH or LOW. A0/B0 LOW will program the device to execute linear bursts, A0/B0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information ($0010\ 000x_B$) where x=A0/B0 is supplied on addresses A7-A0/B0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle to exit this programming mode.

A READ or WRITE cycle is selected with the $\overline{WE}$ input during the first $\overline{CAS}$ LOW pulse of the burst. During the burst cycle the $\overline{WE}$ input must remain constant for the burst to continue. Transition of the $\overline{WE}$ input during a burst signals the burst to terminate and place the outputs in a High-Z state. After a terminated burst, the next falling edge of $\overline{CAS}$ will start a new burst access at the address present on the external address bus.

During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must be LOW prior to $\overline{CAS}$ going LOW. This places the input/output pins in the High-Z state allowing the data-in (D) to be driven on the bus. $\overline{WE}$ must remain LOW during the burst operation for it to complete. $\overline{WE}$ going HIGH after ^{t}WCH from $\overline{CAS}$ LOW or before ^{t}WCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the D/Q pins in the High-Z state.

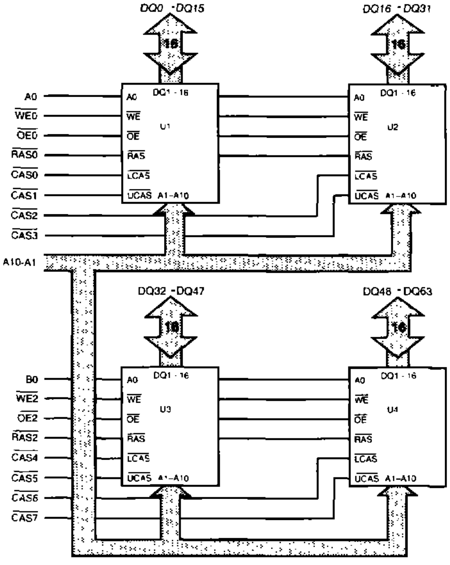
During a READ cycle $\overline{WE}$ must be HIGH prior to $\overline{CAS}$ going LOW. $\overline{WE}$ must remain HIGH during the burst operation for it to complete. $\overline{WE}$ going LOW after ^{t}RCH from $\overline{CAS}$ LOW or before ^{t}RCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the D/Q pins in the High-Z state.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next access during the $\overline{RAS}$ HIGH time.

WORD AND BYTE WRITEs

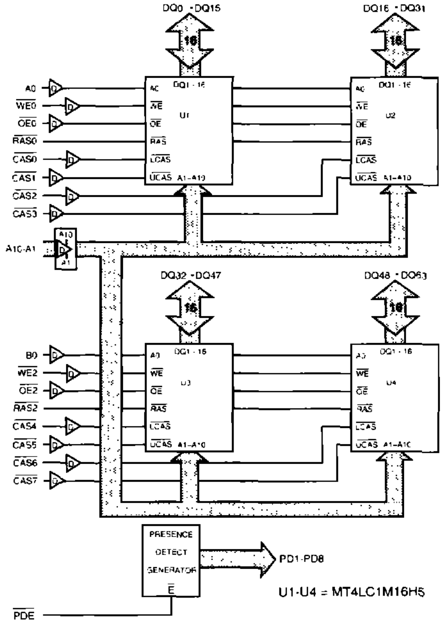
WORD WRITEs on the x16 Burst EDO DRAM based module [MT4LD(T)164] require $\overline{CAS0}$ with $\overline{CAS1}$ and $\overline{CAS2}$ with $\overline{CAS3}$ skew considerations that are not required on modules employing x4 and x8 Burst EDO DRAMs. BYTE WRITEs on the x16 based MT4LD(T)164 require special considerations when bursts are attempted. Refer to the MT4LC1M16H5 1 Meg x 16 Burst EDO DRAM data sheet for information on $\overline{CAS}$ to $\overline{CAS}$ skew requirements during WORD WRITE cycles and bursting BYTE WRITEs.

FUNCTIONAL BLOCK DIAGRAM MT4LD164 BN (8MB)



U1-U4 = MT4LC1M16H5

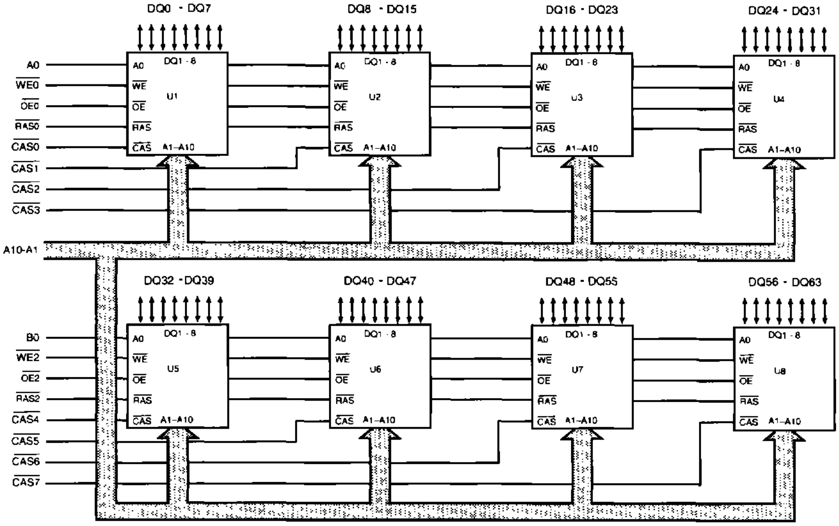
FUNCTIONAL BLOCK DIAGRAM MT4LD164 B (8MB)



U1-U4 = MT4LC1M16H5

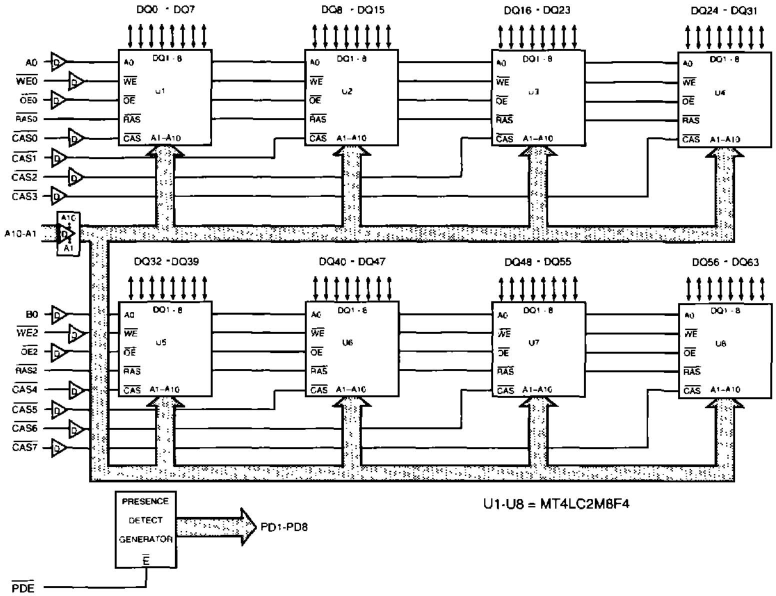
NOTE: 1. D = line buffers.

FUNCTIONAL BLOCK DIAGRAM
MT8LD264 BN (16MB)



U1-U8 = MT4LC2M8F4

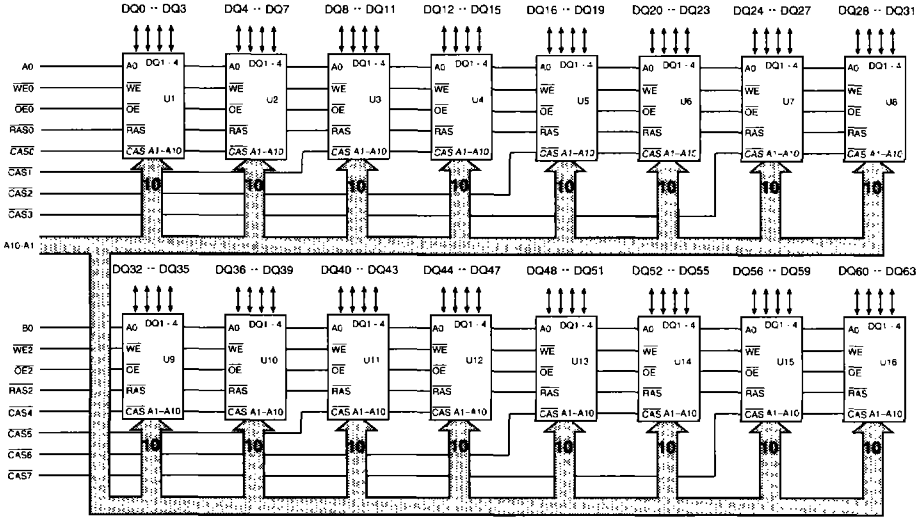
FUNCTIONAL BLOCK DIAGRAM
MT8LD264 B (16MB)



U1-U8 = MT4LC2M8F4

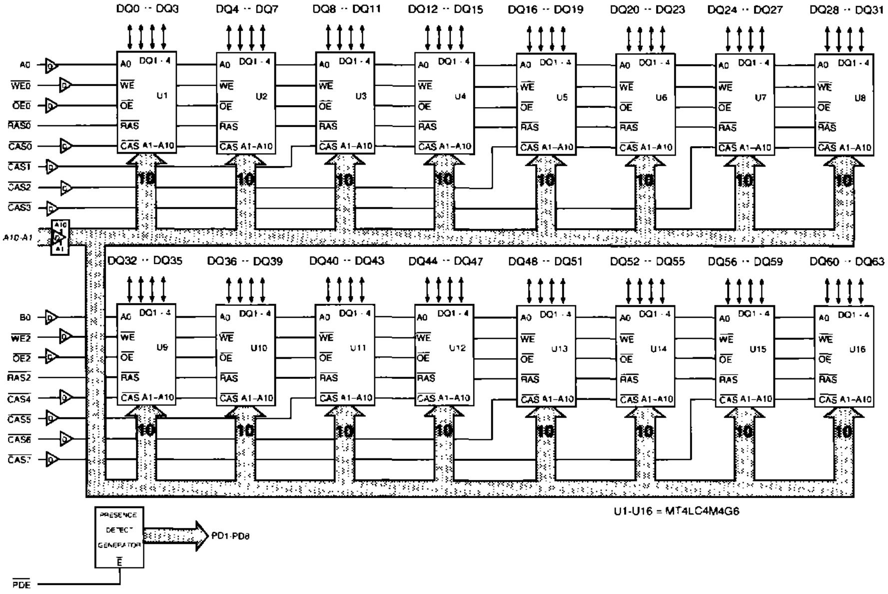
NOTE: 1. D = line buffers.

FUNCTIONAL BLOCK DIAGRAM
MT16LD464 BN (32MB)



U1-U16 = MT4LC4M4G6

FUNCTIONAL BLOCK DIAGRAM
MT16LD464 B (32MB)



U1-U16 = MT4LC4M4G6

NOTE: 1. D = line buffers.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10/11 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0}$-7	Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10/11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149, 151, 153-156, 158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either (1): NC (non-buffered) or driven to V_{OH} (buffered) or (0): V_{SS} (non-buffered) or driven to V_{OL} (buffered).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ± 5%
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	V_{SS}	Supply	Ground

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{\text{PDE}}$	Input	Presence-Detect Enable: $\overline{\text{PDE}}$ is the READ control for the buffered presence-detect pins. (B version only.)
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	—	No connect.

EDO BURST MODE TRUTH TABLE

						ADDRESSES		DATA
PRESENT STATE	RESULTING STATE	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row	Column	DQ0-63
Any	Idle	L→H	H	X	X	X	X	High-Z
Idle	Row Open	H→L	H	X	X	ROW	X	High-Z
Idle	CBR REFRESH	H→L	L	H	X	X	X	High-Z
Row Open	$\overline{\text{RAS}}$-ONLY REFRESH	L	H	X	X	ROW	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	COL	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	COL	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H→L	L	L	X	A0[1]	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H→L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE	L	H	X	X	ROW	X	High-Z

NOTE: 1. A WCBR *cycle determines the burst sequence.* A0/B0=LOW *sets the burst sequence to linear,* A0/B0=HIGH set the burst sequence to interleave. A8 through A10 are "don't cares." A7-A0/B0 should contain the sequence (0010 $000x_8$ where x=A0/B0) to ensure future compatability. A refresh cycle ($\overline{\text{RAS}}$ ONLY or CBR) must follow the WCBR cycle to exit the programming mode.

INTERLEAVE BURST SEQUENCE TABLE

	ADDRESSES USED		
OPERATION	**A9 - A2**	**A1**	**A0/B0**
First access, register external CAS address	A9 - A2	A1	A0/B0
Second access, (first burst address)	registered A9 - A2	registered A1	registered $\overline{\text{A0/B0}}$
Third access (second burst address)	registered A9 - A2	registered $\overline{\text{A1}}$	registered A0/B0
Fourth access (third burst address)	registered A9 - A2	registered $\overline{\text{A1}}$	registered $\overline{\text{A0/B0}}$

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X00	X..X11	X..X10
X..X10	X..X11	X..X00	X..X01
X..X11	X..X10	X..X01	X..X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72	10/9			0	1	0	0				
8MB	1 Meg x 64/72	10/9			1	1	0	0				
• 8MB	1 Meg x 64/72	10/10			0	0	1	0				
16MB	2 Meg x 64/72	10/10			1	0	1	0				
• 16MB	2 Meg x 64/72	11/10			1	0	0	1				
32MB	4 Meg x 64/72	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO / BEDO							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		52ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = Vss (non-buffered) or driven to V_{OL} (buffered); 1 = NC (non-buffered) or driven to V_{OH} (buffered).

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT16LD464 B(N) uses 11/11 DRAMs.

CAPACITANCE

		MAX							
		NON-BUFFERED			BUFFERED				
PARAMETER	SYM	8MB	16MB	32MB	8MB	16MB	32MB	UNITS	NOTES
Input Capacitance: A1-A10	C_{I1}	26	46	86	9	9	9	pF	3
Input Capacitance: $\overline{\text{WE0}}$, $\overline{\text{WE2}}$, $\overline{\text{OE0}}$, $\overline{\text{OE2}}$, A0, B0	C_{I2}	14	24	44	9	9	9	pF	3
Input Capacitance: $\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	C_{I3}	16	28	52	16	28	52	pF	3
Input Capacitance: $\overline{\text{CAS0}}$ - $\overline{\text{CAS7}}$	C_{I4}	8	8	12	9	9	9	pF	3
Input/Output Capacitance: DQ0-DQ63	C_{IO}	10	10	10	10	10	10	pF	3

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any I/O Pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs, NC or I/O pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 10W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.13	3.47	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5	V	2
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	2
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS7}$	I_{I1}	-4	4	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A1-A10	I_{I2}	-32	32	µA	
(All other pins not under test = 0V) for each package input	$\overline{WE0}$,2,$\overline{OE0}$,2	I_{I3}	-16	16	µA	
	$\overline{RAS0}$,2, A,B0	I_{I4}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

			MAX				
PARAMETER/CONDITION	**SYM**	**SIZE**	**-52**	**-60**	**-70**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB	8	8	8	mA	
		16MB	16	16	16		
		32MB	32	32	32		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8MB	2	2	2	mA	
		16MB	4	4	4		
		32MB	8	8	8		
OPERATING CURRENT: Closed Row Burst READ/WRITE Average power supply current; (${}^tPC$ = ${}^tPC$ [MIN]; 50% duty cycle on $\overline{RAS}$; Open Row, four Cycle Burst, Close Row)	I_{CC3}	8MB	600	560	520	mA	5
		16MB	880	800	720		
		32MB	1,760	1,600	1,440		
OPERATING CURRENT: Open Row Burst READ/WRITE Average power supply current (Alternating four cycle burst followed by four cycles of inactivity; ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	8MB	440	400	360	mA	5
		16MB	1,040	960	880		
		32MB	2,080	1,920	1,760		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current $\overline{CAS}$ = V_{IH}; ${}^tRAS$ = ${}^tRAS$ [MIN]; ${}^tRP$ = ${}^tRP$ [MIN])	I_{CC5}	8MB	760	720	640	mA	4
		16MB	1,200	1,120	1,040		
		32MB	2,400	2,240	2,080		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Cycling: ${}^tRAS$ = ${}^tRAS$ [MIN]; ${}^tRP$ = ${}^tRP$ [MIN])	I_{CC6}	8MB	680	640	600	mA	4, 6
		16MB	1,200	1,120	1,040		
		32MB	2,400	2,240	2,080		

NON-BUFFERED (BN) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - NON-BUFFERED		-52		-60		-70			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from CAS	^{t}AA		25		28.2		35	ns	12
Column-address setup time	^{t}ASC	1.5		1.5		1.5		ns	
Row-address setup time	^{t}ASR	1.5		1.5		1.5		ns	
Burst terminate hold time	^{t}BTH	3		3		3		ns	
Output disable from burst terminate	^{t}BTHZ	7	13	7	13	7	13	ns	13, 16
Access time from CAS	^{t}CAC		10		11		15	ns	
Column-address hold time	^{t}CAH	8.5		8.5		8.5		ns	
CAS pulse width	^{t}CAS	5	10,000	5	10,000	5	10,000	ns	
CAS0 and CAS1 or CAS2 and CAS3, etc. Coincident HIGH time	^{t}CCH	5		5		5		ns	25
CAS hold time (CBR or WCBR)	^{t}CHR	15		15		15		ns	6
CAS to output in Low-Z	^{t}CLZ	3		3		3		ns	13
Data Hold time from CAS LOW	^{t}COH	3		3		3		ns	
CAS precharge time	^{t}CP	5		5		5		ns	
CAS precharge time (CBR or WCBR)	^{t}CPN	10		10		10		ns	
CAS to RAS precharge time	^{t}CRP	10		10		10		ns	
CAS LOW to RAS HIGH (WRITE only)	^{t}CRW	15		16.6		20		ns	
Skew between CAS0 and CAS1 or CAS2 and CAS3, etc. (WRITE only)	^{t}CSK		2		2		2	ns	26
CAS setup time (CBR or WCBR)	^{t}CSR	10		10		10		ns	6
Data-in hold time	^{t}DH	5		5		5		ns	
Data-in setup time	^{t}DS	0		0		0		ns	27
Ouput Disable	^{t}OD	4	10	4	10	4	15	ns	13
Ouput Enable access time	^{t}OEA		10		12		15	ns	
Ouput Enable hold (only near CAS)	^{t}OEH	5		5		5		ns	
OE to output in Low-Z	^{t}OELZ	3		3		3		ns	13
OE HIGH pulse width	^{t}OEP	10		10		10		ns	
Ouput Enable setup (only near CAS)	^{t}OES	3		3		3		ns	
Output buffer turn-off delay	^{t}OFF	4	10	4	10	4	15	ns	13
Burst EDO cycle time	^{t}PC	15		16.6		20			
Access time from RAS	^{t}RAC		52		60		70	ns	
Row-address hold time	^{t}RAH	8.5		8.5		8.5		ns	
RAS pulse width	^{t}RAS	52	125,000	60	125,000	70	125,000	ns	
Random Read or Write cycle time	^{t}RC	90		110		130			
RAS to CAS delay time	^{t}RCD1	20		20		20		ns	
RAS to CAS delay time	^{t}RCD2	40		45		55		ns	
Read command hold time	^{t}RCH	5		5		5		ns	
Read command setup time	^{t}RCS	3		4		5		ns	
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
Refresh period (2,048 cycles)	^{t}REF		32		32		32	ms	

NON-BUFFERED (BN) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - NON-BUFFERED		-52		-60		-70			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{\text{RAS}}$ precharge time	^{t}RP	30		40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	5		5		5		ns	
$\overline{\text{RAS}}$ hold time	^{t}RSH	0		0		0		ns	
Transition time (rise or fall)	^{t}T	1.5	50	1.5	50	1.5	50	ns	
Burst Terminate pulse width	^{t}TP	6		6		8		ns	14
Write command hold time	^{t}WCH	5		5		5		ns	
$\overline{\text{WE}}$ command setup time	^{t}WCS	3		4		5		ns	
Ouput Disable from $\overline{\text{WE}}$ LOW	^{t}WHZ	4	10	4	10	4	15	ns	13, 16
$\overline{\text{WE}}$ hold time (CBR or WCBR)	^{t}WRH	10		10		10		ns	
$\overline{\text{WE}}$ setup time (CBR or WCBR)	^{t}WRP	10		10		10		ns	

BUFFERED (B) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - BUFFERED		-52		-60		-70			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from $\overline{\text{CAS}}$	^{t}AA		30		33.2		40	ns	12, 19
Column-address setup time	^{t}ASC	3.5		3.5		3.5		ns	17
Row-address setup time	^{t}ASR	6.5		6.5		6.5		ns	19
Burst terminate hold time	^{t}BTH	3		3		3		ns	
Output disable from burst terminate	^{t}BTHZ	9	18	9	18	9	18	ns	13,16,21
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		16		20	ns	19
Column-address hold time	^{t}CAH	13.5		13.5		13.5		ns	19
$\overline{\text{CAS}}$ pulse width	^{t}CAS	5	10,000	5	10,000	5	10,000	ns	
$\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$, etc. Coincident HIGH time	^{t}CCH	5		5		5		ns	25
$\overline{\text{CAS}}$ hold time (CBR or WCBR)	^{t}CHR	13		13		13		ns	6, 18
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	5		5		5		ns	13, 17
Data Hold time from $\overline{\text{CAS}}$ LOW	^{t}COH	5		5		5		ns	17
$\overline{\text{CAS}}$ precharge time	^{t}CP	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time (CBR or WCBR)	^{t}CPN	10		10		10		ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	15		15		15		ns	19
$\overline{\text{CAS}}$ LOW to $\overline{\text{RAS}}$ HIGH (WRITE only)	^{t}CRW	15		16.6		20		ns	
Skew between $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$, etc. (WRITE only)	^{t}CSK		2		2		2	ns	26
$\overline{\text{CAS}}$ setup time (CBR or WCBR)	^{t}CSR	12		12		12		ns	6,17
Data-in hold time	^{t}DH	10		10		10		ns	19
Data-in setup time	^{t}DS	0		0		0		ns	18, 27
Ouput Disable	^{t}OD	4	10	4	10	4	15	ns	13
Ouput Enable access time	^{t}OEA		15		17		20	ns	19
Ouput Enable hold (only near $\overline{\text{CAS}}$)	^{t}OEH	3		3		3		ns	18
$\overline{\text{OE}}$ to output in Low-Z	^{t}OELZ	8		8		8		ns	13, 19
$\overline{\text{OE}}$ HIGH pulse width	^{t}OEP	10		10		10		ns	
Ouput Enable setup (only near $\overline{\text{CAS}}$)	^{t}OES	3		3		3		ns	
Output buffer turn-off delay	^{t}OFF	6	15	6	15	6	20	ns	13, 21
Burst EDO cycle time	^{t}PC	15		16.6		20		ns	
$\overline{\text{PDE}}$ to valid presence-detect data	^{t}PD		10		10		10	ns	22
$\overline{\text{PDE}}$ inactive to presence-detect inactive	^{t}PDOFF	2		2		2		ns	23
Access time from $\overline{\text{RAS}}$	^{t}RAC		52		60		70	ns	
Row-address hold time	^{t}RAH	6.5		6.5		6.5		ns	18
$\overline{\text{RAS}}$ pulse width	^{t}RAS	52	125,000	60	125,000	70	125,000	ns	
Random Read or Write cycle time	^{t}RC	90		110		130		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD1	18		18		18		ns	18
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD2	38		43		53		ns	18
Read command hold time	^{t}RCH	7		7		7		ns	17
Read command setup time	^{t}RCS	5		6		7		ns	17
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
Refresh period (2,048 cycles)	^{t}REF		32		32		32	ms	

BUFFERED (B) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - BUFFERED		-52		-60		-70			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ precharge time	^tRP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	5		5		5		ns	
$\overline{RAS}$ hold time	^tRSH	5		5		5		ns	19
Transition time (rise or fall)	^tT	1.5	50	1.5	50	1.5	50	ns	
Burst Terminate pulse width	^tTP	6		6		8		ns	14
Write command hold time	^tWCH	10		10		10		ns	19
$\overline{WE}$ command setup time	^tWCS	5		6		7		ns	17
Ouput Disable from $\overline{WE}$ LOW	^tWHZ	6	15	6	15	6	20	ns	13,16,21
$\overline{WE}$ hold time (CBR or WCBR)	^tWRH	8		8		8		ns	18
$\overline{WE}$ setup time (CBR or WCBR)	^tWRP	12		12		12		ns	17

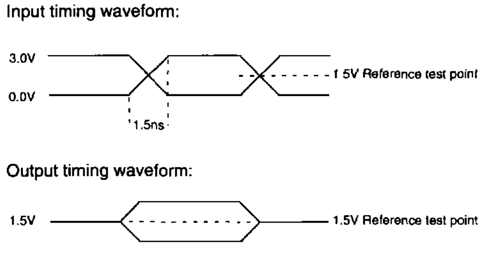


Figure 1
TIMING SPECIFICATIONS

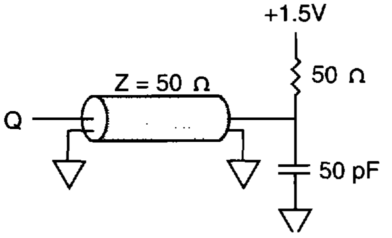


Figure 3
AC TIMING OUTPUT LOAD EQUIVALENT

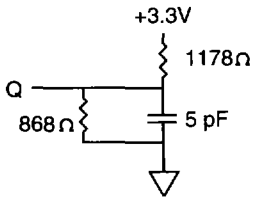


Figure 2
HIGH-Z OUTPUT LOAD

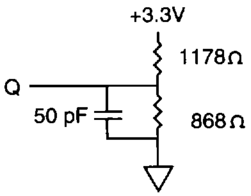


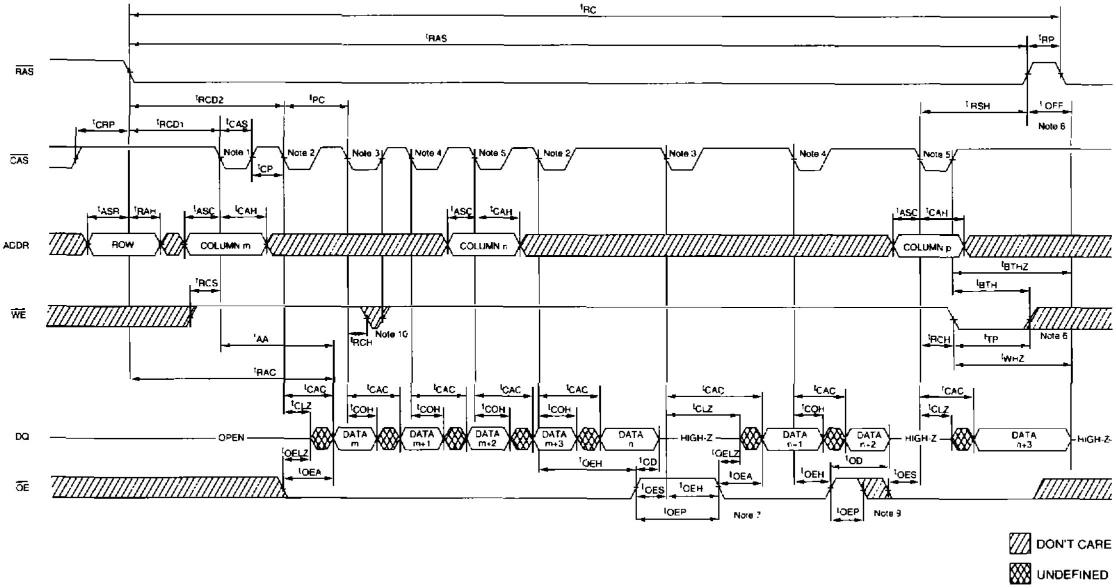
Figure 4
OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss.
2. Input Power-up: VIH ≤ +5.5V and Vcc ≤ +3.13V for t ≤ 200ms.
3. This parameter is sampled. Vcc = 3.3V ±5%; f = 1 MHz.
4. Icc is dependent on cycle rates.
5. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum ^{t}PC and 50 percent duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100µs after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded. A WCBR cycle must be executed to initalize the burst type, interleave or linear followed by a $\overline{\text{RAS}}$-ONLY or CBR REFRESH cycle.
8. AC characteristics assume ^{t}T = 1.5ns.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when AC specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. NC pins are assumed to be left floating and are not tested for leakage.
12. ^{t}AA is a calculated specification which is the sum of ^{t}PC and ^{t}CAC.
13. Output loading is specified with C_L = 5pF as in Figure 2. Transition is measured ±200mV from steady state voltage. These parameters are sampled.
14. Applies only during burst termination operation.
15. AC output loading is specified with C_L = 50pF as in Figure 3. Figure 4 is shown for reference. Transition is measured at the 1.5V reference level.
16. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
17. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
18. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.

19. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
20. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
21. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
22. Measured with the specified current load and 100pf.
23. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
24. B version only.
25. $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$, etc. HIGH pulse widths must be concurrently HIGH for at least this limit [MT4LD(T)164 B(N) module only].
26. The skew between $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$, etc. is required for WRITE cycles and is required only on the MT4LD(T)164 B(N) DIMM since it utilizes x16 Burst EDO DRAMs.
27. Valid data-in is referenced from when a valid logic level (V_{IH}, V_{IL}) is achieved.

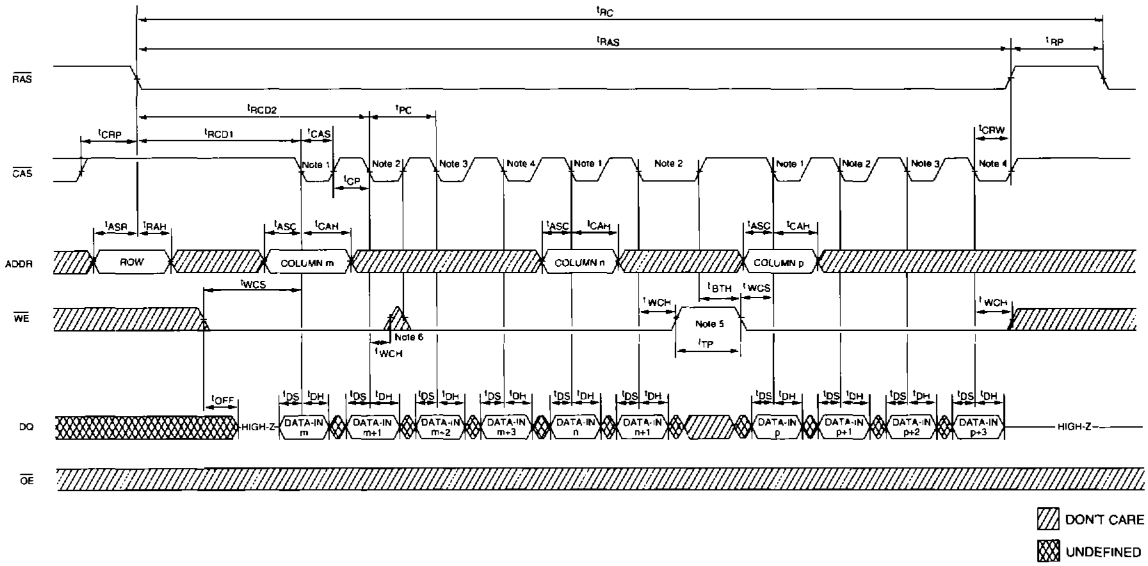
BURST EDO READ CYCLE



NOTE:

1. Latch column address; start READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start READ cycle.
6. $\overline{\text{WE}}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
7. Once $\overline{\text{OE}}$ transitions LOW after $\overline{\text{CAS}}$ transitions LOW, note 9 applies if $\overline{\text{OE}}$ transitions back HIGH.
8. The combination of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH close the row and place the DQs in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{\text{RAS}}$ or $\overline{\text{CAS}}$) that transitions HIGH.
9. When $\overline{\text{OE}}$ transitions HIGH, the DQ pins are placed in the High-Z state and will remain in the High-Z state until another $\overline{\text{CAS}}$ LOW transition occurs, regardless of the state of $\overline{\text{OE}}$.
10. $\overline{\text{WE}}$ transitioning LOW and returning HIGH prior to $\overline{\text{CAS}}$ going HIGH will not terminate the burst.

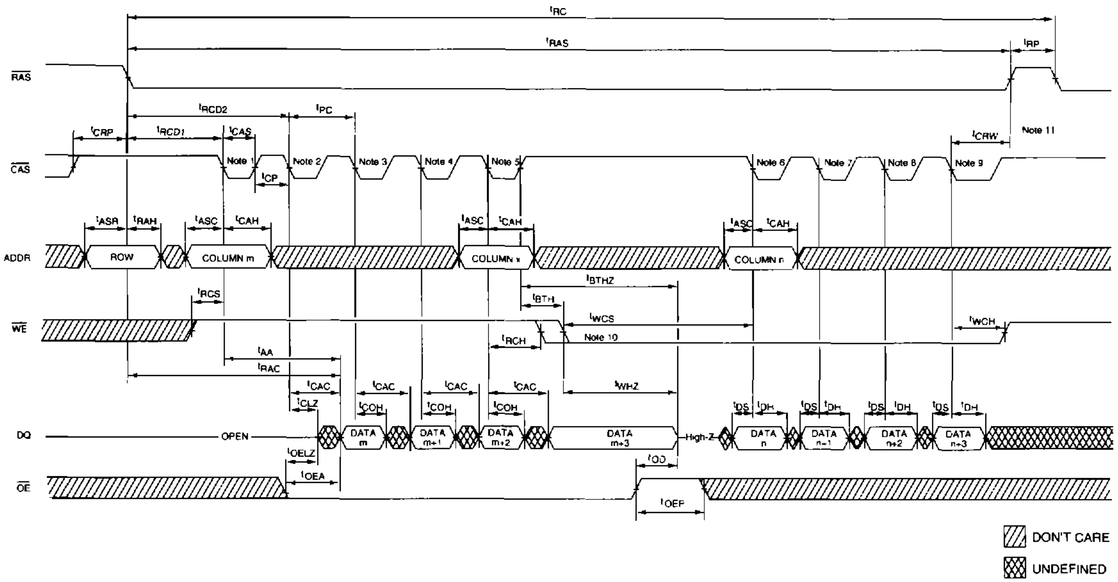
BURST EDO WRITE CYCLE



NOTE:

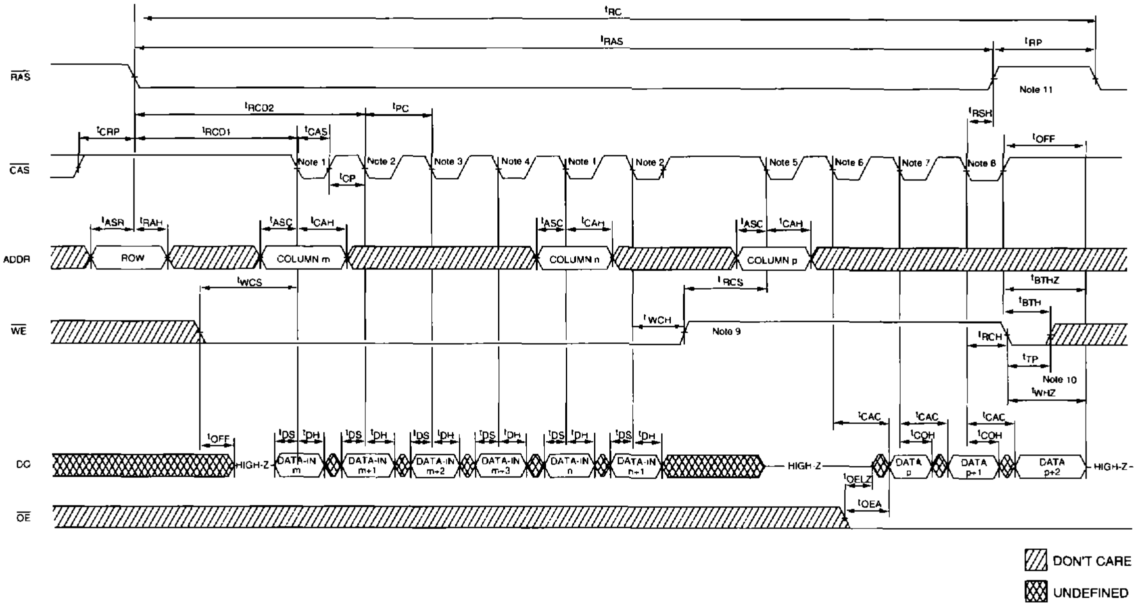
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. $\overline{\text{WE}}$ transitioning HIGH will terminate the burst and reset the burst counter provided tTP and tBTH are satisfied.
6. $\overline{\text{WE}}$ transitioning HIGH and returning LOW prior to $\overline{\text{CAS}}$ going HIGH will not terminate the burst.

BURST EDO READ/WRITE CYCLE



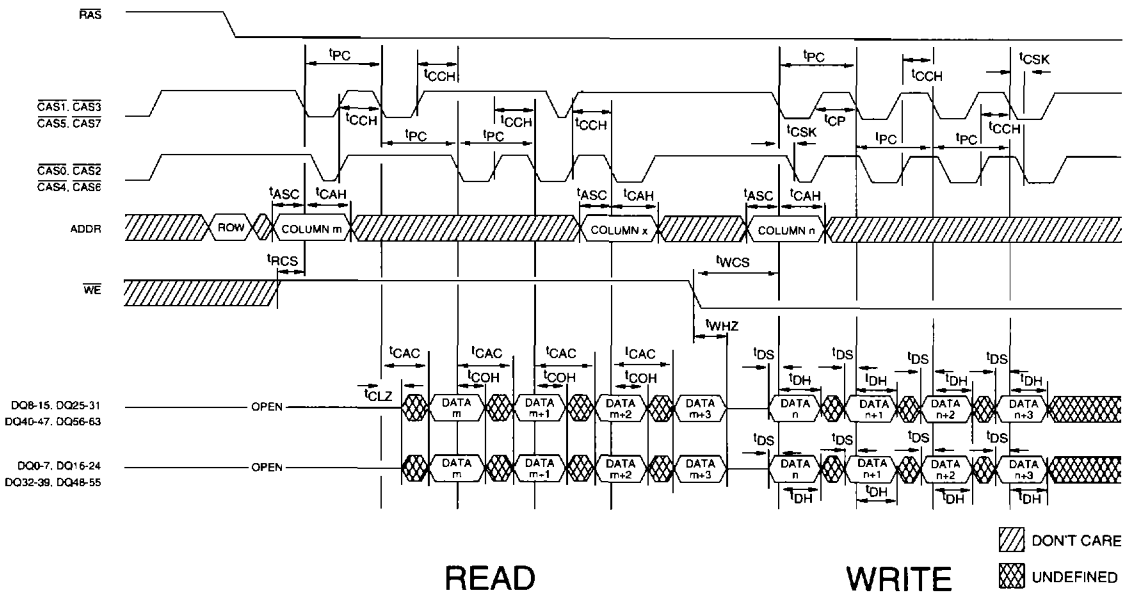
NOTE:
1. Latch column address; start burst READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start burst READ cycle.
6. Latch column address; start burst WRITE cycle; write data 1.
7. Increment burst counter; write data 2.
8. Increment burst counter; write data 3.
9. Increment burst counter; write data 4.
10. $\overline{\text{WE}}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. ^{t}TP is met by the READ burst being terminated by a WRITE burst. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
11. The combination of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH close the row and place the DQ pins in the High-Z state.

BURST EDO WRITE/READ CYCLE



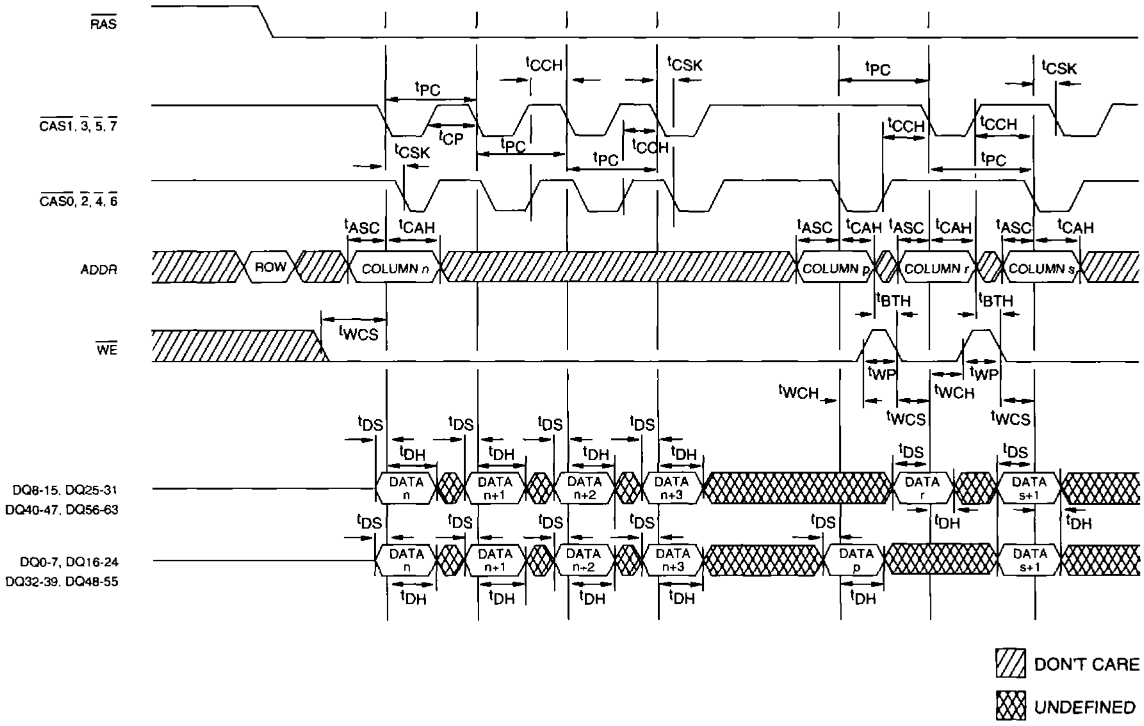
NOTE:
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. Latch column address; start burst READ cycle.
6. Output data 1; increment column address.
7. Output data 2; increment column address.
8. Output data 3; increment column address.
9. $\overline{\text{WE}}$ transitioning HIGH will terminate the burst and reset the burst counter. The ^{t}BTH time is not required as it is satisfied by ^{t}RCS; ^{t}TP is met by the WRITE burst being terminated by a READ burst.
10. $\overline{\text{WE}}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
11. The combination of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH close the row and place the DQ pins in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{\text{RAS}}$ or $\overline{\text{CAS}}$) that transitions HIGH.

BURST EDO
READ/WORD-WRITE CYCLE



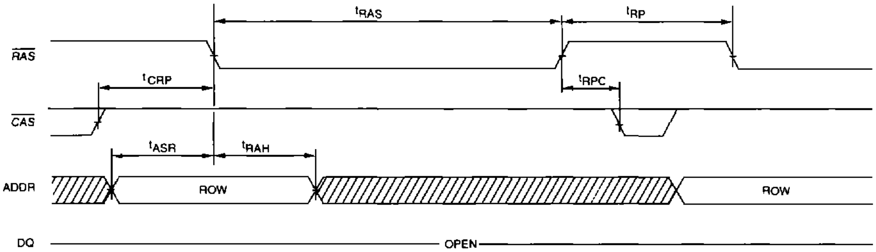
NOTE: 1. The $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ skew requirements apply to $\overline{\text{CAS}}$ lines common to the individual x16 DRAMs used on the MT4LD(T)164 B.

BURST EDO
WORD-WRITE/BYTE-WRITE CYCLE

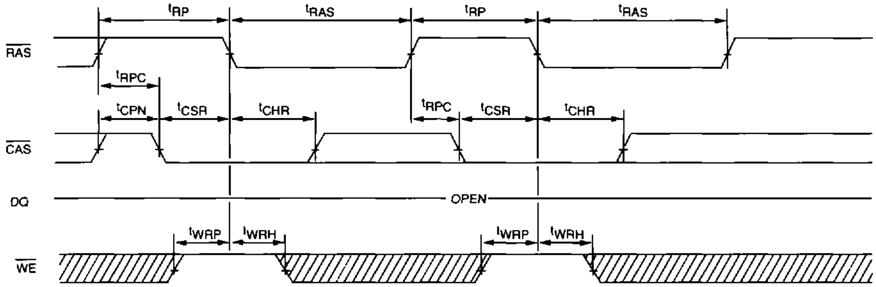


NOTE: 1. Applies to MT4LD(T)164 B(N) modules only.

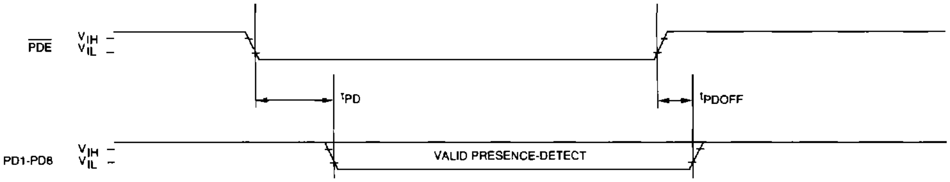
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



CBR REFRESH CYCLE



PRESENCE-DETECT READ CYCLE [24]

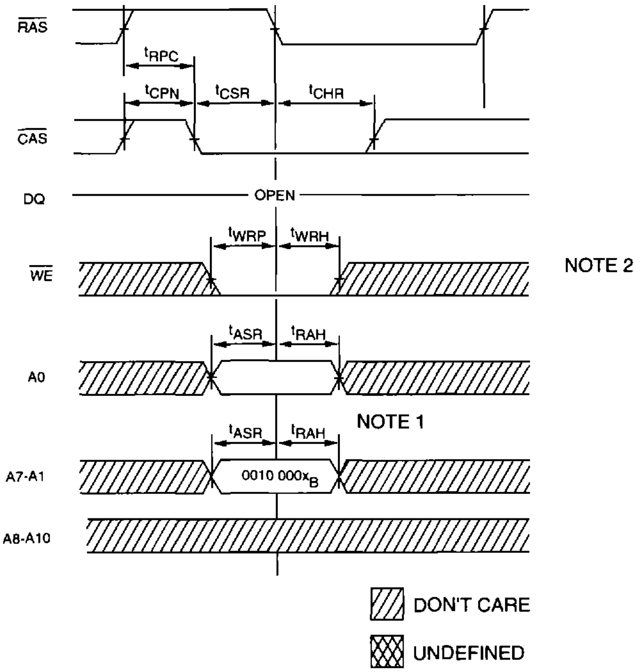


▨ DON'T CARE

▩ UNDEFINED

NOTE:
1. CBR REFRESH is recommended for all new designs to insure compatibility with future generation DRAMs. Micron and JEDEC recommend CBR REFRESH as the preferred method of refresh for the 64 Meg DRAM generation and beyond.
2. PD pins must be pulled HIGH at next level of assembly.

WCBR PROGRAM CYCLE



NOTE:
1. A0 LOW sets the burst sequence to linear bursts. A0/B0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are "don't cares." Addresses A7-A0 should contain the state of (0010 $000x_B$ where x=A0/B0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A $\overline{\text{RAS}}$-ONLY or CBR REFRESH cycle must be executed after the WCBR cycle to exit the programming mode.