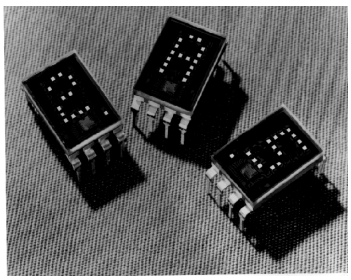
4N51, 4N52, 4N53, 4N54

Glass/Ceramic Numeric and Hexadecimal Displays for Industrial Applications

Data Sheet



Description

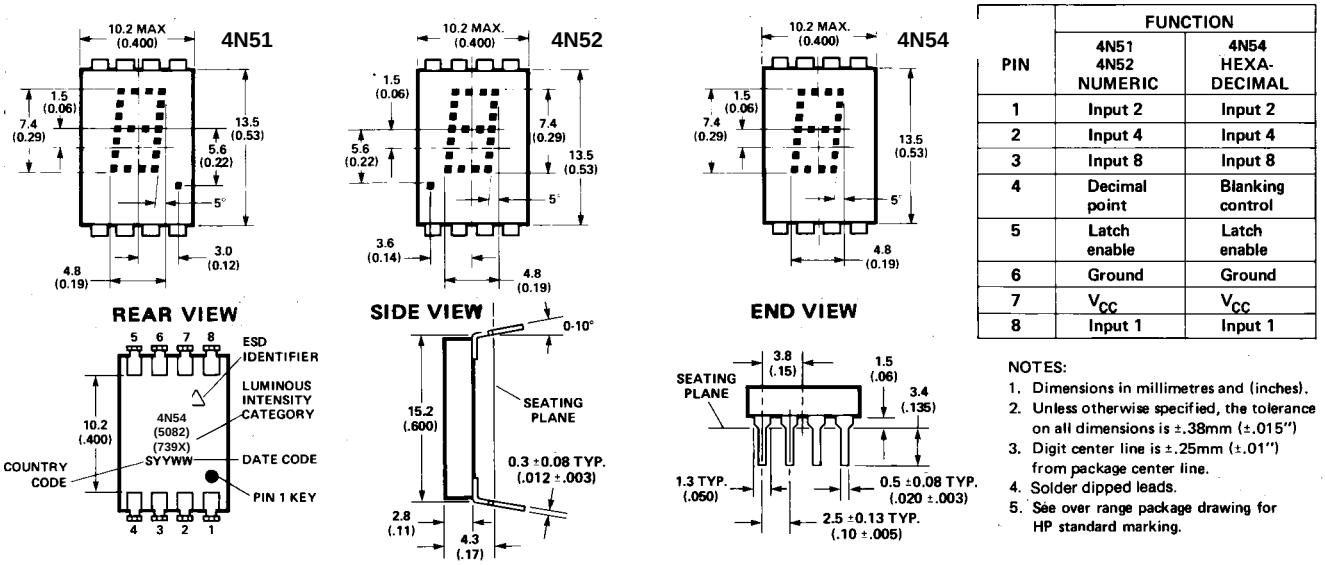
These standard red solid state displays have a 7.4 mm (0.29 inch) dot matrix character and an on-board IC with data memory latch/decoder and LED drivers in a glass/ceramic package. These devices utilize a solder glass frit seal.

The 4N51 numeric display decodes positive 8421 BCD logic inputs into characters 0-9, a "–" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

Features

- Three character options
  Numeric, hexadecimal, over range
- 4 x 7 dot matrix character
- Performance guaranteed over temperature
- High temperature stabilized
- Solder dipped leads
- Memory latch/decoder/driver
  TTL compatible
- Categorized for luminous intensity

Package Dimensions*



PIN	FUNCTION	
	4N51 4N52 NUMERIC	4N54 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.
4. Solder dipped leads.
5. See over range package drawing for HP standard marking.

*JEDEC Registered Data.

The 4N52 is the same as the 4N51 except that the decimal point is located on the left side of the digit.

The 4N54 hexadecimal display decodes positive 8421 logic inputs into 16 states, 0-9 and A-F.

In place of the decimal point an input is provided for blanking the display (all LEDs off), without losing the contents of the memory.

The 4N53 is a "± 1." overrange display, including a right-hand decimal point.

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+125	°C
Operating Temperature, Ambient[1,2]	T_A	-55	+100	°C
Supply Voltage[3]	V_{CC}	-0.5	+7.0	V
Voltage Applied to Input Logic, dp and Enable Pins	V_I, V_{DP}, V_E	-0.5	V_{CC}	V
Voltage Applied to Blanking Input[7]	V_B	-0.5	V_{CC}	V
Maximum Solder Temperature at 1.59 mm (0.062 inch) Below Seating Plane; t ≤ 5 Seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature, Ambient[1,2]	T_A	–55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time Data Must Be Held Before Positive Transition of Enable Line	t_{SETUP}	50			nsec
Time Data Must Be Held After Positive Transition of Enable Line	t_{HOLD}	50			nsec
Enable Pulse Rise Time	t_{TLH}			200	nsec

*JEDEC Registered Data.

Electrical/Optical Characteristics*

T_A = –55°C to +100°C, unless otherwise specified

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC} = 5.5 V (Characters "5." or "B")		112	170	mA
Power Dissipation	P_T			560	935	mW
Luminous Intensity per LED (Digit Average)[5,6]	I_v	V_{CC} = 5.0 V, T_A = 25°C	40	85		µcd
Logic Low-Level Input Voltage	V_{IL}	V_{CC} = 4.5 V			0.8	V
Logic High-Level Input Voltage	V_{IH}		2.0			V
Enable Low-Voltage; Data Being Entered	V_{EL}				0.8	V
Enable High-Voltage; Data Not Being Entered	V_{EH}		2.0			V
Blanking Low-Voltage; Display Not Blanked[7]	V_{BL}				0.8	V
Blanking High-Voltage; Display Blanked[7]	V_{BH}		3.5			V
Blanking Low-Level Input Current[7]	I_{BL}	V_{CC} = 5.5 V, V_{BL} = 0.8 V			50	µA
Blanking High-Level Input Current[7]	I_{BH}	V_{CC} = 5.5 V, V_{BH} = 4.5 V			1.0	mA
Logic Low-Level Input Current	I_{IL}	V_{CC} = 5.5 V, V_{IL} = 0.4 V			-1.6	mA
Logic High-Level Input Current	I_{IH}	V_{CC} = 5.5 V, V_{IH} = 2.4 V			+100	µA
Enable Low-Level Input Current	I_{EL}	V_{CC} = 5.5 V, V_{EL} = 0.4 V			-1.6	mA
Enable High-Level Input Current	I_{EH}	V_{CC} = 5.5 V, V_{EH} = 2.4 V			+130	µA
Peak Wavelength	λ_{PEAK}	T_A = 25°C		655		nm
Dominant Wavelength[8]	λ_d	T_A = 25°C		640		nm
Weight**				1.0		gm
Leak Rate					5×10^{-8}	cc/sec

Notes:

1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA} = 50°C/W; Θ_{JC} = 15°C/W.
2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A = +100°C.
3. Voltage values are with respect to device ground, pin 6.
4. All typical values at V_{CC} = 5.0 Volts, T_A = 25°C.
5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking.
6. The luminous intensity at a specific ambient temperature, $I_v(T_A)$, may be calculated from this relationship: $I_v(T_A) = I_{v(25°C)}(0.985)^{(T_A-25°C)}$.
7. Applies only to 4N54.
8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data.
**Non-Registered Data.

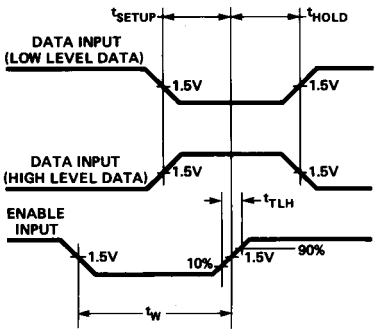


Figure 1. Timing Diagram of 4N51-4N54 Series Logic.

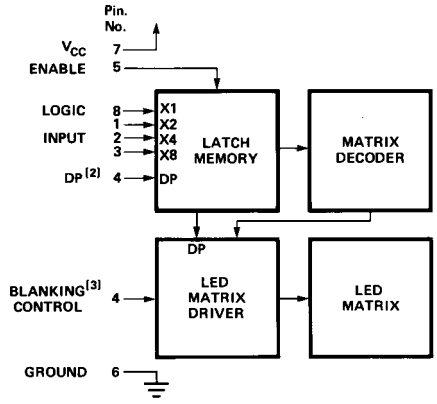


Figure 2. Block Diagram of 4N51-4N54 Series Logic.

TRUTH TABLE					
BCD DATA[1]				4N51 AND 4N52	4N54
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	A	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	----	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control input, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon display memory.

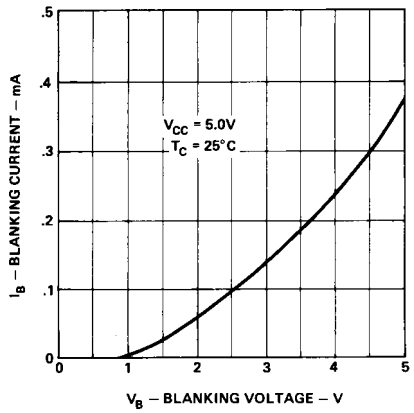


Figure 3. Typical Blanking Control Current vs. Voltage for 4N54.

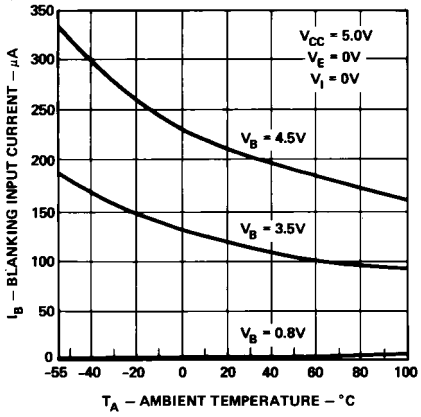


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 4N54.

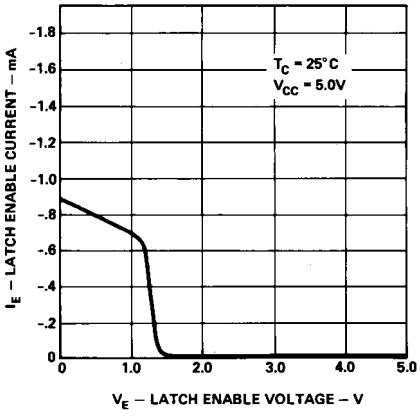


Figure 5. Typical Latch Enable Input Current vs. Voltage.

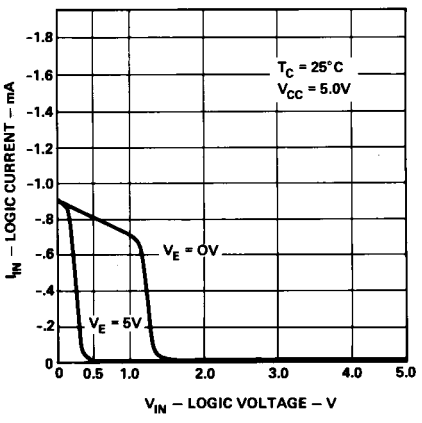


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

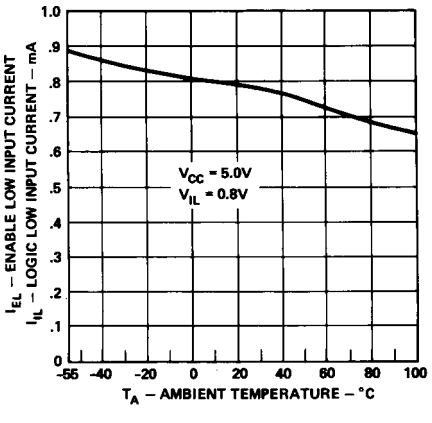


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

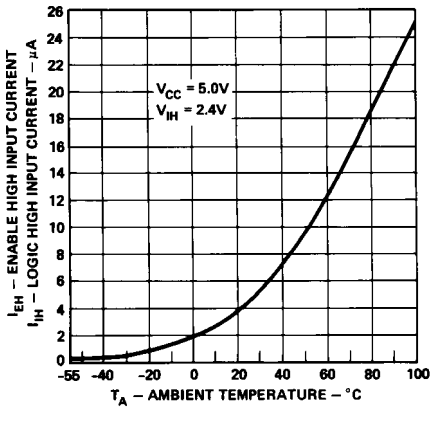


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

Electrical

The 4N51-4N54 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LEDs) to display decimal/hexadecimal numeric information. The LEDs are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The blanking control input on the 4N54 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5\ V)/[N\ (1.0\ mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The ESD susceptibility of the IC devices is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263.

Mechanical

4N51-4N54 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5×10^{-8} cc/sec and a fluorocarbon gross leak bubble test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54 mm (0.100 inch) and the lead row spacing is 15.24 mm (0.600 inch). These displays may be end stacked with 2.54 mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324 AG2D (3 digits) or Augat 508 (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100°C, it is important to maintain a case-to-ambient thermal resistance of less than 35°C/watt as measured on top of display pin 3.

Soldering

For information on soldering and post solder cleaning, see Application Note *1027 Soldering LED Components.*

Preconditioning

4N51-4N54 series displays are 100% preconditioned by 24 hour storage at 125°C.

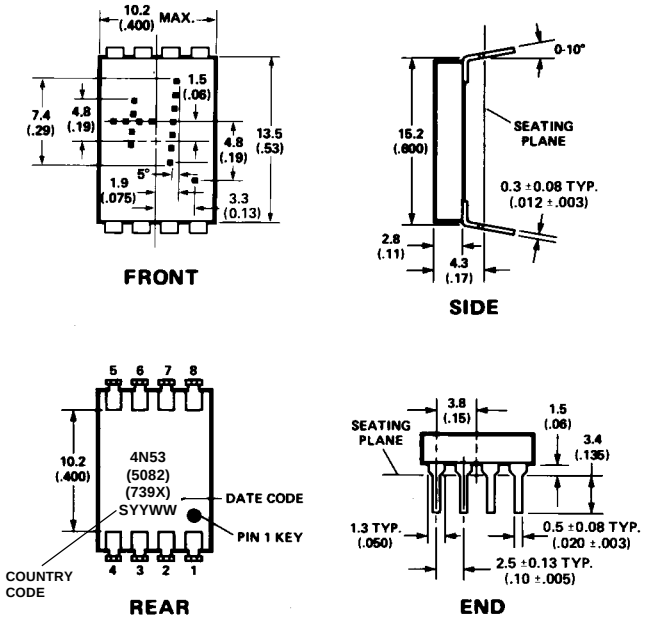
Contrast Enhancement

The 4N51-4N54 displays have been designed to provide the maximum possible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. For further information see Avago Application Note 1015, *Contrast Enhancement for LED Displays.*

Solid State Over Range Display

For display applications requiring a ±, 1, or decimal point designation, the 4N53 over range display is available. This display module comes in the same package as the 4N51-4N54 series numeric display and is completely compatible with it.

Package Dimensions*



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

*JEDEC registered data

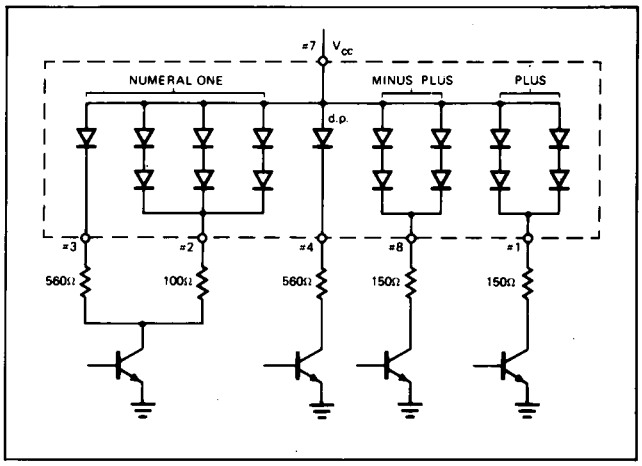


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

4N53 (T_A = –55°C to +100°C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power Dissipation	P_T	I_F = 10 mA, all diodes lit		280	320	mW
Luminous Intensity per LED (Digit Average)	I_F	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak Wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight**				1.0		gm

Recommended Operating Conditions*

Description	Sym	Min	Nom	Max	Unit
LED Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Forward Current, Each LED	I_F		5.0	10	mA

Absolute Maximum Ratings*

Description	Symbol	Min	Max	Unit
Storage Temperature, Ambient	T_S	–65	+125	°C
Operating Temperature, Ambient	T_A	–55	+100	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		4	V

Note:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

*JEDEC Registered Data.
**Non-Registered Data.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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