MOTOROLA

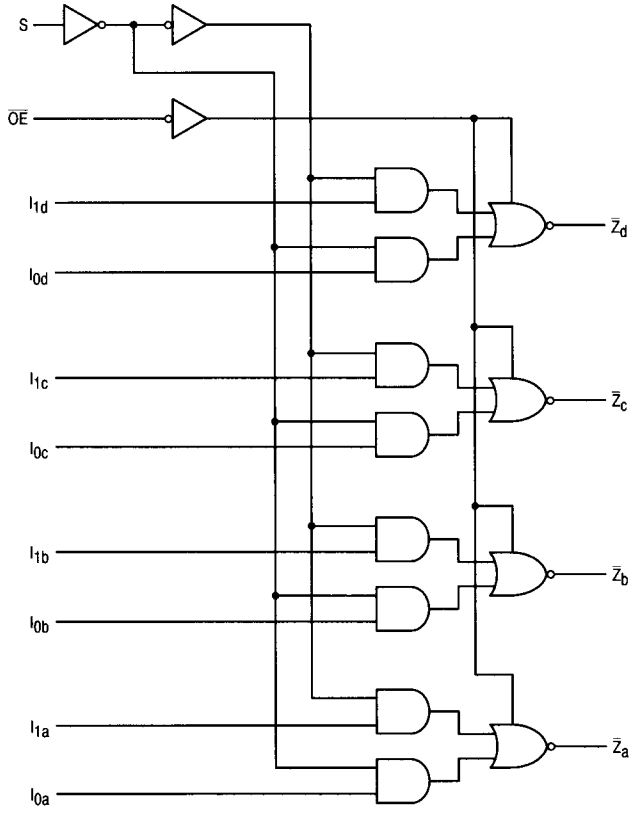
Quad 2-Input Data Selector/Multiplexer With 3-State Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/33907

The 54F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in the complemented (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with the bus oriented systems.

- Multiplexer Expansion By Tying Outputs Together
- Inverting 3-State Outputs

LOGIC DIAGRAM



Military 54F258

AVAILABLE AS:

1) JAN: JM38510/33907BXA
2) SMD: N/A
3) 883: 54F258/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
S	1	1	2	V_{CC}
I_{0a}	2	2	3	V_{CC}
I_{1a}	3	3	4	V_{CC}
$\overline{Z}_a$	4	4	5	OPEN
I_{0b}	5	5	7	V_{CC}
I_{1b}	6	6	8	V_{CC}
$\overline{Z}_b$	7	7	9	OPEN
GND	8	8	10	GND
$\overline{Z}_d$	9	9	12	OPEN
I_{1d}	10	10	13	V_{CC}
I_{0d}	11	11	14	V_{CC}
$\overline{Z}_c$	12	12	15	OPEN
I_{1c}	13	13	17	V_{CC}
I_{0c}	14	14	18	V_{CC}
$\overline{OE}$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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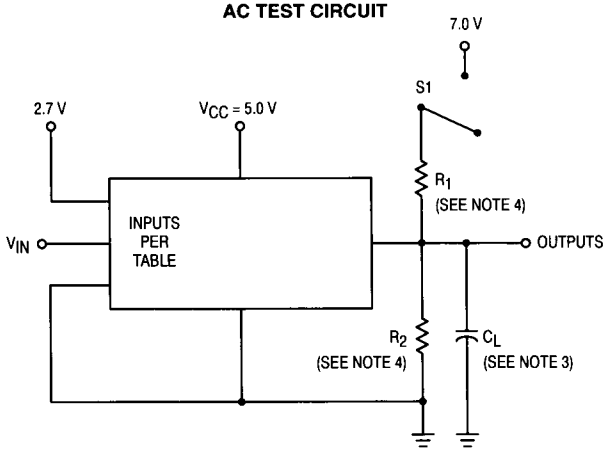
FUNCTIONAL DESCRIPTION

The F258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under the control of a Common Data Select input (S). When the Select input is LOW, the I_{0X} inputs are selected and when Select is HIGH, I_{1X} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

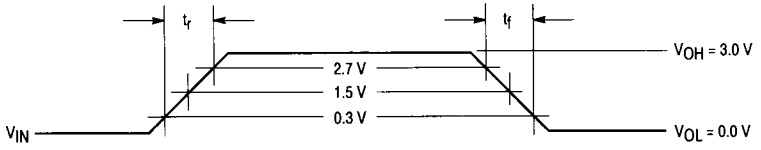
$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \quad Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \quad Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

AC TEST CIRCUIT



Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed



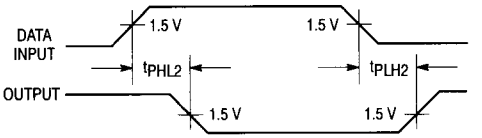
TRUTH TABLE

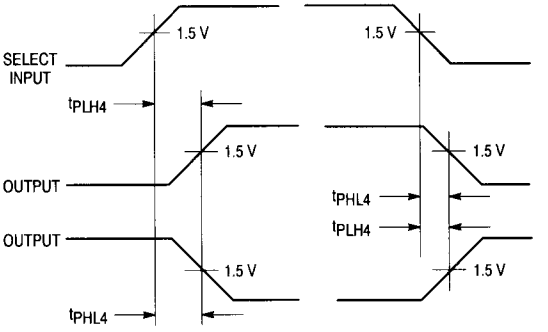
Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

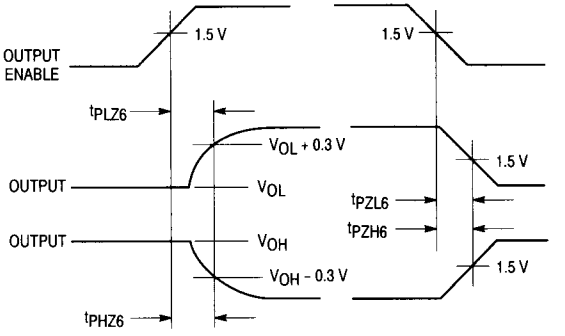
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

NOTES:
1. V_{IN} = input pulse has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f \leq 2.5$ ns, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
4. $R_1 = R_2 = 499\ \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

WAVEFORMS


DATA
INPUT
1.5 V
1.5 V
tPHL2
tPLH2
OUTPUT
1.5 V
1.5 V


SELECT
INPUT
1.5 V
1.5 V
tPLH4
1.5 V
1.5 V
OUTPUT
tPHL4
tPLH4
OUTPUT
1.5 V
1.5 V
tPHL4


OUTPUT
ENABLE
1.5 V
1.5 V
tPLZ6
VOL + 0.3 V
1.5 V
OUTPUT
VOL
tPZL6
tPZH6
OUTPUT
VOH
VOH - 0.3 V
1.5 V
tPHZ6

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IH} = 2.0 V, S = 0.8 V or 2.0 V, V_{IL} = 0.8 V, $\overline{OE}$ = 0.8 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, S = 0.8 V or 2.0 V, V_{IH} = 2.0 V, $\overline{OE}$ = 0.8 V, other inputs are open.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{OE}$ = 4.5 V, or (2.7 V), S = 0 V, 4.5 V or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open, $\overline{OE}$ = 4.5 V, or (7.0 V), S = 0 V, 4.5 V or (7.0 V).
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, $\overline{OE}$ = GND or (0.5 V), S = 4.5 V, 0 V or (0.5 V).
I_{OD}	Diode Current	35		35		35		mA	V_{CC} = 4.5 V, V_{IN} = 5.5 V or open, S = 0 V, V_{OUT} = 2.5 V, $\overline{OE}$ = 0 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V or 0 V, all other inputs are open, V_{OUT} = 0 V, S = 0 V, $\overline{OE}$ = 0 V.
I_{OZH}	Output Off Current High		50		50		50	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, all other inputs are open, V_{OUT} = 2.4 V, S = 0 V, $\overline{OE}$ = 2.0 V.
I_{OZL}	Output Off Current Low		−50		−50		−50	µA	V_{CC} = 5.5 V, V_{IH} = 4.5 V, V_{IL} = 0 V, V_{OUT} = 0.5 V, S = 4.5 V, $\overline{OE}$ = 2.0 V.
I_{CCH}	Power Supply Current		9.5		9.5		9.5	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		23		23		23	mA	V_{CC} = 5.5 V, V_{IH} = 4.5 V, V_{IL} = 0 V, S = 4.5 V, $\overline{OE}$ = 0 V.
I_{CCZ}	Power Supply Current		17		17		17	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), $\overline{OE}$ = 4.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**), V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2}	Propagation Delay /Data-Output I_n to $\overline{Z}$	1.0	4.0	1.0	6.0	1.0	6.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output I_n to $\overline{Z}$	2.5	5.3	2.0	7.5	2.0	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output S to $\overline{Z}$	2.5	7.0	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output S to $\overline{Z}$	3.0	7.5	3.0	9.5	3.0	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZH6}	Propagation Delay /Data-Output I_n or S to $\overline{Z}$	2.0	6.0	2.0	8.0	2.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZL6}	Propagation Delay /Data-Output I_n or S to $\overline{Z}$	2.5	7.0	2.5	9.0	2.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHZ6}	Propagation Delay /Data-Output I_n or S to $\overline{Z}$	2.0	6.0	1.5	7.0	1.5	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLZ6}	Propagation Delay /Data-Output I_n or S to $\overline{Z}$	2.0	6.0	2.0	8.5	2.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.