HYM5V32224A X-Series

2M x 32-bit CMOS DRAM MODULE

DESCRIPTION

The HYM5V32224A is a 2M x 32-bit EDO mode CMOS DRAM module consisting of four HY51V18164B in 44/50 pin TSOPII on a 72 Zig Zag Dual tabs pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.
The HYM5V32224ATXG/ASLTXG are Gold plated socket type Small outline Dual In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 5.0mW (SL-part)
  Max. battery back-up 6.5mW (SL-part)
  Max. CMOS standby 2.9mW (SL-part)
  14.4mW
  Max. TTL standby 28.8mW
  Max. operating

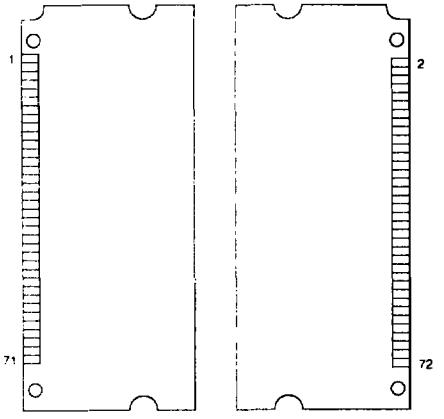
Speed	Power
60	1.24W
70	1.09W
80	0.95W

- **Single power supply of 3.3V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tHPC
60	60ns	17ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- **EDO mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh, Self-refresh**
- **1024 refresh cycles / 256ms (SL-part)**
  1024 refresh cycles / 16ms

PIN CONNECTION



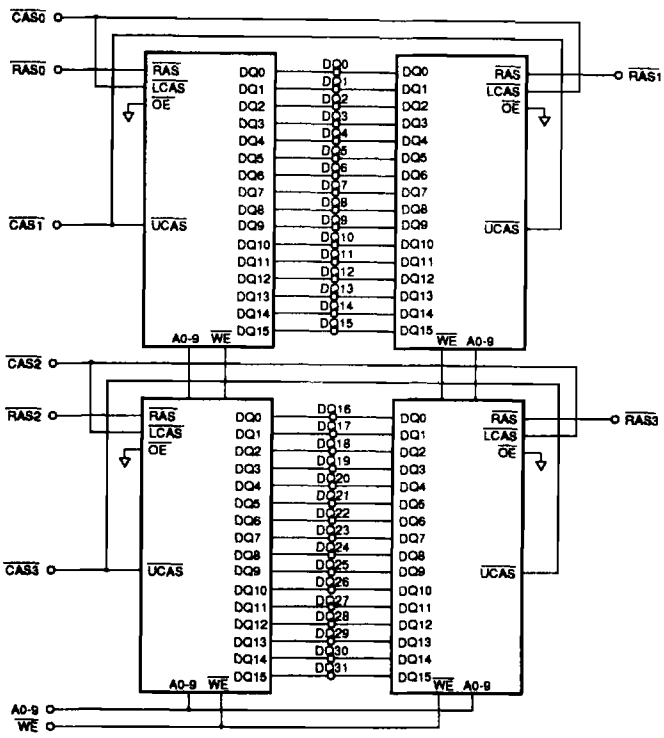
PIN DESCRIPTION

$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A9	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 3.3V)
Vss	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ16
2	DQ0	38	DQ17
3	DQ1	39	Vss
4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	$\overline{CAS2}$
6	DQ4	42	$\overline{CAS3}$
7	DQ5	43	$\overline{CAS1}$
8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	$\overline{RAS1}$
10	Vcc	46	NC
11	PD1	47	$\overline{WE}$
12	A0	48	NC
13	A1	49	DQ18
14	A2	50	DQ19
15	A3	51	DQ20
16	A4	52	DQ21
17	A5	53	DQ22
18	A6	54	DQ23
19	NC	55	NC
20	NC	56	DQ24
21	DQ8	57	DQ25
22	DQ9	58	DQ26
23	DQ10	59	DQ28
24	DQ11	60	DQ27
25	DQ12	61	Vcc
26	DQ13	62	DQ29
27	DQ14	63	DQ30
28	A7	64	DQ31
29	NC	65	NC
30	Vcc	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	$\overline{RAS3}$	69	PD5
34	$\overline{RAS2}$	70	PD6
35	DQ15	71	PD7
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	NC	NC	NC
PD2	Vss	Vss	Vss
PD3	Vss	Vss	Vss
PD4	Vss	Vss	Vss
PD5	NC	Vss	NC
PD6	NC	NC	Vss

PD7	REFRESH MODE
NC	Normal
Vss	Self Refresh

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 3.3V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+ 1.0, All other pins not under test= V_{SS}		-40	40	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-20	20	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	60	-	344	mA	1,2,3
			70	-	304		
			80	-	264		
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH} other inputs≥ V_{SS}		-	8	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	60	-	344	mA	1,3
			70	-	304		
			80	-	264		
I_{CC4}	V_{CC} Supply Current, EDO mode	t_{HPC}= t_{HPC} (min.)	60	-	284	mA	1,2,3
			70	-	244		
			80	-	204		
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V		-	4	mA	
			SL-part	-	0.8		5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	60	-	344	mA	1,3
			70	-	304		
			80	-	264		
I_{CC7}	V_{CC} Supply Current, Battery Back Up (SL-part only)	t_{RC}= 250µs $\overline{CAS}$= CBR cycling or 0.2V $\overline{WE}$= V_{CC}–0.2V A0-A9= V_{CC}–0.2V or 0.2V DQ0-DQ31= V_{CC}–0.2V, 0.2V, or open	$t_{RAS} \le$ 300ns		1.4	mA	1,4,5
			$t_{RAS} \le$ 1µs	-	1.8		
I_{CC8}	V_{CC} Supply Current, Self Pefresh (SL-Part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤0.2V other pins same as I_{CC7}			1.4	mA	
V_{OL}	Output Low Voltage	I_{OL}= 2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}= -2mA		2.4		V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. Icc is specified as average current. for I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$= V_{IL}. for I_{CC4}, address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal functional operation.
5. I_{CC5}(max.)= 0.8mA, I_{CC7} and I_{CC8} are applied to SL-part only (HYM5V32224ASLX/ASLTXG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V32224A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	150	-	ns	
2	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	14,15
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	40	-	40	-	ns	13,15
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	17	-	20	-	20	ns	4,9,15
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10,15
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	35	-	40	ns	4,15
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4,13
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5,17
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3,12
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	13	-	15	-	20	-	ns	15
16	tCSH	$\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	14
17	tCAS	$\overline{CAS}$ Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	9,16
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10,16
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	$\overline{CAS}$ Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	15
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	14
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	13
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	13
26	tAR	Column Address Hold Time from $\overline{RAS}$	26	-	26	-	26	-	ns	14
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	15
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	13
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6,13
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6,14
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	13
32	tWCR	Write Command Hold Time from $\overline{RAS}$	53	-	53	-	58	-	ns	14
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	15	-	15	-	ns	15
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	20	-	ns	13
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7,14
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	53	-	53	-	58	-	ns	14
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		SL-part	-	256	-	256	-	256		
40	tWCS	Write Command Set-up Time	2	-	2	-	2	-	ns	8,13

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V32224A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	37	-	45	-	45	-	ns	8,15
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	-	95	-	105	-	ns	8,14,15
43	tAWD	Column Address to $\overline{WE}$ Delay Time	50	-	60	-	65	-	ns	8,14,15
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	15
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	14
46	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
46	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	
46	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	-	65	-	75	-	ns	8,14,15
49	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
50	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
51	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
52	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
53	tCHS	$\overline{CAS}$ Hold Tlime (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
54	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
55	tREZ	Output Buffer Turn Off Delay Time from $\overline{RAS}$	0	15	0	15	0	15	ns	
56	tWEZ	Output Buffer Turn Off Delay Time from $\overline{WE}$	0	15	0	15	0	15	ns	
57	tWED	$\overline{WE}$ to Data Delay Time	15	-	15	-	15	-	ns	
58	tWPE	$\overline{WE}$ Pulse Width (EDO Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= V_{SS} during power-up, the HYM5V32224A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
4. Refer to the HY51V18164B data sheet for detailed information.
5. Measured at V_{OH}= 2.4V and V_{OL}= 0.4V with a load equivalent to 1 TTL loads and 100pF.
6. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
9. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
10. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
11. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
12. t_{REF}(max.)= 256ms is applied to SL-part only (HYM5V32124ASLTXG).
13. A burst of 1024 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 16ms after exiting self refres (for SL-part).

CAPACITANCE

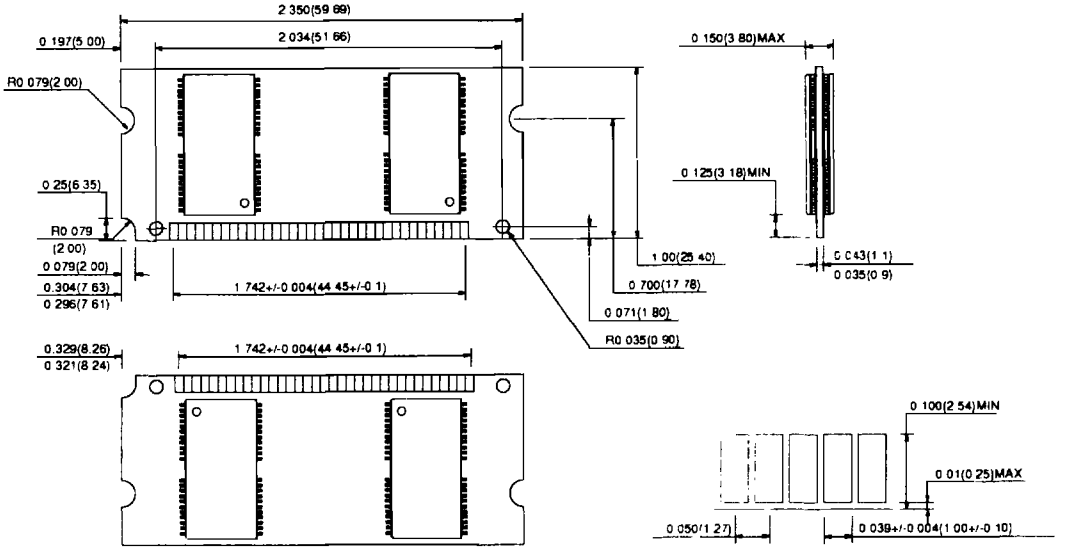
(T_A= 25°C, V_{CC}= 3.3V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9, B0, $\overline{WE0}$, $\overline{WE2}$)	-	40	pF
C_{IN2}	Input Capacitance ($\overline{RAS0}$-$\overline{RAS3}$)	-	15	PF
C_{IN3}	Input Capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	-	20	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ63)	-	15	pF

PACKAGE INFORMATION

72 pin Small Outline Dual In-line Memory Module (XG ; Gold plated)

UNIT INCH(mm)
TOLERANCE +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V32224ATXG	60/70/80		DIMM	Gold
HYM5V32224ASLTXG	60/70/80	SL-part	DIMM	Gold