MOTOROLA

Military 54F164

Advance Information

8-Bit Serial In/Parallel-Out Shift Register

ELECTRICALLY TESTED PER:
MPG54F164

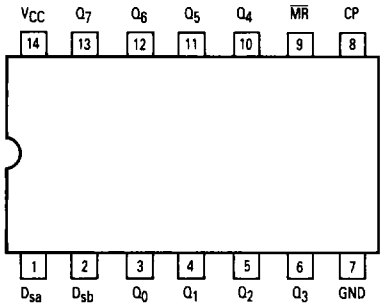
MPO

AVAILABLE AS:

1) JAN: *
2) SMD: *
3) 883C: *

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
***Call Factory for latest update**

CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
D_{sa}	1	1	2	V_{CC}
D_{sb}	2	2	3	V_{CC}
Q_0	3	3	4	OPEN
Q_1	4	4	6	OPEN
Q_2	5	5	8	OPEN
Q_3	6	6	9	OPEN
GND	7	7	10	GND
$\overline{CP}$	8	8	12	V_{CC}
$\overline{MR}$	9	9	13	GND
Q_4	10	10	14	OPEN
Q_5	11	11	16	OPEN
Q_6	12	12	18	OPEN
Q_7	13	13	19	OPEN
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

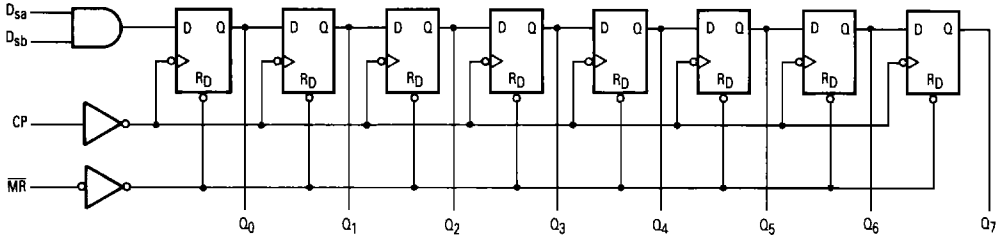
MODE SELECT TRUTH TABLE

OPERATING MODE	Inputs				Outputs			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	–	Q_7
Reset (Clear)	L	X	X	X	L	L	–	L
Shift	H	^	l	l	L	q_0		q_6
	H	^	l	h	L	q_0		q_6
	H	^	h	l	L	q_0		q_6
	H	^	h	h	H	q_0		q_6

H = HIGH Voltage Levels.
L = LOW Voltage Levels.
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.
X = Don't Care.
^ = LOW to HIGH clock transition.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

LOGIC DIAGRAM



Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 0.8 V or 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IN} = 0.8 V or 2.0 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{OUT} = 0 V.
I_{IL}	Logical "0" Input Current	−0.3	−0.6	−0.3	−0.6	−0.3	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V.
I_{CC}	Power Supply Current Off		55		55		55	mA	V_{CC} = 5.5 V, V_{IN} = open (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q_n		11		13		13	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output CP to Q_n		8.0		11		11	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PHL2}	Propagation Delay /Data-Output $\overline{MR}$ to Q_n		13		17		17	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
f_{MAX}	Maximum Clock Frequency	80		60		60		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.

5