

FAST 74F838

Microprogram Sequence Controller

FAST Products

FEATURES

- 5-bit address generator (32 micro-instruction addressability)
- Two subroutine branching capability
- Interrupt branching
- Cascadable for increased addressing
- Direct branching over full address range

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F838	90MHz	mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
20-Pin Plastic DIP	N74F838N
20-Pin SOL	N74F838D

DESCRIPTION

The 74F838 Microprogram Sequence Controller generates addresses to access instructions from a microprogram memory.

This high speed device provides an efficient means of controlling the flow through a microprogram by providing a powerful set of sequencing functions.

In addition to providing branching facility over the entire address range, the device also supports two subroutines and an interrupt level.

The 74F838 can directly address up to 32 micro-instructions: two or more of these devices may be cascaded for increased addressing. For example, two devices can address 1K and three devices can address up to 32K of program storage.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

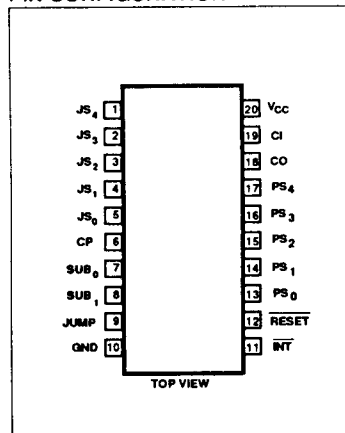
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$JS_0 - JS_4$	Jump state inputs	1.0/1.0	20 μ A/0.6mA
JMP	Jump input	1.0/1.0	20 μ A/0.6mA
SUB_0, SUB_1	Subroutine inputs	1.0/1.0	20 μ A/0.6mA
\overline{INT}	Interrupt input	1.0/1.0	20 μ A/0.6mA
CP	Clock input	1.0/1.0	20 μ A/0.6mA
CI	Cascade In input	1.0/1.0	20 μ A/0.6mA
\overline{RESET}	Reset input	1.0/1.0	20 μ A/0.6mA
$PS_0 - PS_4$	Present state outputs	150/40	3.0mA/24mA
CO	Cascade Out output	150/40	3.0mA/24mA

NOTE:

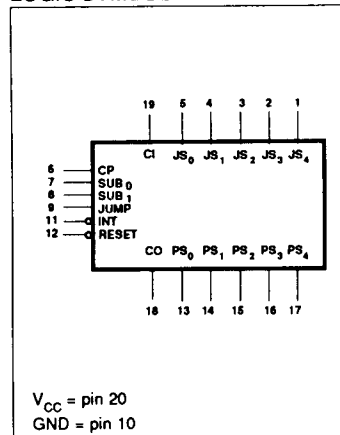
One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

Combined with memory, the 74F838 form a powerful control section for CPUs and I/O controllers.

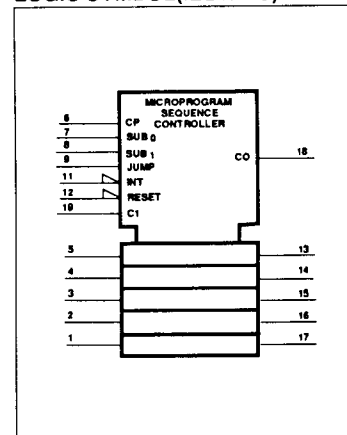
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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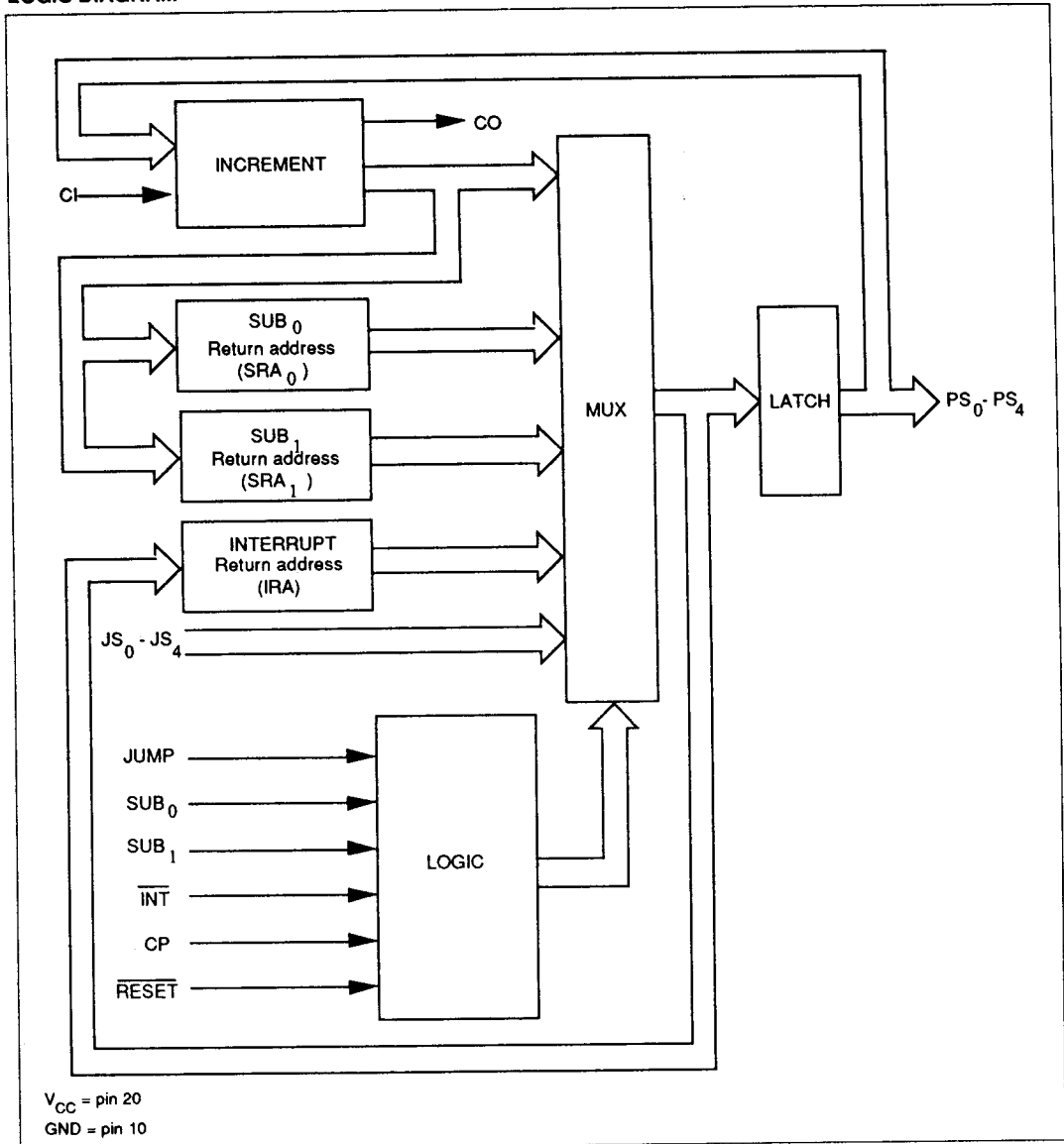
PIN DESCRIPTION

PIN NO.	SYMBOL	TYPE	FUNCTION	DESCRIPTION
5	JS ₀	Input	Jump State	Address on these inputs is transferred to the PS ₀ -PS ₄ outputs if the JMP input is High or the SUB ₀ or SUB ₁ inputs change from Low-to-High. These inputs are ignored if neither of the above conditions is true.
4	JS ₁			
3	JS ₂			
2	JS ₃			
1	JS ₄			
7	SUB ₀	Input	Subroutine	On a Low-to-High transition, the Present State address (PS ₀ -PS ₄) plus one is saved internally as a return address, and address on pins JS ₀ -JS ₄ will be transferred to the PS ₀ -PS ₄ outputs. On a High-to-Low transition, the saved return address state will be enabled onto the PS ₀ -PS ₄ outputs.
8	SUB ₁			
9	JMP	Input	Jump	When JMP is High, the next state address will be JS ₀ -JS ₄ .
11	$\overline{\text{INT}}$	Input	Interrupt	On a High-to-Low transition, the next address to appear on the PS ₀ -PS ₄ output is saved internally as a return address and PS ₀ -PS ₄ are forced to all ones. If this feature is used, a micromode jump would normally be stored at state address 11111. SUB ₀ or SUB ₁ inputs are ignored when $\overline{\text{INT}}$ is Low. On a Low-to-High transition, the saved return address state is enabled onto the PS ₀ -PS ₄ outputs.
6	CP	Input	Clock	This clock determines the sequence rate of the controller.
12	$\overline{\text{RESET}}$	Input	Reset	When Low, all internal registers and PS ₀ -PS ₄ are set to zeros.
19	CI	Input	Cascade In	This input should be tied to V _{CC} for the least significant device. For all other devices, CI is connected to CO of the previous device.
18	CO	Output	Cascade Out	This signal is connected to CI of the next device. One device permits 32 states; two devices allow 1024 states; three devices allow 32,768 states.
13	PS ₀	Output	Present state	The address of the present state.
14	PS ₁			
15	PS ₂			
16	PS ₃			
17	PS ₄			

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LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS							OUTPUTS			OPERATING MODE	
							INTERNAL REGISTERS				
RESET	INT	JUMP	SUB ₀	SUB ₁	CP	JS _n	PS ₀ -PS ₄	SRA ₀	SRA ₁		IRA
L	X	X	X	X	X	X	00000	0	0	0	Reset
H	H	L	H or L	H or L	↑	X	PS _{n+1}				Increment
H	L	L	X	X	↑	X	PS _{n+1}				
H	L	H	X	X	↑	JS _n	JS _n				Jump
H	H	H	↓	↓	↑	JS _n	JS _n				
H	H	X	↑	H or L	↑	JS _n	JS _n	PS _{n+1}			Subroutine Call
H	H	X	H or L	↑	↑	JS _n	JS _n	PS _{n+1}	PS _{n+1}		
H	H	X	↑	↑	↑	JS _n	JS _n	PS _{n+1}	PS _{n+1}		
H	H	L	↓	H or L	↑	X	SRA ₀				Return from Subroutine
H	H	L	H or L	↓	↑	X	SRA ₁				
H	↓	L	H or L	H or L	↑	X	11111			PS _{n+1}	Interrupt Call
H	↓	H	H or L	H or L	↑	JS _n	11111			JS _n	
H	↓	X	↑	H or L	↑	JS _n	11111	PS _{n+1}		JS _n	
H	↓	X	H or L	↑	↑	JS _n	11111			JS _n	
H	↓	X	↑	↑	↑	JS _n	11111	PS _{n+1}	PS _{n+1}	JS _n	
H	↓	L	↓	H or L	↑	X	11111			SRA ₀	
H	↓	L	H or L	↓	↑	X	11111			SRA ₁	Return from Interrupt
H	↑	X	X	X	↑	X	IRA				Illegal
H	H	H	↓	H or L	↑	JS _n	JS _n + SRA ₀				
H	H	H	H or L	↓	↑	JS _n	JS _n + SRA ₁				
H	H	L	↓	↓	↑	X	SRA ₀ + SRA ₁				
H	H	H	↓	↓	↑	JS _n	JS _n + SRA ₀ + SRA ₁				
H	↓	H	↓	H or L	↑	JS _n	11111			JS _n + SRA ₀	
H	↓	H	H or L	↓	↑	JS _n	11111			JS _n + SRA ₁	
H	↓	L	↓	↓	↑	X	11111			SRA ₀ + SRA ₁	
H	↓	H	↓	↓	↑	JS _n	11111			JS _n + SRA ₀ + SRA ₁	

H = High voltage level.
 L = Low voltage level.
 X = Don't care.
 ↓ = High-to-Low clock transition.
 ↓ = Anything except a High-to-Low clock transition.
 ↑ = Low-to-High clock transition.
 H or L = Either High or Low
 0 = Low output
 1 = High output
 To avoid timing problems INT is sampled on the falling edge of the clock and serviced on the next rising edge.

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APPLICATION

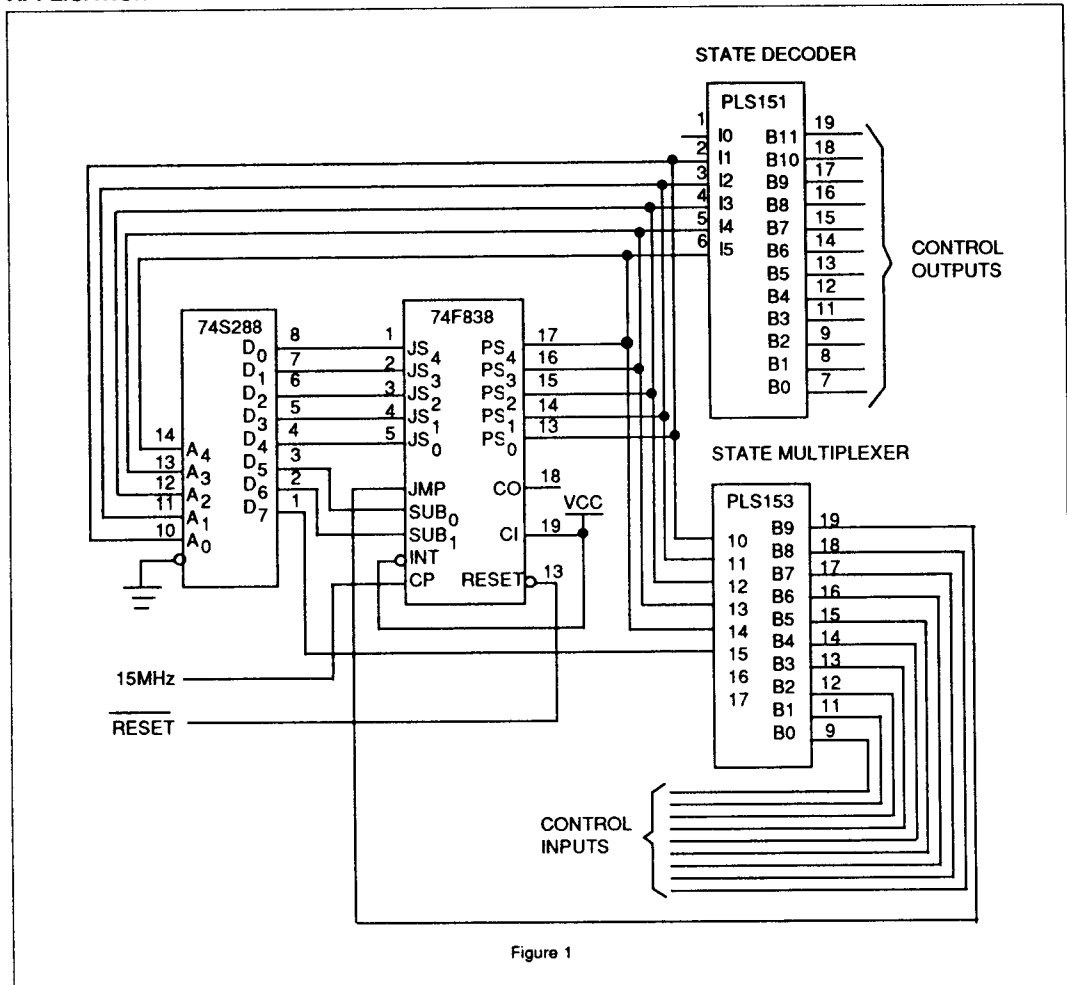


Figure 1

As shown in Figure 1, a PROM paired with a 74F838 creates a state machine. When reset, the PS₀-PS₄ outputs are zero. The present state is decoded to generate control inputs. In this application, a PLS151 acts as the state decoder. When a state has a branch option

based on the state of a control signal, the Present is used as the address input to a multiplexer. The output of the multiplexer connects to the JUMP input of the 74F838. When the proper state is decoded, the associated control input is passed on to the JUMP

input. In this application, to allow a forced jump, D₀ is also a control input. All state changes occur on the rising edge of the Clock input. However, since the interrupt input (INT) is normally asynchronous in many applications, to avoid timing problems, INT is sampled on the falling edge of the Clock.

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V	
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7		V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35 0.50	V	
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.35 0.50	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
I_{OS}	Short circuit output current ³	$V_{CC} = \text{MAX}, V_O = 2.25V$		-60	-150	mA	
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$			90	mA
		I_{CCL}				90	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	90				MHz
t_{PLH} t_{PHL}	Propagation delay CP to PS_n or CO	Waveform 1						ns
t_{PHL}	Propagation delay $\overline{\text{RESET}}$ to PS_n or CO.	Waveform 2						ns

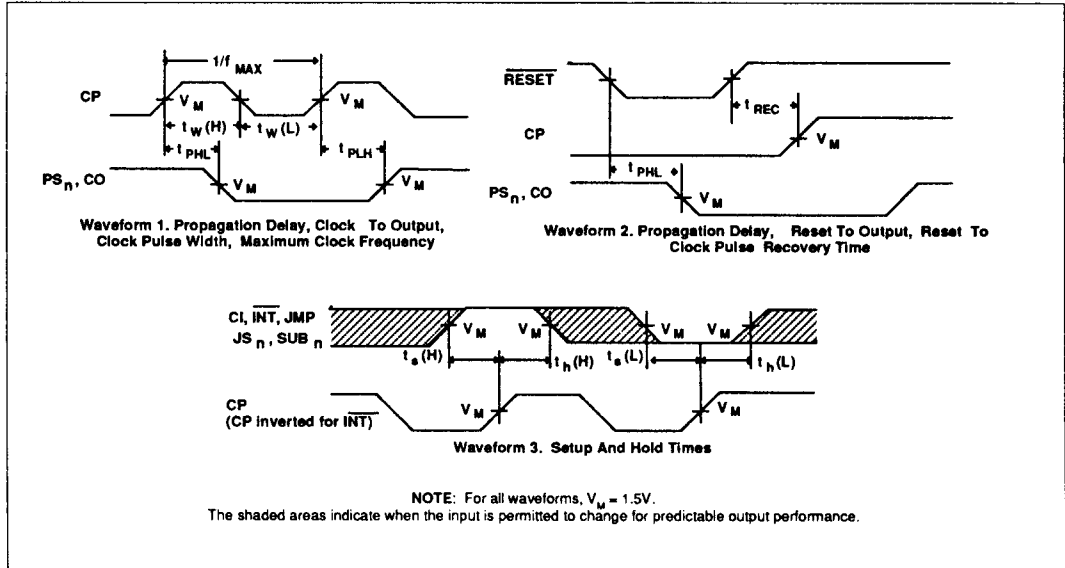
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low JS_n to CP	Waveform 3						ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low JS_n to CP	Waveform 3						ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low JMP to CP	Waveform 3						ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low JMP to CP	Waveform 3						ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low INT to CP	Waveform 3						ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low INT to CP	Waveform 3						ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low SUB_n to CP	Waveform 3						ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low SUB_n to CP	Waveform 3						ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low CI to CP	Waveform 3						ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low CI to CP	Waveform 3						ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse width, High or Low	Waveform 1						ns
$t_w(\text{L})$	$\overline{\text{RESET}}$ Pulse width, Low	Waveform 2						ns
t_{REC}	Recovery Time, $\overline{\text{RESET}}$ to CP	Waveform 2						ns

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

