PRELIMINARY

FEATURES

- 12-Bit Accuracy
- Fast Conversion Speeds: 5µs and 12µs
- Fast 90ns Bus Access Time
- No Missing Codes
- Complete ADC with On-Board Reference
- 215mW Max Power Dissipation
- Space Saving Narrow 0.3", 24-Pin DIP Package
- Alternate Source to the AD7572

APPLICATIONS

- Digital Signal Processing
- High Precision Industrial/Process Controls
- High-Speed Data Acquisition Systems
- Telecommunications
- Sonar/Radar

ORDERING INFORMATION †

5µs CONVERSION TIME††

NON-LINEARITY (FULL TEMP)	FULL SCALE (TEMPCO)	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	25ppm/°C	PM7572AW05	PM7572EW05
±1/2 LSB	25ppm/°C	PM7572ATC05	PM7572EP05
±1/2 LSB	25ppm/°C	–	PM7572ES05
±1 LSB	45ppm/°C	–	PM7572FW05
±1 LSB	45ppm/°C	–	PM7572FP05
±1 LSB	45ppm/°C	–	PM7572FS05†††

12µs CONVERSION TIME††

NON-LINEARITY (FULL TEMP)	FULL SCALE (TEMPCO)	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	25ppm/°C	PM7572AW12	PM7572EW12
±1/2 LSB	25ppm/°C	PM7572ATC12	PM7572EP12
±1/2 LSB	25ppm/°C	–	PM7572ES12
±1 LSB	45ppm/°C	–	PM7572FW12
±1 LSB	45ppm/°C	–	PM7572FP12
±1 LSB	45ppm/°C	–	PM7572FS12†††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages. For ordering information, see PMI's Data Book, Section 2.

†† Last two (2) part number digits signify conversion speed.

††† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

CROSS REFERENCE†

PMI	ADI	TEMPERATURE RANGE
PM7572AW	AD7572UQ	MIL
PM7572AW	AD7572TQ	
PM7572AW	AD7572SQ	
PM7572EW	AD7572CQ	IND
PM7572FW	AD7572BQ	
PM7572FW	AD7572AQ	
PM7572EP	AD7572LN	COM
PM7572FP	AD7572KN	
PM7572FP	AD7572JN	

† Conversion speed part number digits omitted for clarity.

GENERAL DESCRIPTION

The PM-7572 is a complete 12-bit BiCMOS Analog-to-Digital converter that is designed for high speed and low power applications. It uses a successive approximation technique to convert an analog input signal to a 12-bit digital output code. Simplified control circuitry makes the PM-7572 easy to use and interface to most microprocessors; its data output lines are controlled by read ($\overline{RD}$) and chip select ($\overline{CS}$) inputs. It also uses few microprocessor interface control lines and requires no external components.

The PM-7572's 3-state outputs are speed compatible with most popular microprocessors, thus, eliminating the need for wait states. It also has internal clock circuitry that allows it to be clocked from an external source, or for stand alone applications, can use its internal clock by using an external crystal.

The PM-7572 is fabricated using PMI's advanced BiCMOS process that combines bipolar and CMOS circuits on the same silicon chip.

The PM-7572 is offered in two conversion speeds, 5µs and 12µs. An 05 or 12 part number suffix differentiates the two devices; see ordering information. CerDIP and plastic packaged devices are offered in the extended industrial temperature range of –40°C to +85°C.

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

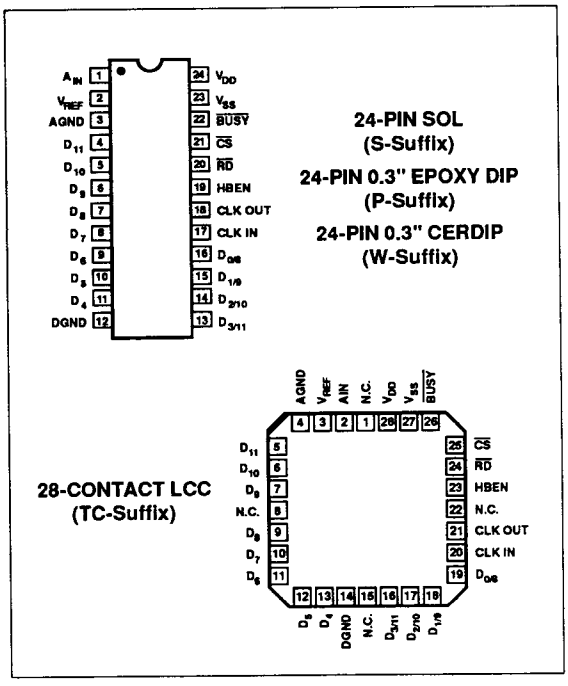
V_{DD} to DGND ..... –0.3 to +7V
V_{SS} to DGND ..... +0.3V to –17V
AGND to DGND ..... –0.3V, V_{DD} + 0.3V
A_{IN} to AGND ..... –15V to +15V
Digital Input Voltage to DGND
Pins 17, 19-21 ..... –0.3V, V_{DD} + 0.3V
Digital Output Voltage to DGND
Pins 4-11, 13-16, 18, 22 ..... –0.3V, V_{DD} + 0.3V
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering Temperature ..... +300°C
Operating Temperature Ranges
PM-7572AW Version ..... –55°C to +125°C
PM-7572EW/FW/EP/FP/ES/FS ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	64	7	°C/W
24-Pin Plastic DIP (P)	57	26	°C/W
28-Contact LCC (TC)	70	–	°C/W
24-Pin SOL (S)	70	22	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS at V_{DD} = +5V ± 5%; V_{SS} = –15V ± 5%; f_{CLK} = 2.5MHz for PM-7572XX05, 1MHz for PM-7572XX12; Specifications apply to Slow Memory Mode. T_A = Full Temperature Range as specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7572 MIN	PM-7572 TYP	PM-7572 MAX	UNITS
ACCURACY						
Resolution	N		12	–	–	Bits
Integral Nonlinearity	INL	PM-7572AW/EW/EP/ES	–	–	±1/2	LSB
		PM-7572FW/FP/FS	–	–	±1	
Differential Nonlinearity	DNL	Guaranteed Monotonic over Temperature	–	–	±1	LSB
Offset Error	V_{ZSE}	T_A = +25°C				LSB
		PM-7572AW/EW/EP/ES	–	–	±2	
		PM-7572FW/FP/FS	–	–	±3	
		T_A = Full Temperature Range				
		PM-7572AW/EW/EP/ES	–	–	±4	
		PM-7572FW/FP/FS	–	–	±6	
Full Scale Error	G_{FSE}	V_{DD} = +5V; V_{SS} = –15V; FS = +5V; Ideal Last Code Transition = FS – 3/2 LSBs	–	–	±10	LSB
Full Scale Tempco (Note 1)	TCG_{FS}	PM-7572AW/EW/EP/ES	–	–	±25	ppm/°C
		PM-7572FW/FP/FS	–	–	±45	
ANALOG INPUT						
Input Voltage Range	V_{IN}		0	–	+5	V
Input Current	I_{IN}		–	–	3.5	mA

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V ± 5%; V_{SS} = –15V ± 5%; f_{CLK} = 2.5MHz for PM-7572XX05, 1MHz for PM-7572XX12; Specifications apply to Slow Memory Mode. T_A = Full Temperature Range as specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7572 MIN	PM-7572 TYP	PM-7572 MAX	UNITS
INTERNAL REFERENCE						
V_{REF} Output Voltage	V_{REF}	T_A = +25°C	–5.2	–5.25	–5.3	V
V_{REF} Output Tempco	$V_{REF}TC$		–	20	–	ppm/°C
Output Current Sink Capability	I_{SINK}	External Load Should Not Change During Conversion	–	–	500	µA
POWER SUPPLY REJECTION						
V_{DD} Only	PSR+	FS Change, V_{SS} = –15V, V_{DD} = +4.75 to +5.25V	–	±1/2	–	LSB
V_{SS} Only	PSR–	FS Change, V_{DD} = 5V, V_{SS} = –14.25 to –15.75V	–	±1/2	–	LSB
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN						
Input Low Voltage	V_{INL}		–	–	+0.8	V
Input High Voltage	V_{INH}		+2.4	–	–	
Input Capacitance	C_{IN}		–	–	10	pF
$\overline{CS}$, $\overline{RD}$, HBEN Input Current	I_{IN}	V_{IN} = 0V to V_{DD}	–	–	±10	µA
CLK IN Input Current	I_{IN}	V_{IN} = 0V to V_{DD}	–	–	±20	µA
LOGIC OUTPUTS						
D11 - D0/8, $\overline{BUSY}$, CLK OUT						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6m	–	–	+0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	+4.0	–	–	
Floating State Leakage Current D11 - D0/8	I_{LKG}		–	–	10	µA
Floating State Output Capacitance	C_{OUT}		–	–	15	pF
CONVERSION TIME						
PM-7572XX05						
Synchronous Clock	t_{CONV}	f_{CLK} = 2.5MHz	–	–	5	µs
Asynchronous Clock			4.8	–	5.2	
PM7572XX12						
Synchronous Clock	t_{CONV}	f_{CLK} = 1.0MHz	–	–	12.5	µs
Asynchronous Clock			12	–	13	
POWER REQUIREMENTS						
Positive Power Supply	V_{DD}	For Specified Performance	4.75	5	5.25	V
Negative Power Supply	V_{SS}	For Specified Performance	–14.25	–15	–15.75	V
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = BUSY = V_{DD}; A_{IN} = +5V	–	–	7	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = BUSY = V_{DD}; A_{IN} = +5V	–	–	12	mA
Power Dissipation	P_{DISS}	$\overline{CS}$ = $\overline{RD}$ = BUSY = V_{DD}; A_{IN} = +5V 5VX 7mA + 15VX 12mA	–	135	215	mW

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V ± 5%; V_{SS} = –15V ± 5%; f_{CLK} = 2.5MHz for PM-7572XX05, 1MHz for PM-7572XX12; Specifications apply to Slow Memory Mode. T_A = Full Temperature Range as specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7572 MIN	PM-7572 TYP	PM-7572 MAX	UNITS
TIMING CHARACTERISTICS (V_{DD} = +5V; V_{SS} = –5V) (Note 2)						
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0	–	–	ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2	T_A = +25°C All Grades	–	–	190	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	230	
		T_A = Full Temperature PM-7572AW	–	–	270	
Data Access Time after $\overline{RD}$ (Note 3)	t_3	C_L = 20pF T_A = +25°C All Grades	–	–	90	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	110	
		T_A = Full Temperature PM-7572AW	–	–	120	
		C_L = 100pF T_A = +25°C All Grades	–	–	125	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	150	
		T_A = Full Temperature PM-7572AW	–	–	170	
$\overline{RD}$ Pulse Width	t_4		t_3	–	–	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0	–	–	ns
Data Setup Time after $\overline{BUSY}$ (Note 3)	t_6	T_A = +25°C All Grades	–	–	70	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	90	
		T_A = Full Temperature PM-7572AW	–	–	100	
Bus Relinquish Time (Note 4)	t_7	T_A = +25°C All Grades	20	–	75	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	20	–	85	
		T_A = Full Temperature PM-7572AW	20	–	90	
HBEN to $\overline{RD}$	t_8		0	–	–	ns
HBEN to $\overline{RD}$ Hold Time	t_9		0	–	–	ns
Delay Between Successive Read Operations	t_{10}		500	–	–	ns

NOTES:
1. Full Scale TC = ΔFS/ΔT, where ΔFS is Full Scale change from T_A = +25°C to T_{MIN} or T_{MAX}.
2. All timing input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Timing signal t_3 and t_6 are defined as the time required for the output to cross 0.8V or 2.4V.
4. Timing signal t_7 is defined as the time required for the data lines to change 0.5V when loaded with a specified circuit.

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	A_{IN}	Analog Input.
2	V_{REF}	–5.25V; Voltage Reference Output.
3	AGND	Analog Ground.
4-11	D_{11}-D_4	Three-State Outputs; active when $\overline{CS}$ and $\overline{RD}$ are brought low.
12	DGND	Digital Ground.
13-16	$D_{3/11}$-$D_{0/8}$	HBEN (High Byte Enable Input) determines individual pin functions.

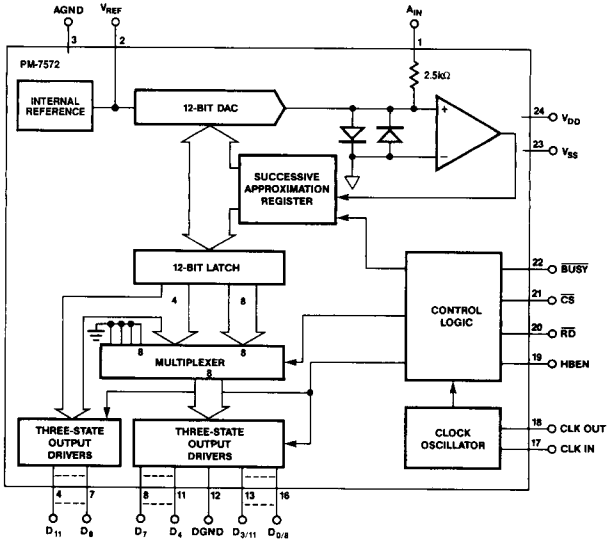
DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
HBEN = LOW	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
HBEN = HIGH	DB_{11}	DB_{10}	DB_9	DB_8	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8

*D_{11}-$D_{0/8}$ are the ADC's data output pins.
DB_{11}-DB_0 are the 12-bit conversion results; DB_{11} is the MSB.

17	CLK IN	Clock Input. Accepts a TTL compatible external clock, or crystal between pin 17 (CLK IN) and pin 18 (CLK OUT).
18	CLK OUT	Clock Output. An inverted CLK IN signal appears at this pin when an external clock is used.
19	HBEN	High Byte Enable Input. Multiplexes the 12-bit conversion results into the lower bit outputs, D_7-$D_{0/8}$ (4 MSBs or 8 LSBs). It also disables conversion start when HBEN is high.
20	$\overline{RD}$	Read Input. Active LOW, starts conversion if $\overline{CS}$ is also low and enables the output data three state drivers.
21	$\overline{CS}$	Chip Select Input. Active LOW, starts conversion if $\overline{RD}$ and HBEN are also low and enables the output data drivers.
22	$\overline{BUSY}$	$\overline{BUSY}$ Output. LOW when a conversion is in progress.
23	V_{SS}	Negative Supply, –15V.
24	V_{DD}	Positive Supply, +5V.

FUNCTIONAL DIAGRAM



CONVERTER OPERATION

The PM-7572 uses a successive approximation technique to convert an unknown analog input signal to a 12-bit digital output code. $\overline{CS}$, $\overline{RD}$, and HBEN control inputs are used to start a conversion. With HBEN low (or coincident with the $\overline{RD}$ input falling edge), the falling edge of $\overline{CS}$ and $\overline{RD}$ starts the conversion. Conversion start resets the internal successive approximation register (SAR) and enables the three-state output buffers.

The SAR sequences the voltage output DAC from the most-significant-bit (MSB) to the least-significant-bit (LSB). The analog input connects to the comparator via a 2.5kΩ resistor. The DAC, which has a 2.5kΩ output resistance, connects to the same comparator input. The comparator, performing a zero crossing detection, tests the addition of successively weighted bits from the DAC output versus the analog input signal. The MSB decision occurs after the second negative edge of the CLK IN following conversion initiation. The remaining 11-bit trials occur on the next 11 negative CLK IN edges.

Once a conversion cycle is started, it cannot be stopped or re-started without upsetting the remaining bit decisions. Every conversion cycle must have 13 negative CLK IN edges. At the end of conversion, the comparator input voltage is zero, and the SAR contains the 12-bit data word representing the analog input voltage. Data is then transferred from the SAR to the three-state output buffers when the $\overline{BUSY}$ line returns to logic high, signaling end of conversion.

CONTROL INPUTS SYNCHRONIZATION

Conversion time can vary from 12 to 13 CLK IN periods if the $\overline{RD}$ control input is not synchronized with the ADC clock. This delay can vary from zero to an entire clock period. To ensure a constant conversion time, $\overline{RD}$ must go low on either the rising edge of CLK IN or falling edge of CLK OUT. The delay between the falling edge of $\overline{RD}$ to the falling edge of CLK IN must not be less than 180ns to ensure 12.5 clock cycle conversion time, see Figure 1.

POWER-ON INITIALIZATION

During system power-up, the PM-7572 comes up in a random state. Once the clock is operating or an external clock is applied, the first valid conversion begins with the application of a high-to-low transition of both $\overline{CS}$ and $\overline{RD}$. The next 13 negative clock edges completes the first conversion producing valid data at the digital outputs. This is important in battery operated systems where power supplies are shut down between measurements.

DRIVING ANALOG INPUT

During conversion, the internal DAC output current modulates the analog input at the CLK IN frequency. For accurate conversions, the analog input to the PM-7572 must not change during the conversion periods. This requires an external buffer with low output impedance at the CLK IN frequency. Suitable devices meeting this requirement include the OP-27, OP-42, and SMP-11.

CLOCK OSCILLATOR

A simplified clock oscillator diagram for the PM-7572 is shown in Figure 2. As shown, an external crystal can be used between pins 17 and 18 to generate the internal clock signal required for the ADC. Capacitance values, C_1 and C_2, depend on the crystal or ceramic resonator manufacture and varies typically from 30pF and 100pF.

The CLK IN input accepts a TTL compatible external clock signal. The external clock must have a 45% to 55% duty cycle. No connection is necessary for the CLK OUT pin.

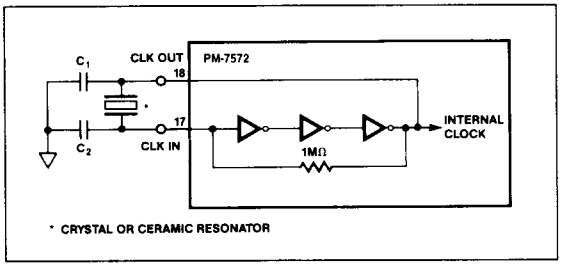


FIGURE 2: *Simplified Internal Clock Circuit*

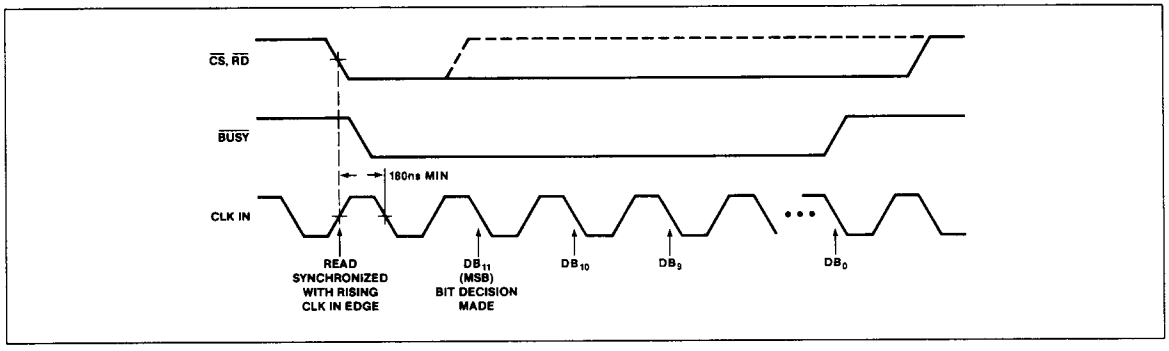


FIGURE 1: *External Clock Input Synchronization*

INTERNAL REFERENCE

The PM-7572 has an internal reference that provides the internal DAC with its reference voltage. This reference voltage is also made avilable at Pin 2 with a current sink capability of 500µA. The reference is internally trimmed during manufacture to –5.25V ± 1%, and is temperature compensated to minimize drift over temperature.

The PM-7572's reference pin (Pin 2) should be bypassed to AGND (Pin 3) with a 47µF capacitor in parallel with a 0.1µF capacitor.

UNIPOLAR OPERATION

The PM-7572's input to output transfer function is shown in Figure 3. Its output code is binary, and for a 0V to +5V analog input, the output code for 1 LSB = FS/4096 = 5/4096 = 1.22mV. The maximum full-scale input voltage for a 5V analog input is FS x 4095/4096 = 5 x 4095/4096 = 4.9988V. Code transitions occur halfway between successive integer LSB values; for example, 0.5 LSB, 1.5 LSB, 2.5 LSB ... FS - 1.5 LSBs.

OFFSET AND FULL-SCALE ERROR ADJUSTMENT, UNIPOLAR OPERATION

Full-scale error and offset error may need to be adjusted to 0V in those applications requiring absolute accuracy. This can be easily accomplished by using several external components as shown in Figure 4. This is also the unipolar mode of operation configuration. Zero offset error must be adjusted first. It is adjusted by applying 0.61mV (1/2 LSB for a 5V analog input) to V_{IN} and adjusting the op amp offset until the PM-7572's output code toggles between 0000 0000 0000 and 0000 0000 0001.

The full-scale error adjustment is performed by applying 4.99817V (equivalent to FS - 1.5 LSB) at V_{IN} and adjusting the full-scale adjust pot until the PM-7572's output toggles between 1111 1111 1110 and 1111 1111 1111.

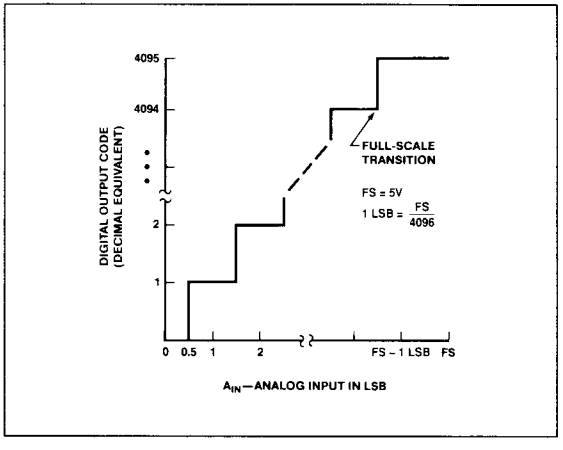


FIGURE 3: *Input/Output Transfer Function*

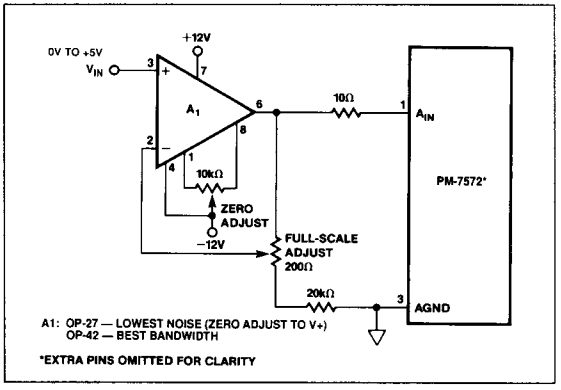


FIGURE 4: *Unipolar 0V to +5V Operation with Zero and Full-Scale Adjust*

BIPOLAR ANALOG INPUT OPERATION

Bipolar operation is achieved with an external amplifier that provides an analog offset voltage of 2.5V. If desired, a sample-and-hold can replace the amplifier. Figure 5 shows a circuit that provides offset binary, and Figure 6 complementary offset binary.

In Figure 5, offset binary coding is produced when the external amplifier is connected in the noninverting mode. The op amp transfer function is shown in Figure 7 and is given by:

$A_{IN} = V_{IN} + 2.5V$

The analog input voltage range is ±2.5V; an LSB is equal to 1.22mV.

In Figure 6, complementary offset binary coding is produced when the external amplifier is connected in the inverting mode. The op amp transfer function is also shown in Figure 7 and is given by:

$A_{IN} = -V_{IN} + 2.5V$

The analog input voltage range is also ±2.5V and an LSB 1.22mV.

If other values of the analog input signal are desired, change R_3 and R_4 in Figure 5 and R_2 in Figure 6. Regardless of resistor values chosen, the full range of 0V to +5V at A_{IN} must be maintained.

To obtain good performance over temperature in these configurations, the scaling resistors chosen should be of the same type and from the same manufacture, and be 0.1% tolerance.

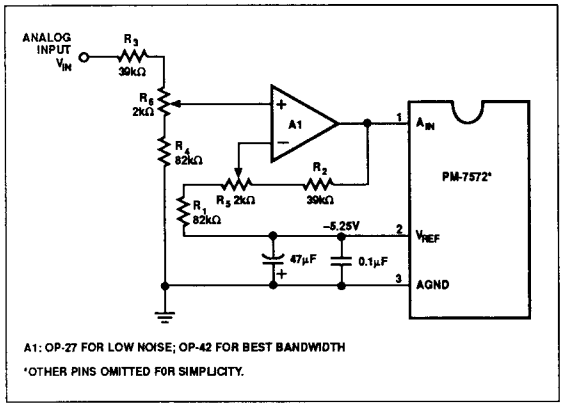


FIGURE 5: *Bipolar Operation (Offset Binary)*

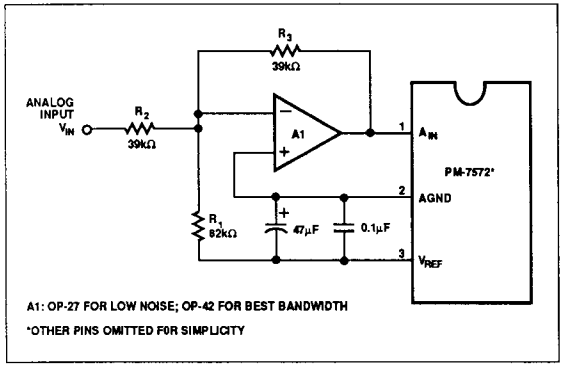


FIGURE 6: *Bipolar Operation (Complementary Offset Binary)*

OFFSET AND FULL-SCALE ERROR ADJUSTMENT BIPOLAR OPERATION

As with the unipolar adjustment, zero adjustment is performed first. Referring to Figure 5, apply 0.61mV (±1/2 LSB) analog input to V_{IN} and adjust R_5 until the successive digital output codes toggle between 1000 0000 0000 and 1000 0000 0001.

For the inverting configuration, Figure 6, replace R_1 with a potentiometer and adjust the output to toggle between 0111 1111 1111 and 0111 1111 1110.

Full-scale is adjusted (for Figure 5) by applying a FS - 1.5 LSB analog input signal to V_{IN} (for Consistency) and adjust R_6 until the successive digital output codes toggle between 1111 1111 1110 and 1111 1111 1111.

For Figure 6, apply 2.49817V at V_{IN} and adjust R_2 until the output code varies between 0000 0000 0001 and 0000 0000 0000.

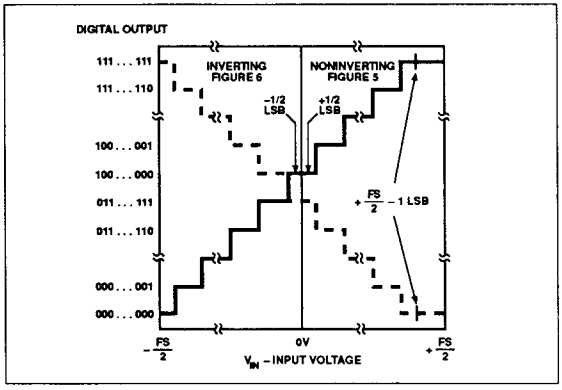


FIGURE 7: *Ideal Input/Output Transfer Characteristics for Bipolar Input Circuits*

DATA FORMAT

The PM-7572 has self-contained logic for both 8-bit and 16-bit data bus interfacing. Data output can be formatted into either a 12-bit parallel word for 16-bit data bus systems, or two byte word for an 8-bit data bus. The format is selected with HBEN that controls an internal multiplexer.

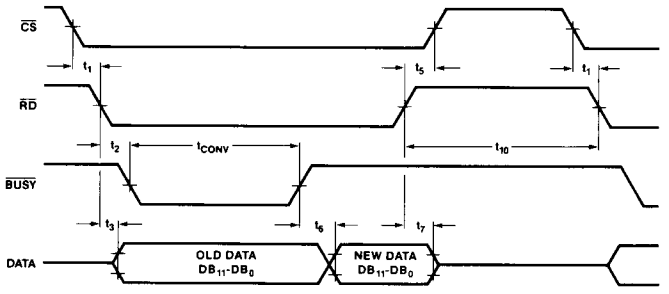
With HBEN LOW, converted data is directed to D_{11} ... $D_{0/8}$ outputs for the 12-bit data format. For two byte operation, data is presented to D_7 ... $D_{0/8}$ outputs. With HBEN LOW, the lower 8 bits are presented to the data outputs, and when HBEN goes high, the upper 4 bits are presented to the outputs with the leading 4 bits being low for D_7 ... $D_{0/8}$. See Pin Description table for pins 13-16. Note that the 4 MSBs always appear at the digital outputs D_{11} ... D_8 whenever the outputs are enabled, regardless of the state of HBEN.

CONVERSION MODES

The PM-7572's versatile processor interfacing offers two A/D conversion modes of operation for both data bus sizes. It offers the Slow-Memory mode and ROM mode. Processors that can be forced into WAIT states for the PM-7572's conversion time, can use the Slow-Memory mode. Other processors that cannot be forced into WAIT states can use the ROM mode. In both modes, a processor READ operation to the ADC address starts the conversion. A second READ operation is required to access the conversion result in the ROM mode.

SLOW-MEMORY MODE, PARALLEL READ (HBEN = LOW)

Slow-Memory mode is the simplest mode to use. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results.



SLOW-MEMORY MODE, PARALLEL READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

FIGURE 8: *Parallel Read Timing Diagram, Slow-Memory Mode (HBEN = LOW)*

If the system throughput tolerates WAIT states and the hardware is correct, then Slow-Memory mode is virtually immune to subsequent software modifications. Placing the microprocessor in the WAIT state has the additional advantage of quieting digital systems to reduce noise pickup, especially in analog conversion circuitry. The Slow-Memory, 12-bit parallel mode provides the fastest analog sampling and digital data transfer rate for sampled data systems. The timing diagram and data bus status are shown in Figure 8.

The conversion process starts when $\overline{CS}$ and $\overline{RD}$ are taken low, the PM-7572 acknowledges that conversion is taking place by taking BUSY low. During this conversion period, data from the previous conversion appears at the digital outputs. At the end of conversion, the output latches are updated and the conversion result is placed on data outputs D_{11} ... $D_{0/8}$, BUSY returns high.

SLOW-MEMORY MODE, TWO BYTE READ

Slow-Memory mode can also be used for 8-bit data bus systems. The operation is the same as for the Slow-Memory mode, parallel load, with the addition of a second memory read with HBEN HIGH. The first read, with HBEN LOW, places the end of conversion data on the low data outputs, DB_7 ... DB_0. The second read,with HBEN HIGH, places the high byte data on outputs $D_{3/11}$ ... $D_{0/8}$, and disables conversion start. The timing diagram and data bus status are shown in Figure 9.

ROM MODE, PARALLEL READ (HBEN = LOW)

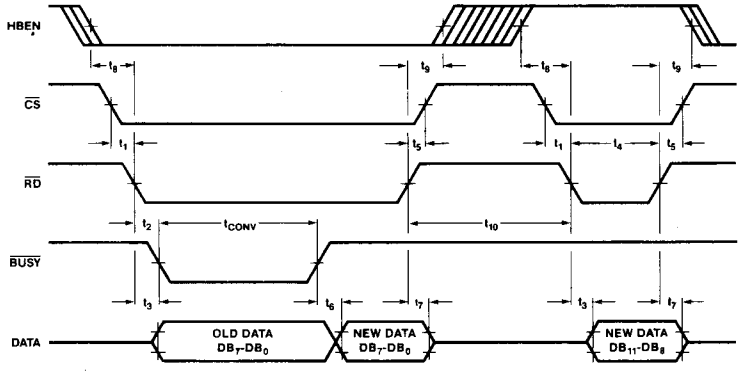
The ROM mode operates the same as for the Slow-Memory mode except that a second READ is taken. This mode avoids placing the microprocessor into a wait state. The first READ starts the conversion and places 12 bits of previous conversion on data outputs D_{11} ... $D_{0/8}$. This data, if not required, can be discarded. The second READ operation reads the new data, D_{11} ... DB_0, and starts another conversion. See the timing diagram and data bus status in Figure 10. The second read operation must have a delay time of at least as long as the PM-7572's conversion time.

ROM MODE, TWO BYTE READ

Data outputs D_7 ... $D_{0/8}$ are used for the two-byte READ mode. Conversion is started by taking READ LOW with HBEN LOW. The 8 LSBs from a previous conversion is then placed on the data outputs; this data can be discarded if not used. The new conversion results are then obtained with two more READ operations. The second READ operation, with HBEN HIGH, stops the conversion and places the high byte (4 MSBs) on the data outputs $D_{3/11}$ ... $D_{0/8}$. See the timing diagram and data bus status in Figure 11. A delay equal to the PM-7572's conversion time must be allowed between conversion start and the second data READ operation.

MICROPROCESSOR INTERFACING

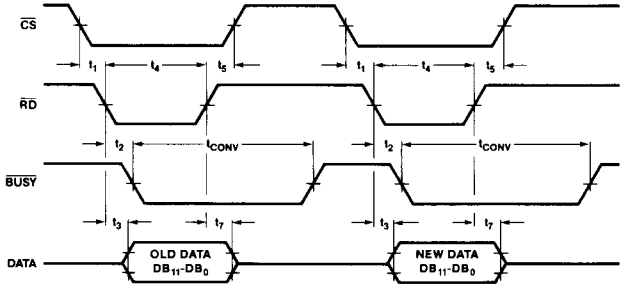
The PM-7572's interface structure allows interfacing to microprocessors as a memory mapped device. Control inputs, $\overline{CS}$ and $\overline{RD}$, are common to all peripheral memory interfacing. For 8-bit microprocessors, HBEN is connected to the microprocessor address bus for the data byte select. The PM-7572's 3-state data outputs allow direct connection to the data bus.



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8

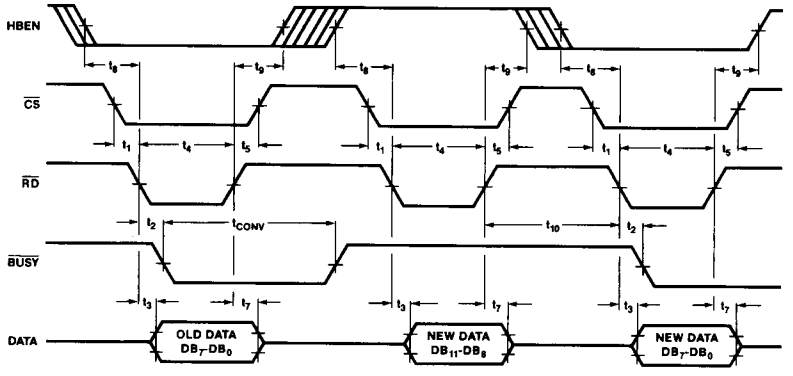
FIGURE 9: *Two-Byte Read Timing Diagram, Slow-Memory Mode*



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

FIGURE 10: *Parallel Read Timing Diagram, ROM Mode (HBEN = LOW)*



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8
THIRD READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

FIGURE 11: *Two-Byte Read Timing Diagram, ROM Mode*