CMOS PRESETTABLE UP/DOWN COUNTER

FEATURES

- Binary or Decade Up/Down Counting
- BCD Outputs in Decade Mode
- Asynchronous Preset Enable
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design
- 6MHz Counting Rate @ 10Vdc
- Carry Output for Cascading Stages

DESCRIPTION

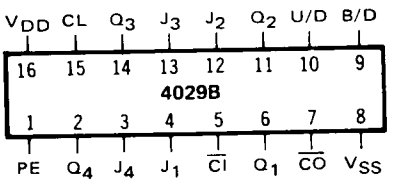
The 4029B consists of a four-stage Binary or BCD Decade Up/Down Counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A low on each Jam line, when the Preset/Enable signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable". The Carry-in terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the Binary/Decade input is high; the counter counts in the Decade mode when the Binary/Decade input is low. The counter counts up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel-clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and difference counting and programmable frequency synthesizer applications. It is also useful in A/D and D/A conversion techniques and for magnitude and sign generation.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

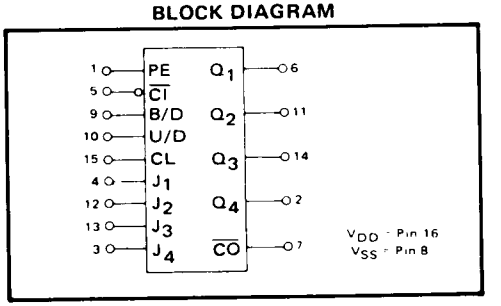
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

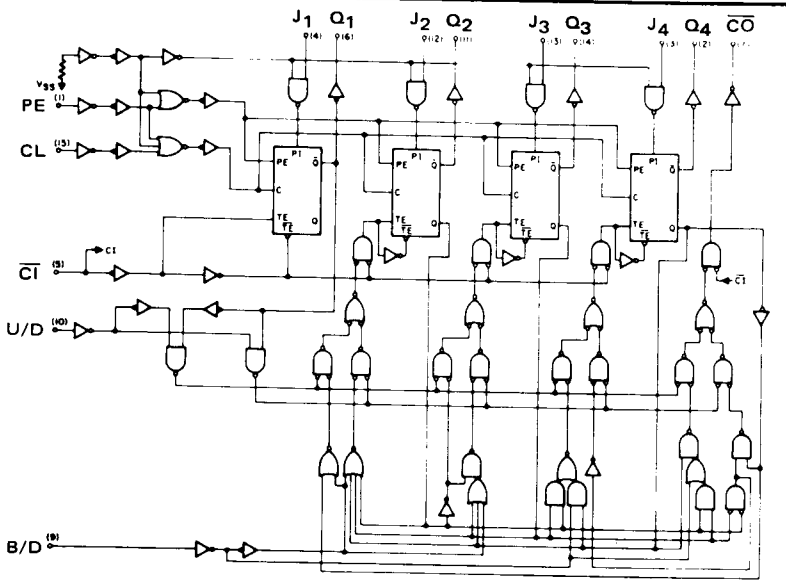
$\overline{CI}$	U/D	PE	B/D	Action
1	X	0	X	No Count
0	1	0	0	Count Up (Decade)
0	1	0	1	Count Up (Binary)
0	0	0	0	Count Down (Decade)
0	0	0	1	Count Down (Binary)
X	X	1	X	Preset

X = Don't Care

BLOCK DIAGRAM

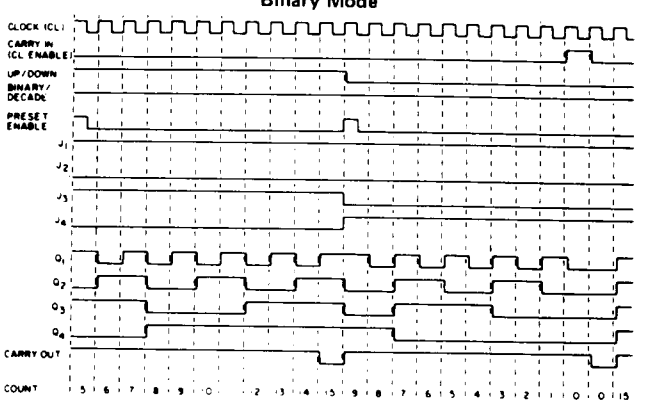


LOGIC DIAGRAM

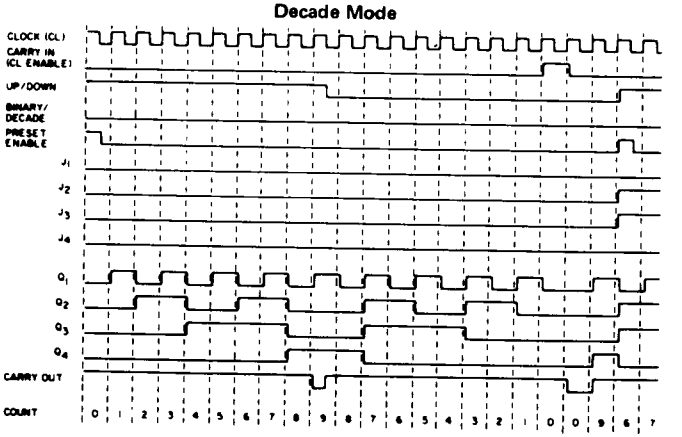


TIMING DIAGRAMS

Binary Mode



Decade Mode



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

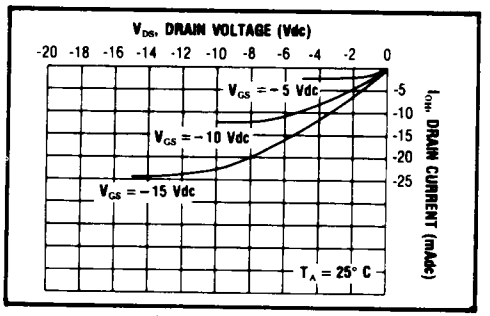
NOTES: [1] Remaining Static Characteristics are listed under "4000B Series Family Specifications"

[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

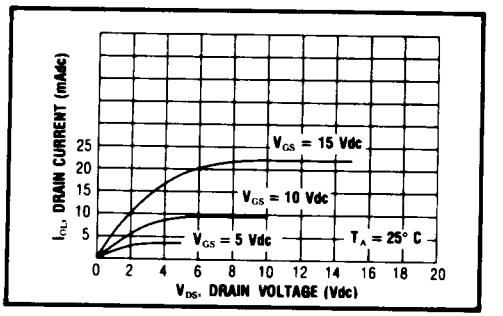
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	120	240	
		15	–	90	180	
Clock to $\overline{\text{Carry Out}}$		5	–	280	560	ns
		10	–	130	260	
		15	–	95	190	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$		5	–	170	340	ns
		10	–	70	140	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	170	340	ns
		10	–	85	170	
		15	–	70	140	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	4	–	MHz
		10	4.0	8	–	
		15	5.5	11	–	
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM SETUP TIME Carry In	t_{setup}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
Up/Down, B/D		5	–	325	650	ns
		10	–	115	230	
		15	–	85	170	
PRESET OPERATION						
PROPAGATION DELAY TIME Preset Enable to Q	t_{PLH}, t_{PHL}	5	–	360	720	ns
		10	–	140	280	
		15	–	110	220	
Preset Enable to $\overline{\text{Carry Out}}$		5	–	410	820	ns
		10	–	165	330	
		15	–	130	260	
MINIMUM PRESET ENABLE PULSE WIDTH	PW_{PE}	5	–	170	340	ns
		10	–	85	170	
		15	–	70	140	
PRESET ENABLE REMOVAL TIME	t_{rem}	5	–	325	650	ns
		10	–	110	220	
		15	–	90	180	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



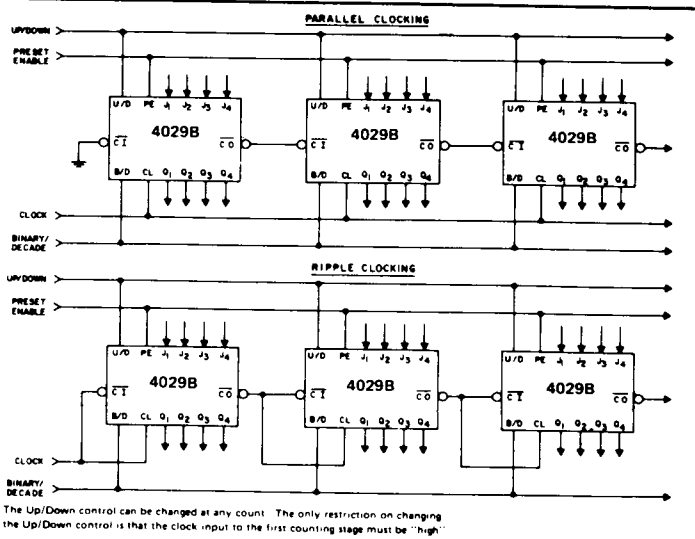
Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

APPLICATIONS INFORMATION

CASCADING CONNECTIONS



The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be "high".

PROGRAMMABLE CASCADED FREQUENCY DIVIDER