Si3226/27 + Si3208/09

DUAL PROSLIC® WITH DC-DC CONTROLLER

Features

- Performs all BORSCHT functions
- Ideal for short- or long-loop applications
- Internal balanced or unbalanced ringing
- Low power consumption
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Integrated dc-dc controller
- Wideband CODEC (Si3227)
- Low-power sleep mode
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- DTMF generator/decoder
- A-Law/µ-Law companding, linear PCM
- PCM and SPI bus digital interfaces with programmable interrupts
- GCI/IOM-2 mode support
- 3.3 V operation
- GR-909 loop diagnostics
- Audio diagnostics with loopback
- Pb-free/RoHS-compliant packaging

Ordering Information

See page 38.

Patents pending

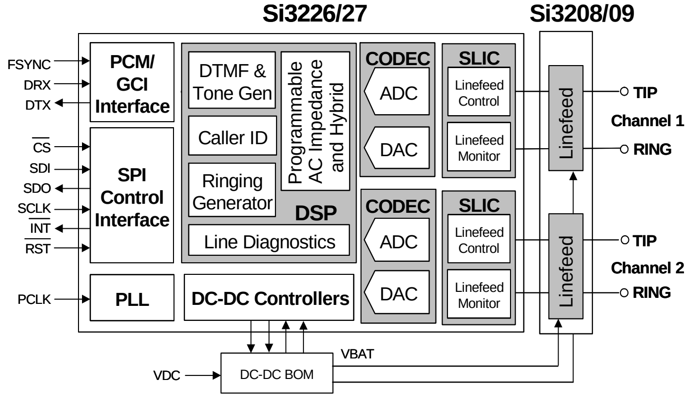
Applications

- Customer Premises Equipment (CPE)
- Optical Network Terminals (ONT)
- Private Branch Exchange (PBX)
- Cable EMTAs, ATAs, VoIP Gateways

Description

The Si3226/27 Dual ProSLIC® chipsets each consist of a low-voltage CMOS device integrating both SLIC and CODEC functionality in combination with a high-voltage linefeed IC (LFIC). The chipset provides two complete foreign exchange station (FXS) telephony interfaces. The Si3226/27 operate from a single 3.3 V supply and interface to standard PCM/SPI or GCI bus digital interfaces. A built-in dc-dc controller automatically generates the optimal battery voltage required for each line-state, optimizing efficiency and minimizing heat generation. Self-testing and metallic loop testing (MLT), e.g., GR-909, is facilitated by the built-in DSP, monitor ADC, and test load. The companion Si3208/09 LFICs are available with voltage ratings up to –135 V to support high power ringing and the Si3227 supports wideband audio for better-than-PSTN voice quality (see Ordering Guide below). The Si3226/27 are available in a 64-pin thin quad flat package (TQFP); the LFICs are available in a 40-pin quad, flat, no-lead package (QFN).

Functional Block Diagram



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1. Electrical Specifications

Table 1. Absolute Maximum Ratings and Thermal Information[1]

Parameter	Symbol	Test Condition	Value	Unit
Operating Temperature Range	T_A		–40 to 85	°C
Storage Temperature Range	T_{STG}		–55 to 150	°C
Thermal Resistance, Typical[2] TQFP-64	θ_{JA}		45	°C/W
Continuous Power Dissipation[3] TQFP-64	P_D	T_A = 85 °C	.88	W
Maximum Junction Temperature, Si3226/27	T_J		125	°C
Thermal Resistance, Typical[2] QFN-40	θ_{JA}		32	°C/W
Continuous Power Dissipation[4] QFN-40	P_D	T_A = 85 °C	1.87	W
Maximum Junction Temperature, Si3208/09[4]	T_J	Continuous	145	°C
Si3226/27				
Supply Voltage	V_{DD} V_{DDA}, V_{DDC}, V_{DDD}		–0.5 to 4.0	V
Digital Input Voltage	V_{IND}		–0.3 to 3.6	V
Si3208				
Supply Voltage	V_{DD}		–0.5 to 4.0	V
Battery Supply Voltage[5]	V_{BAT}		+0.4 to –115	V
TIP or RING Voltage[6]	V_{TIP}, V_{RING}		–130	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA
Si3209				
Supply Voltage	V_{DD}		–0.5 to 4.0	V
High Battery Supply Voltage[5]	V_{BAT}		+0.4 to –140	V
TIP or RING Voltage[6]	V_{TIP}, V_{RING}		–140	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane.
3. Operation of the Si3226 or Si3227 above 125 °C junction temperature will degrade device reliability.
4. Si3208 and Si3209 are equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold should normally be set to 145 °C; when in the ringing state the thermal shutdown may be set to 200 °C. For optimal reliability long term operation of the Si3208/Si3209 above 150 °C junction temperature should be avoided.
5. The dv/dt of the voltage applied to the VBAT pins must be limited to 10 V/µs.
6. Specification requires protection circuit for surge event as shown in typical application circuit.

Table 2. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min[1]	Typ[1]	Max[1]	Unit
Ambient Temperature	T_A	F-grade	0	25	70	^oC
Ambient Temperature	T_A	G-grade	–40	25	85	^oC
Junction Temperature, Si3208/09	T_J		—	—	145	°C
Junction Temperature, Si3226/27	T_J		—	—	125	°C
Supply Voltage, Si3226/27	V_{DDA}, V_{DDC}, V_{DDD}		3.13	3.3	3.47	V
Supply Voltage, Si3208/09	V_{DD}		3.13	3.3	3.47	V
Battery Voltage, Si3208[2]	V_{BAT}		–110	—	–15	V
Battery Voltage, Si3209[2]	V_{BAT}		–136	—	–15	V

Notes:

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Operation at minimum voltage dependent upon loop conditions and dc-dc converter configurations.

Table 3. 3.3 V Power Supply Characteristics

(V_{DD} = 3.3 V, T_A = 0 to 70 ºC for F-Grade, –40 to 85 ºC for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Reset	I_{DD}	V_T and V_R = Hi-Z $\overline{RST}$ = 0	—	4.0	—	mA
	I_{VBAT}		—	0	—	mA
Supply Currents: High Impedance, Open	I_{DD}	V_T and V_R = Hi-Z	—	13.1	—	mA
	I_{VBAT}		—	.43	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V Automatic Power Save Mode Enabled	—	18.7	—	mA
	I_{VBAT}		—	1.2	—	mA
Supply Currents: Forward/Reverse Active, On-hook	I_{DD}	V_{TR} = –48 V Automatic Power Save Mode Disabled	—	27.7	—	mA
	I_{VBAT}		—	1.2	—	mA
Supply Currents: Forward/Reverse Active, Off-hook	I_{DD}	I_{LOOP} = 18 mA V_{BAT} = –12 V R_{LOAD} = 200 Ω Automatic Power Save Mode Disabled	—	43	—	mA
	I_{VBAT}		—	2.9 + 1.02*I_{LOOP}	—	mA
Supply Currents: Forward/Reverse OHT, On-hook	I_{DD}	V_{TR} = –48 V	—	40.2	—	mA
	I_{VBAT}		—	1.9	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z Automatic Power Save Mode Disabled	—	27	—	mA
	I_{VBAT}		—	0.43	—	mA
Supply Currents: Ringing	I_{DD}	V_{TR} = 55 V_{RMS} + 0 V_{DC} balanced, sinusoidal, f = 20 Hz V_{BAT} = –136 V R_{LOAD} = 5 REN = 1400 Ω	—	27.2	—	mA
	I_{VBAT}		—	5.6 + I_{AVE}	—	mA

Notes:
1. All specifications are for a single channel of Si3226/27 using Si3208/09 linefeed IC and based on measurements with all channels in the same operating state.
2. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.
3. I_{AVE} is the average of the full-wave rectified current in the subscriber loop during ringing ($I_{AVE} = I_{PEAK} \times 2/\pi$) = 36 mA under the test conditions shown for Ringing Current.
4. $I_{DD} = I_{DDD} + I_{DDA} + I_{DDC}$.

Table 4. AC Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level		2.5	—	—	V_{PK}
Overload Compression	2-Wire – PCM	See Figure 12			
Single Frequency Distortion[1]	2-Wire – PCM or PCM – 2-Wire: 200 Hz to 3.4 kHz	+35	+40	—	dB
	PCM – 2-Wire – PCM: 200 Hz – 3.4 kHz, 16-bit Linear mode	—	—	+63	dB
Signal-to-(Noise + Distortion) Ratio[2]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 11	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[2]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[2]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, Any gain setting	–0.2	—	0.2	dB
Attenuation Distortion vs. Frequency	0 dBm 0	See Figure 5 and 6			
Group Delay vs. Frequency		See Figure 7 and 8			
Gain Tracking[3]	1014 Hz sine wave, reference level –10 dBm Signal level:				
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
Crosstalk between channels	0 dBm0,				
TX or RX to TX	300 Hz to 3.4 kHz	—	—	–75	dB
TX or RX to RX	300 Hz to 3.4 kHz	—	—	–75	dB
2-Wire Return Loss[4]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[4]	300 Hz to 3.4 kHz	26	30	—	dB

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DDA}, V_{DDC}, V_{DDD} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.

Table 4. AC Characteristics (Continued)

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
Noise Performance					
Idle Channel Noise[5]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	–78	dBmP
PSRR from	VDDA, VDDD, VDDC = 3.3 V RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 kHz to 3.4 kHz	52	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability per Pin	Active off-hook 60 Hz REG 73 = 0x0B	—	25	—	mA_{RMS}

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DDA}, V_{DDC}, V_{DDD} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.

Table 5. Linefeed Characteristics
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω, R_{PROT} = 0 Ω I_{LOOP} = 18 mA, V_{BAT} = –52V	—	—	2000	Ω
DC Feed Current*		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance—Ringing	R_{RING}	$I_{LOOP} < I_{LIM}$	100	—	320	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Maximum Ringing Amplitude	V_{RING}	Si3208, Open circuit, V_{BAT} = –110 V	—	108	—	V_{PK}
		Si3209, Open Circuit, V_{BAT} = –136 V	—	134	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	Si3208: 60 V_{RMS}, 15 V offset, 0–5 REN Si3209: 55V_{RMS}, 48 V offset, 0–5 REN	—	1	—	%
Ringing Frequency Accuracy		f = 16 Hz to 100 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms

***Note:** Absolute value.

Table 5. Linefeed Characteristics (Continued)

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Voltage Sense Accuracy		Accuracy of boundaries for each output code; $V_{TIP} – V_{RING}$ = 48 V	—	2	4	%
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, I_{LOOP} = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%
***Note:** Absolute value.						

Table 6. Monitor ADC Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (8-bit resolution)	DNLE		—	1	—	LSB
Integral Nonlinearity (8-bit resolution)	INLE		—	1	—	LSB
Gain Error			—	5	—	%

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Table 7. Digital/Characteristics
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DD}	V
High Level Output Voltage	V_{OH}	DTX, SDO, SDITHRU, GPIO3a/b,GPIO1a/b, GPIO2a/b: I_O = 4 mA	V_{DD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	DTX, SDO, $\overline{INT}$, SDITHRU, GPIO3a/b: I_O = –4 mA	—	—	0.4	V
		GPIO1 a/b, GPIO2 a/b: I_O = –40 mA	—	—	0.72	
SDITHRU Internal Pullup Current			33	42	65	µA
Input Leakage Current	I_L		—	—	10	µA

Table 8. Switching Characteristics—General Inputs[1,2]
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{RESET}$	t_r	—	—	5	ns
$\overline{RESET}$ Pulse Width, GCI Mode[3,4]	t_{rl}	33/PCLK	—	—	µs
$\overline{RESET}$ Pulse Width, SPI Daisy Chain Mode[4]	t_{rl}	33/PCLK	—	—	µs

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. $\overline{RESET}$ input capacitance = 0.3 pF.
3. The minimum $\overline{RESET}$ pulse width assumes the SDITHRU pin is tied to ground via a pulldown resistor no greater than 10 kΩ per device.
4. The minimum $\overline{RESET}$ pulse width is 33/PCLK frequency (i.e. 33/8.192 MHz = 4 µs).

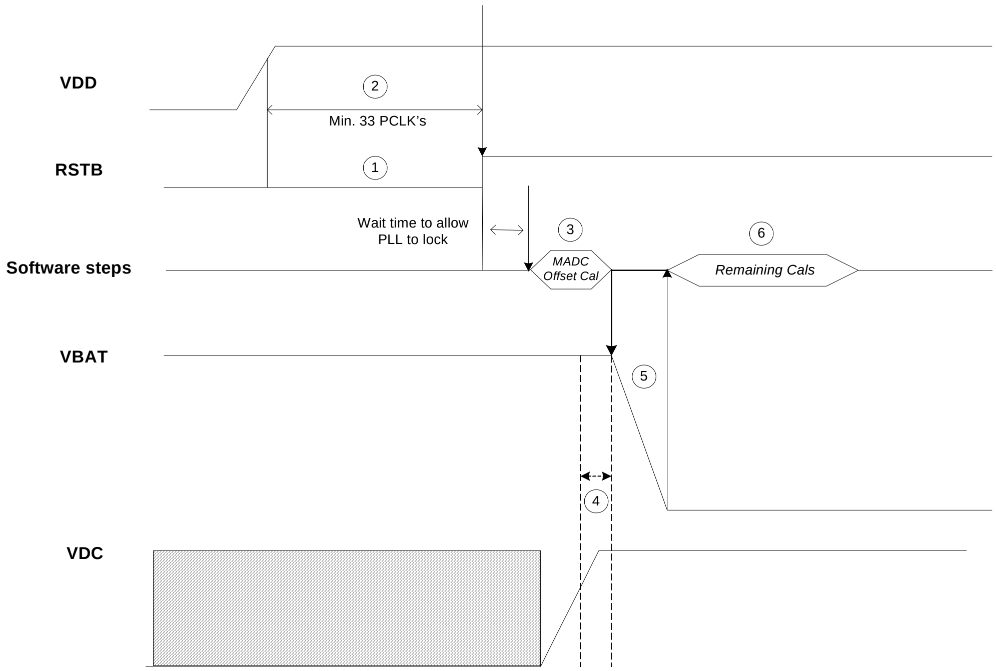


Figure 1. Powerup and Initialization Sequence

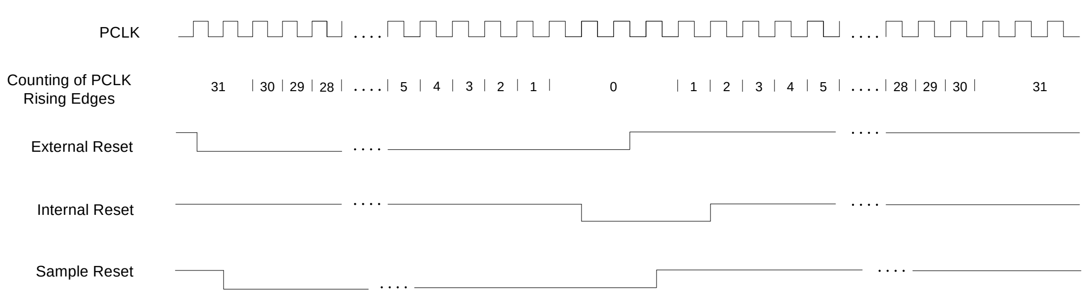
The following Powerup and Initialization Sequence must be followed:

1. VDD must be brought up while RSTB pin is held low.
2. Release RSTB at least 33 PCLK cycles after VDD.
3. Perform on-chip MADC offset calibration from OPEN state.
4. 10 ms is recommended prior to initializing the dc-dc converter after the MADC offset calibration. The VDC supply must be at the minimum valid voltage to ensure proper operation. The minimum valid voltage is shown in the application circuit schematic.
5. Bring up VBAT.
6. Perform remaining calibrations (except for common mode balance) from OPEN state.

Note: Repeat from step 3 whenever a hardware reset has been performed.

Powerdown Sequence:

1. Powerdown dc-dc converter.
2. Wait until VBAT is smaller than –10 V.
3. Turn off VDD.



Note: The count of PCLK rising edges during reset will be skewed by 1-2 clocks based on the internal sampling of reset.

Figure 2. Reset Timing Diagram

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Table 9. Switching Characteristics—SPI

(V_{DDA} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c		62	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{CS}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects	t_{cs}		220	—	—	ns
SDI to SDITHRU Propagation Delay	t_{d4}		—	4	10	ns

Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DDD} –0.4 V, V_{IL} = 0.4 V

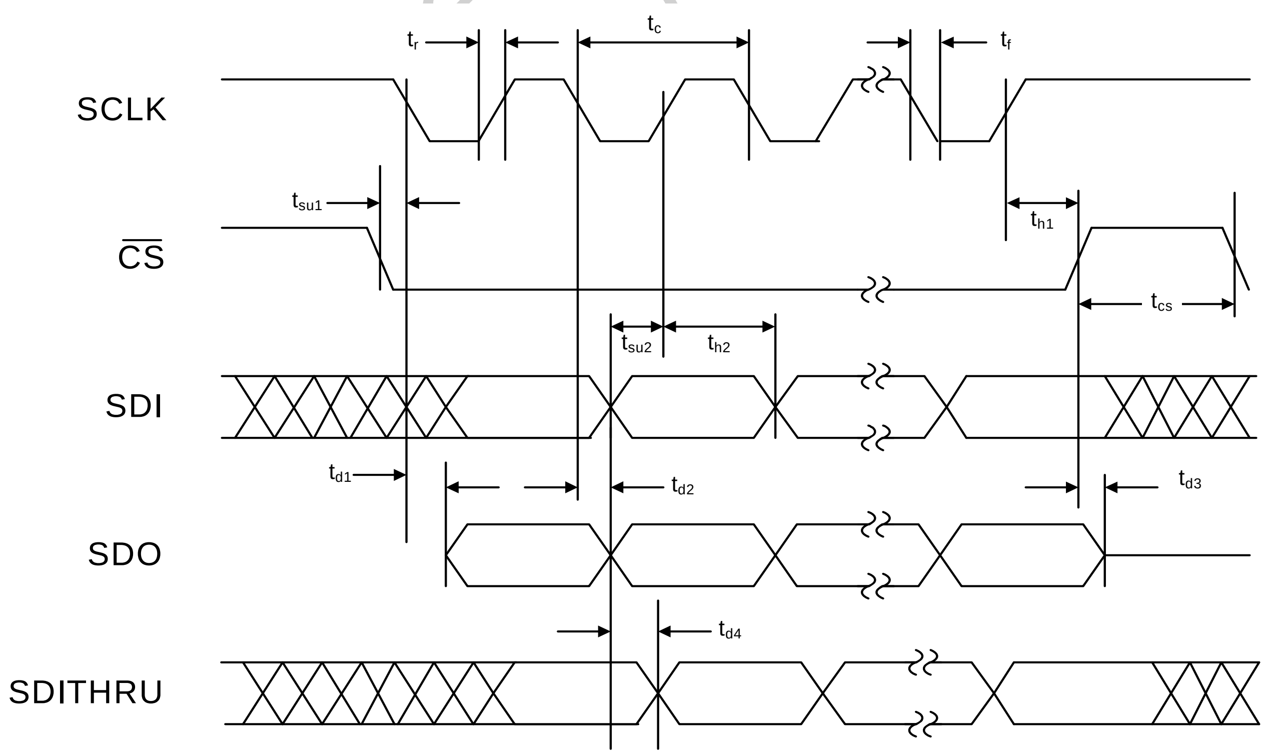


Figure 3. SPI Timing Diagram

Table 10. Switching Characteristics—PCM Highway Interface
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min[1]	Typ[1]	Max[1]	Units
PCLK Period	t_p		122	—	3906	ns
PCLK Jitter Tolerance	t_{jitter}		—	±8	—	ns
Valid PCLK Inputs[2]			— — — — — — — —	512 768 1.024 1.536 1.544 2.048 4.096 8.192	— — — — — — — —	kHz kHz MHz MHz MHz MHz MHz MHz
FSYNC Period[3]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-state[4]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	125 µs–t_p	

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} – V_{I/O}$ – 0.4 V, V_{IL} = 0.4 V.
2. A constant PCLK and FSYNC are required.
3. FSYNC source is assumed to be 8 kHz under all operating conditions.
4. Spec applies to PCLK fall to DTX tristate when that mode is selected.

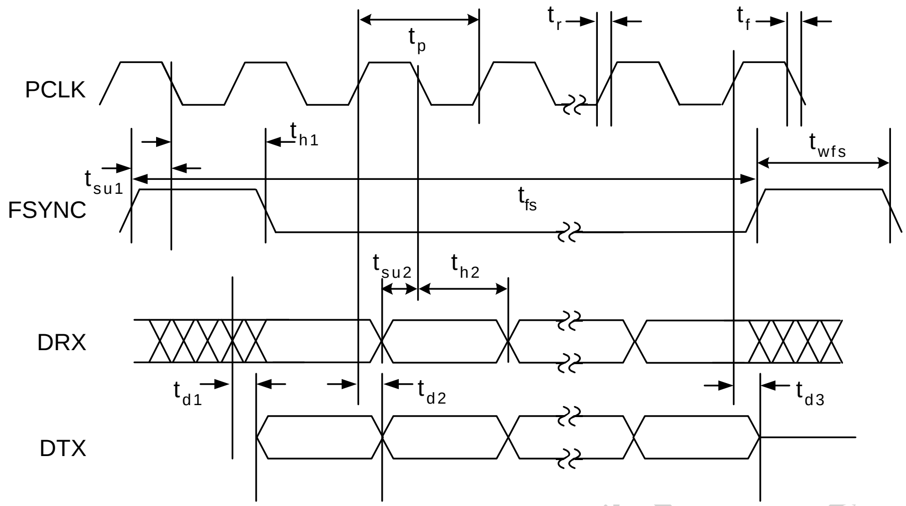


Figure 4. PCM Highway Interface Timing Diagram

Table 11. Switching Characteristics—GCI Highway Serial Interface
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
PCLK Period (2.048 MHz PCLK Mode)	t_p		—	488	—	ns
PCLK Period (4.096 MHz PCLK Mode)	t_p		—	244	—	ns
FSYNC Period[2]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
PCLK Jitter Tolerance	t_{jitter}		—	±8	—	ns
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tristate[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		$t_p/2$	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O - 0.4$ V and V_{IL} = 0.4 V. Rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC source is assumed to be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tristate when that mode is selected.

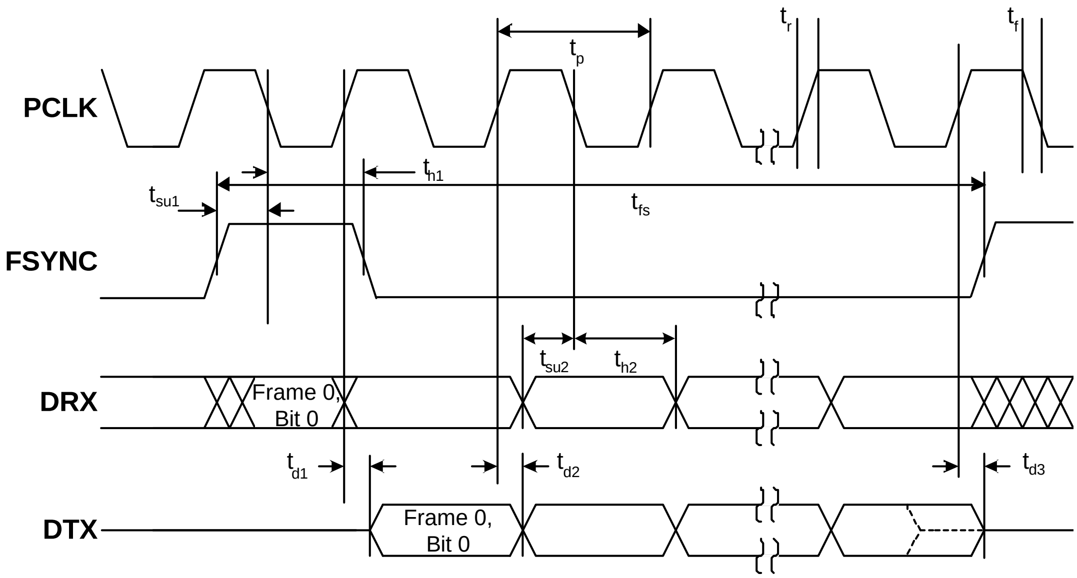


Figure 5. GCI Highway Interface Timing Diagram (2.048 MHz PCLK Mode)

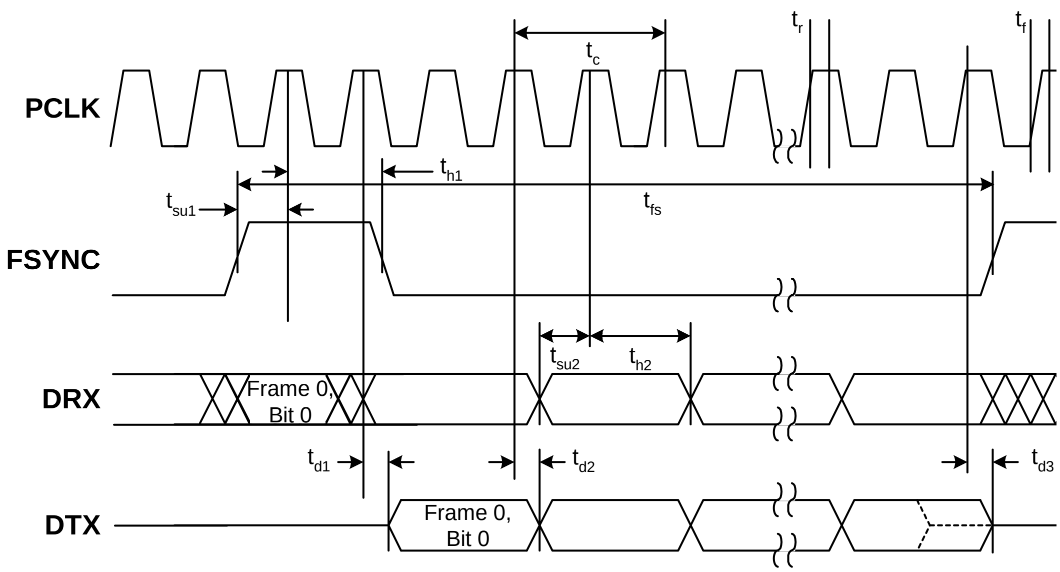


Figure 6. GCI Highway Interface Timing Diagram (4.096 MHz PCLK Mode)

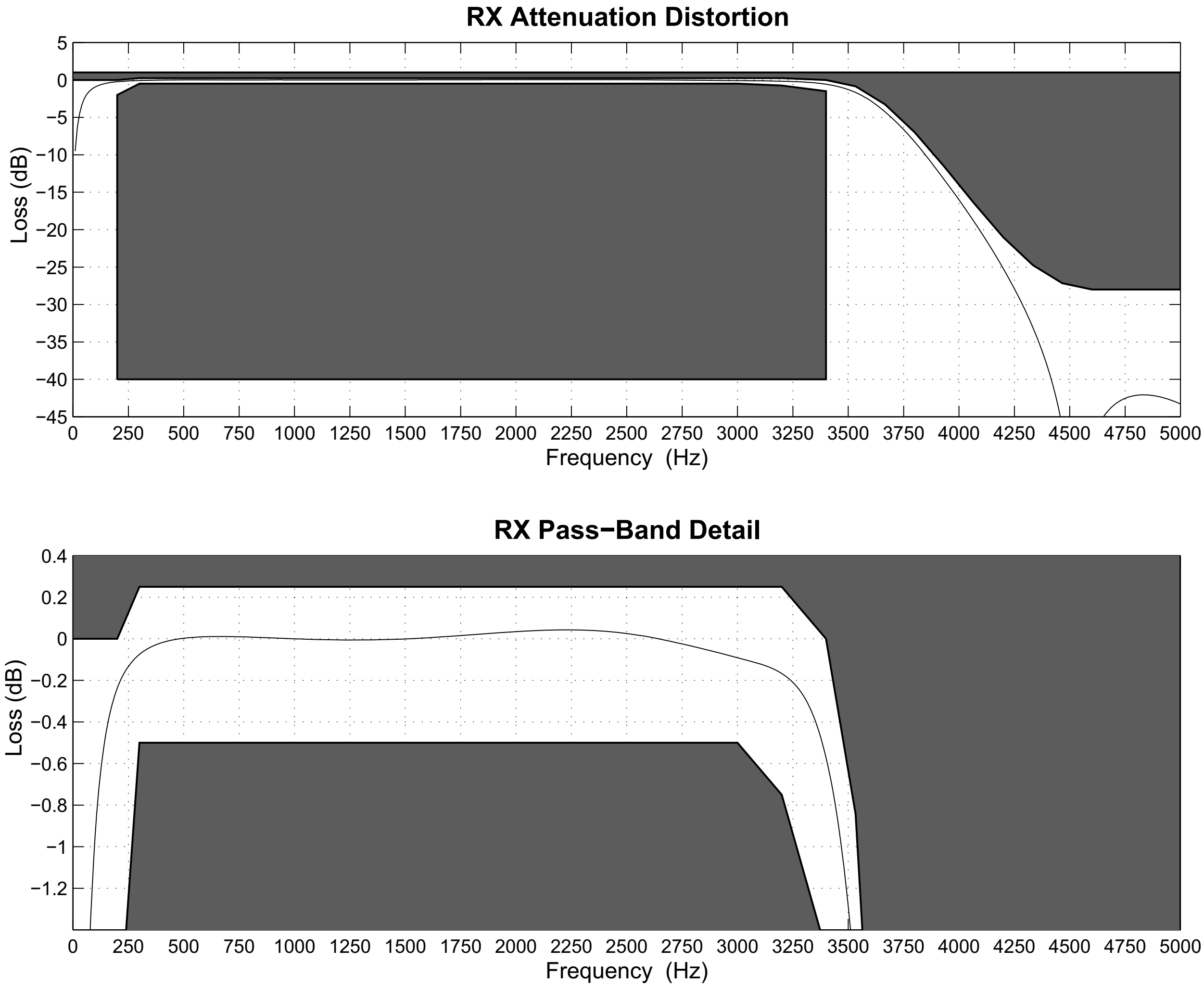


Figure 7. RX Attenuation Distortion

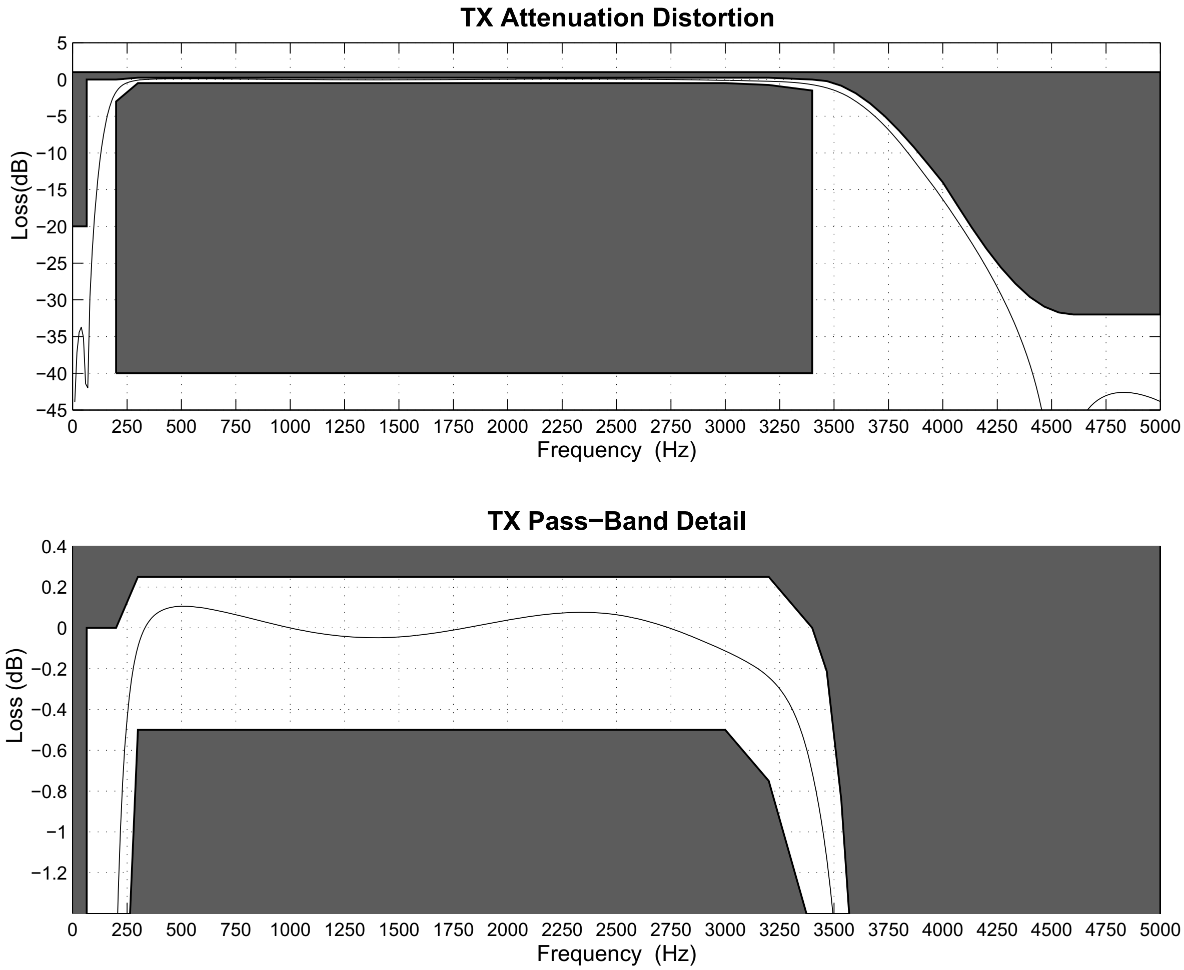


Figure 8. TX Attenuation Distortion

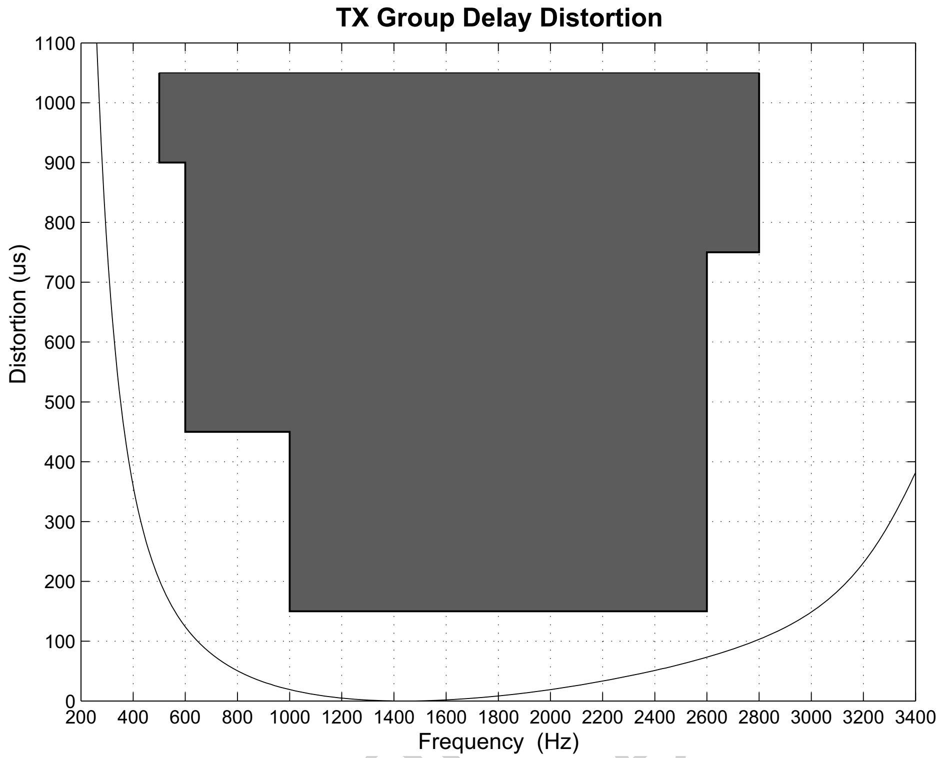


Figure 9. Transmit Group Delay Distortion

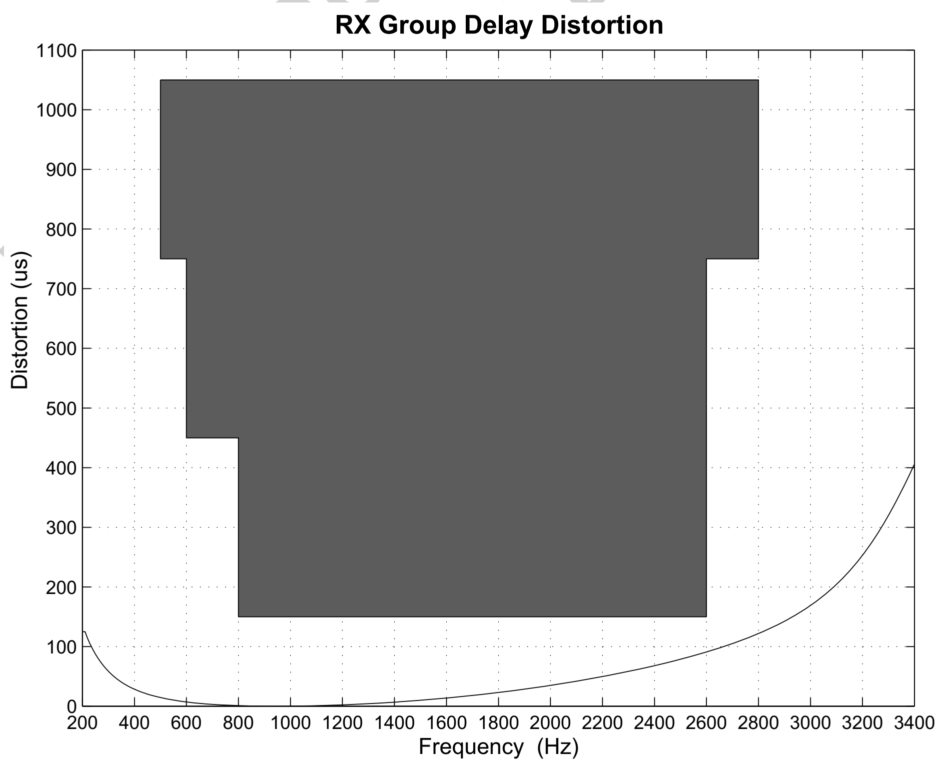


Figure 10. Receive Group Delay Distortion

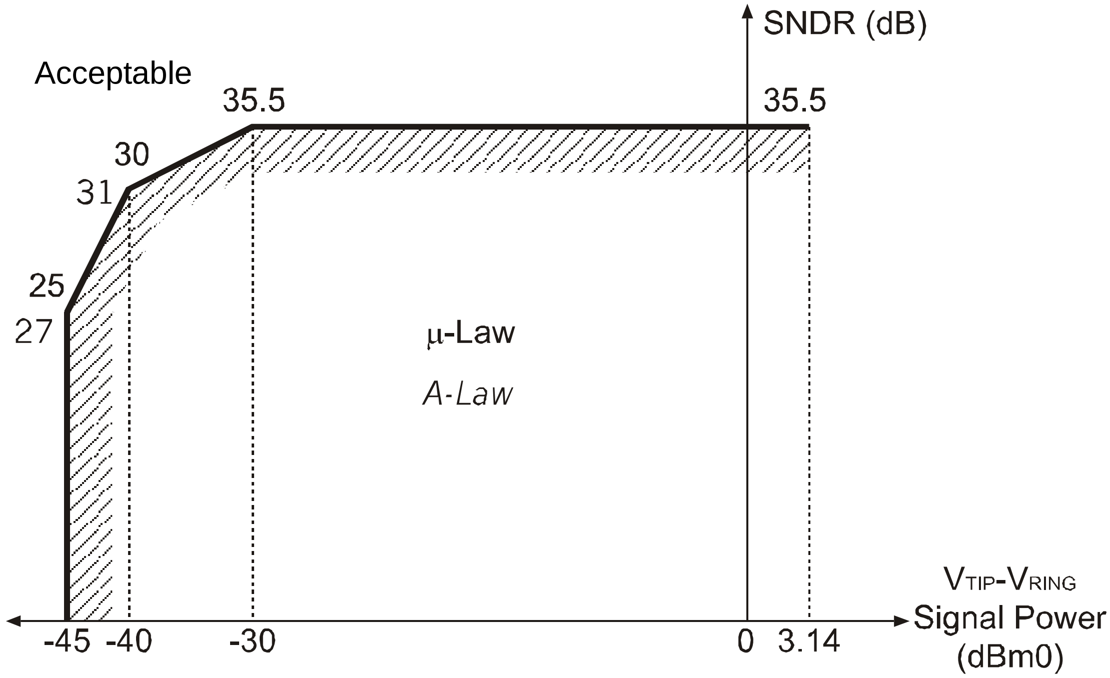


Figure 11. Transmit and Receive Path SNDR

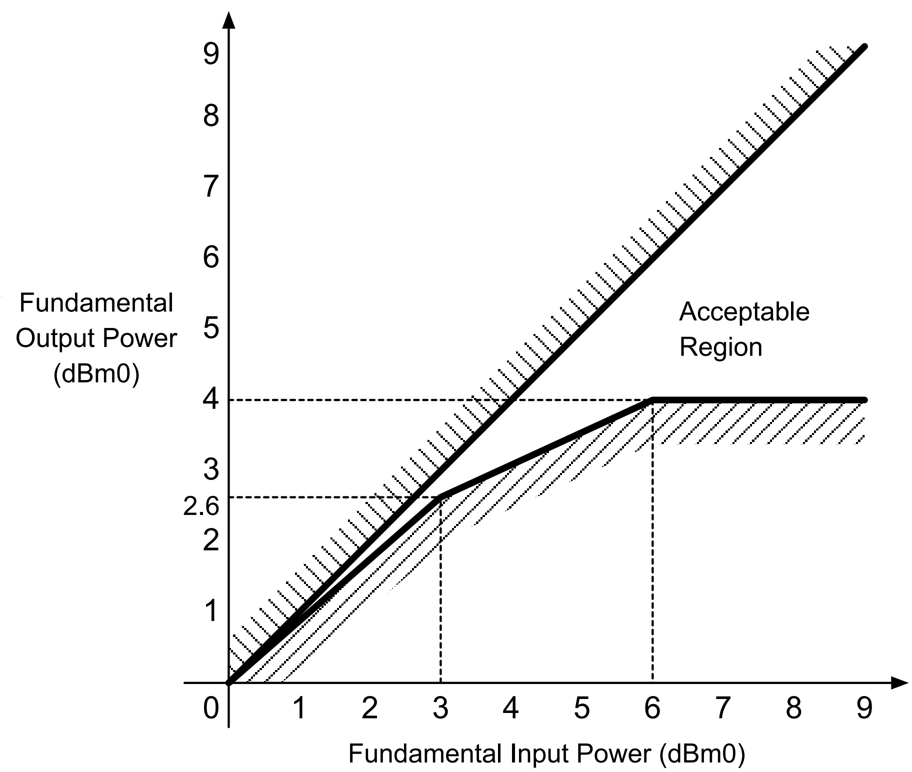


Figure 12. Overload Compression Performance

2. Typical Application Circuits

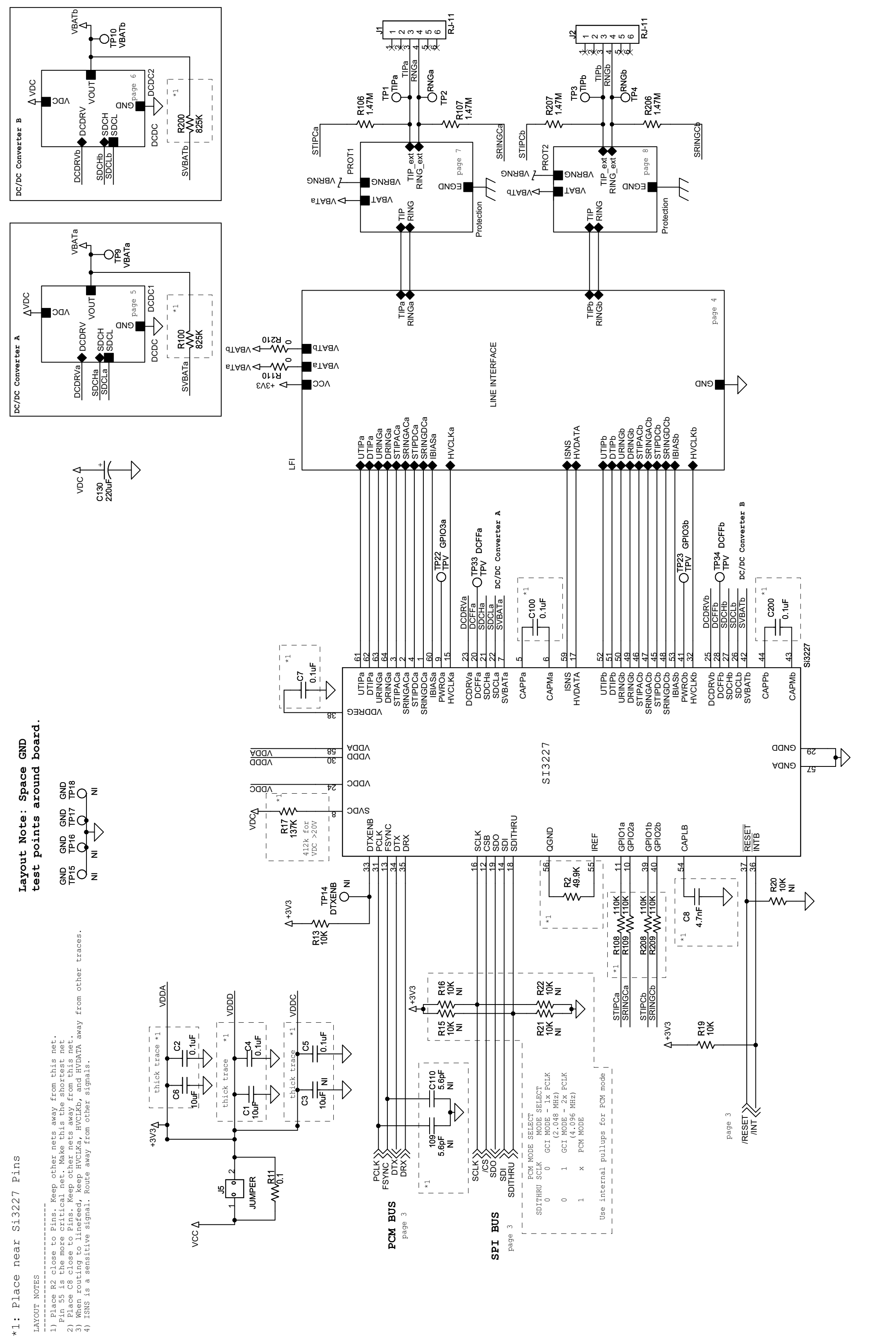


Figure 13. Si3226/27 (2 Lines)

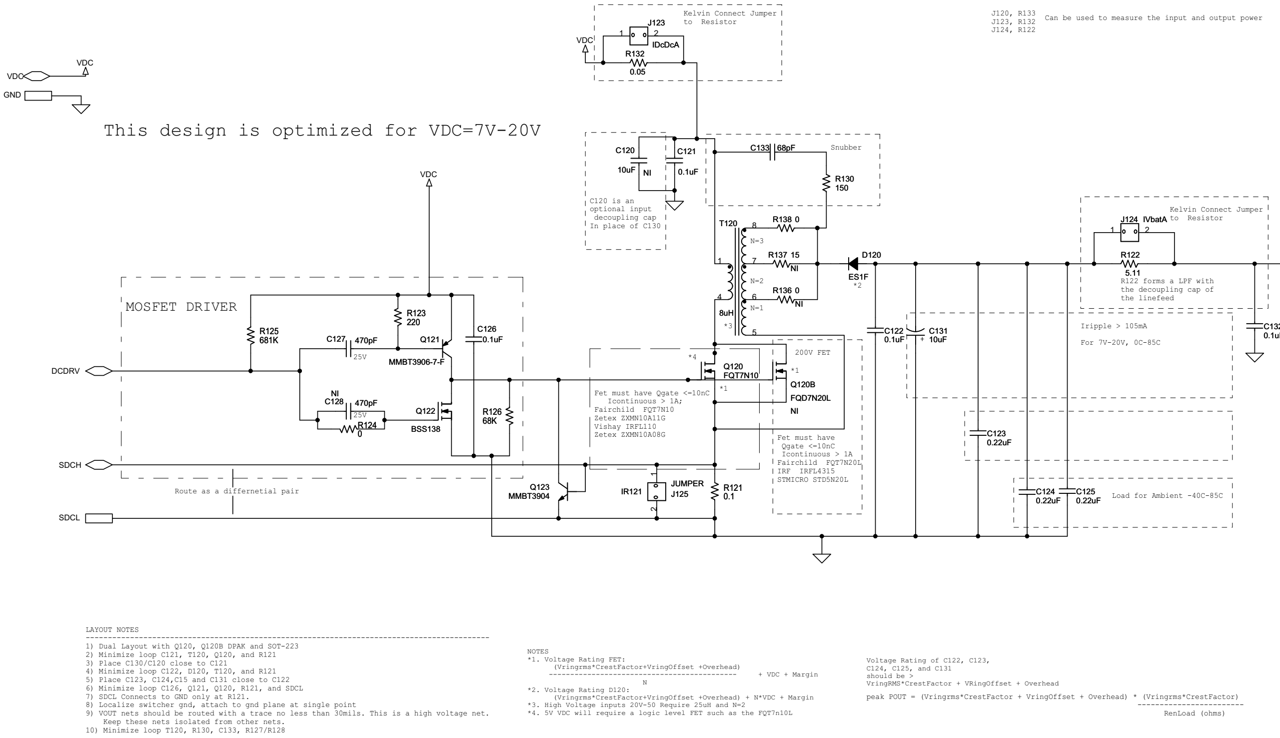


Figure 14. DC-DC Converter (A)

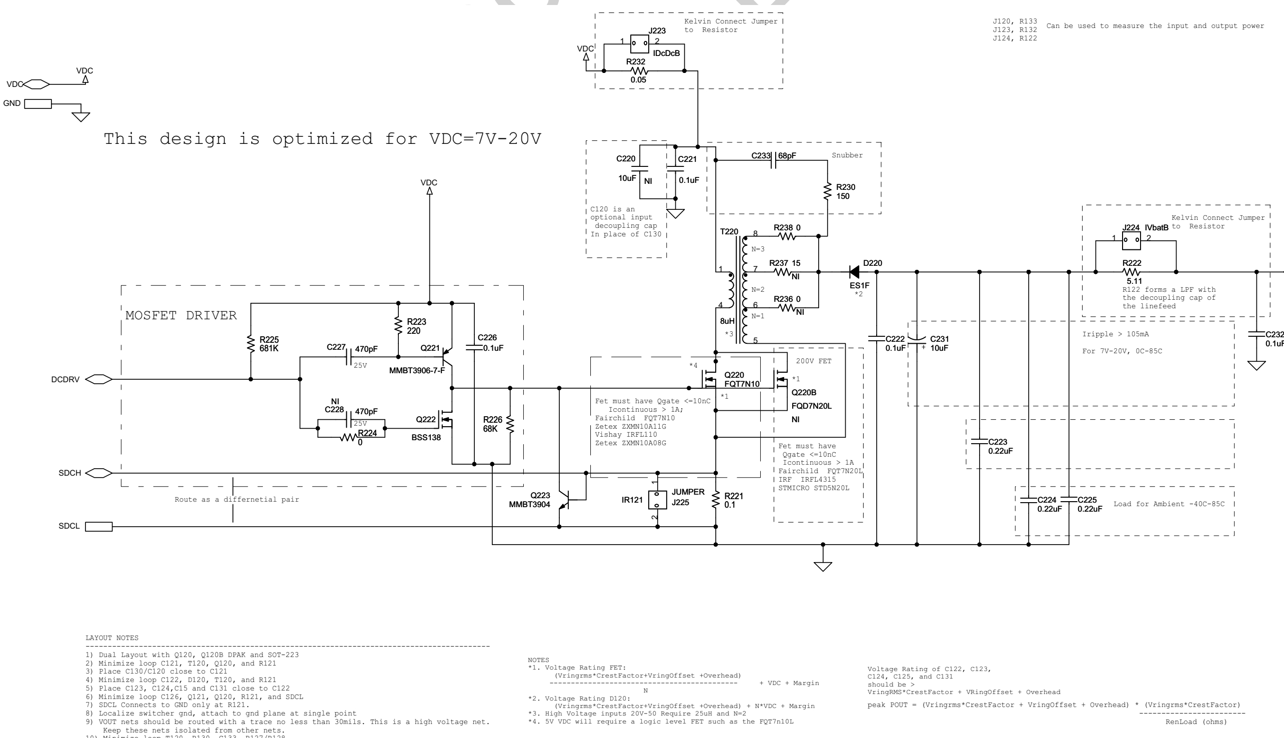


Figure 15. DC-DC Converter (B)

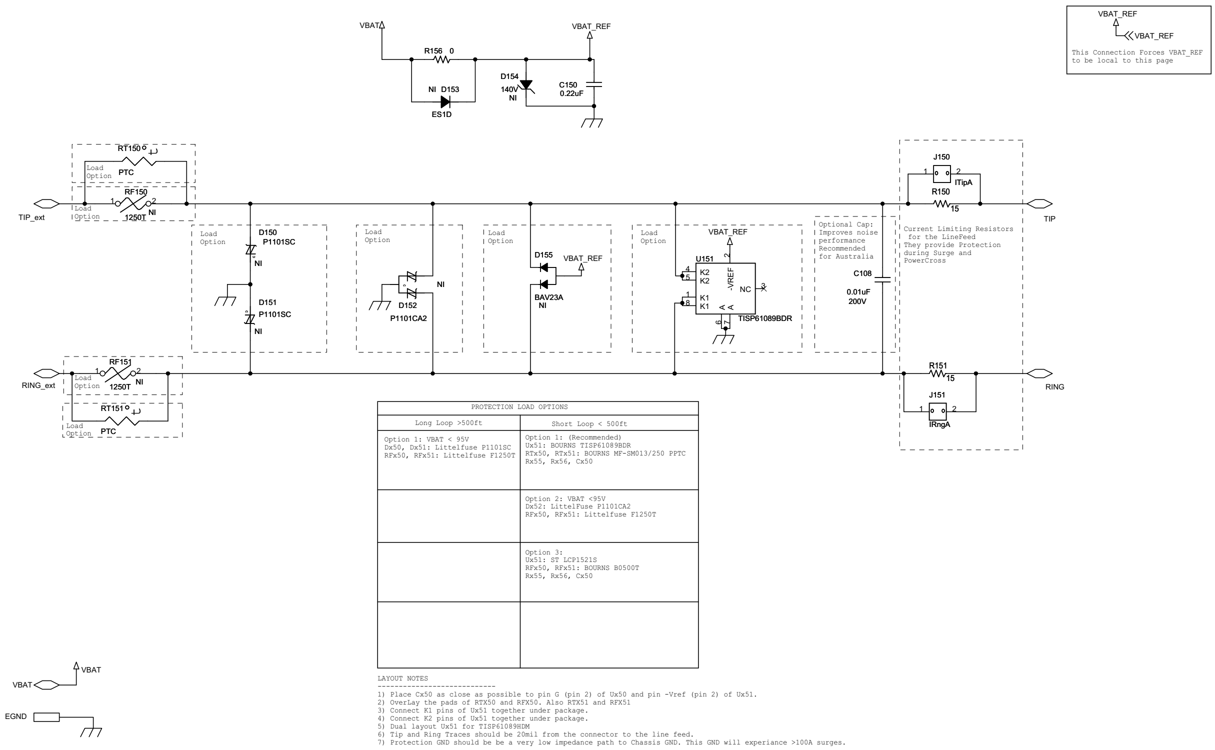


Figure 16. Protection (A)

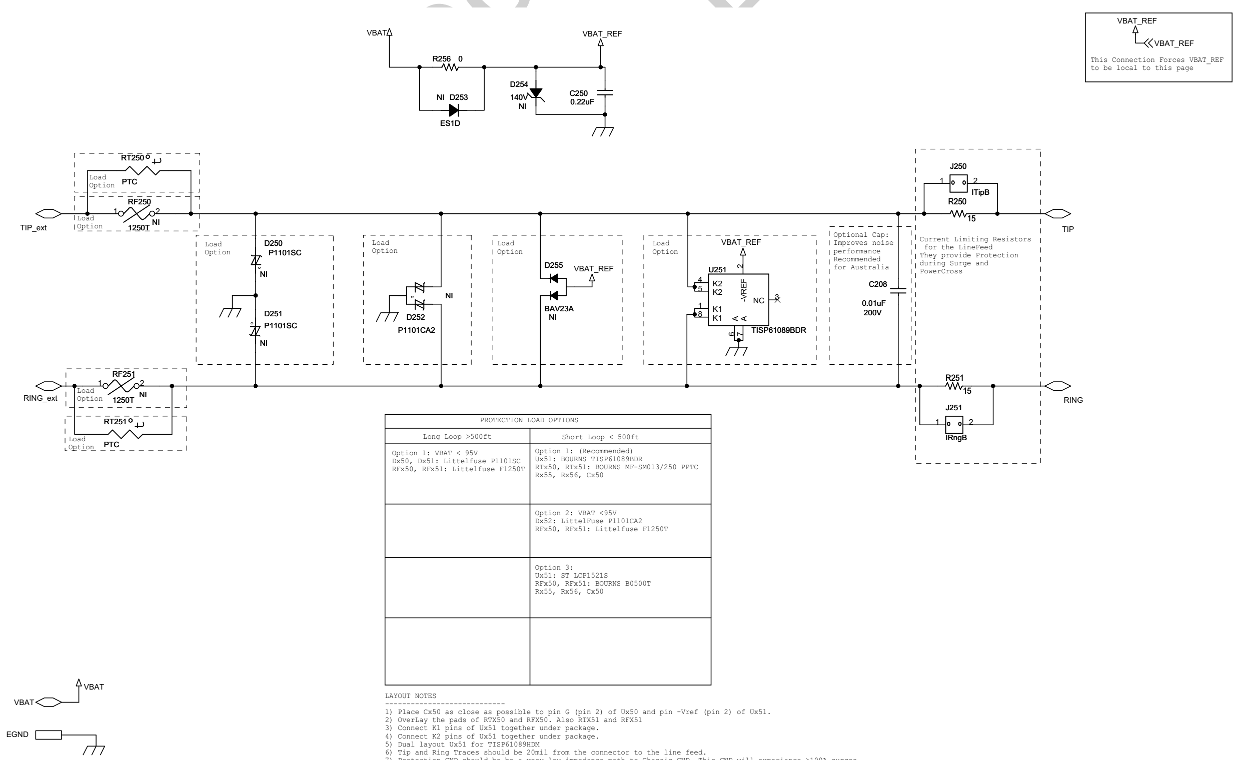


Figure 17. Protection (B)

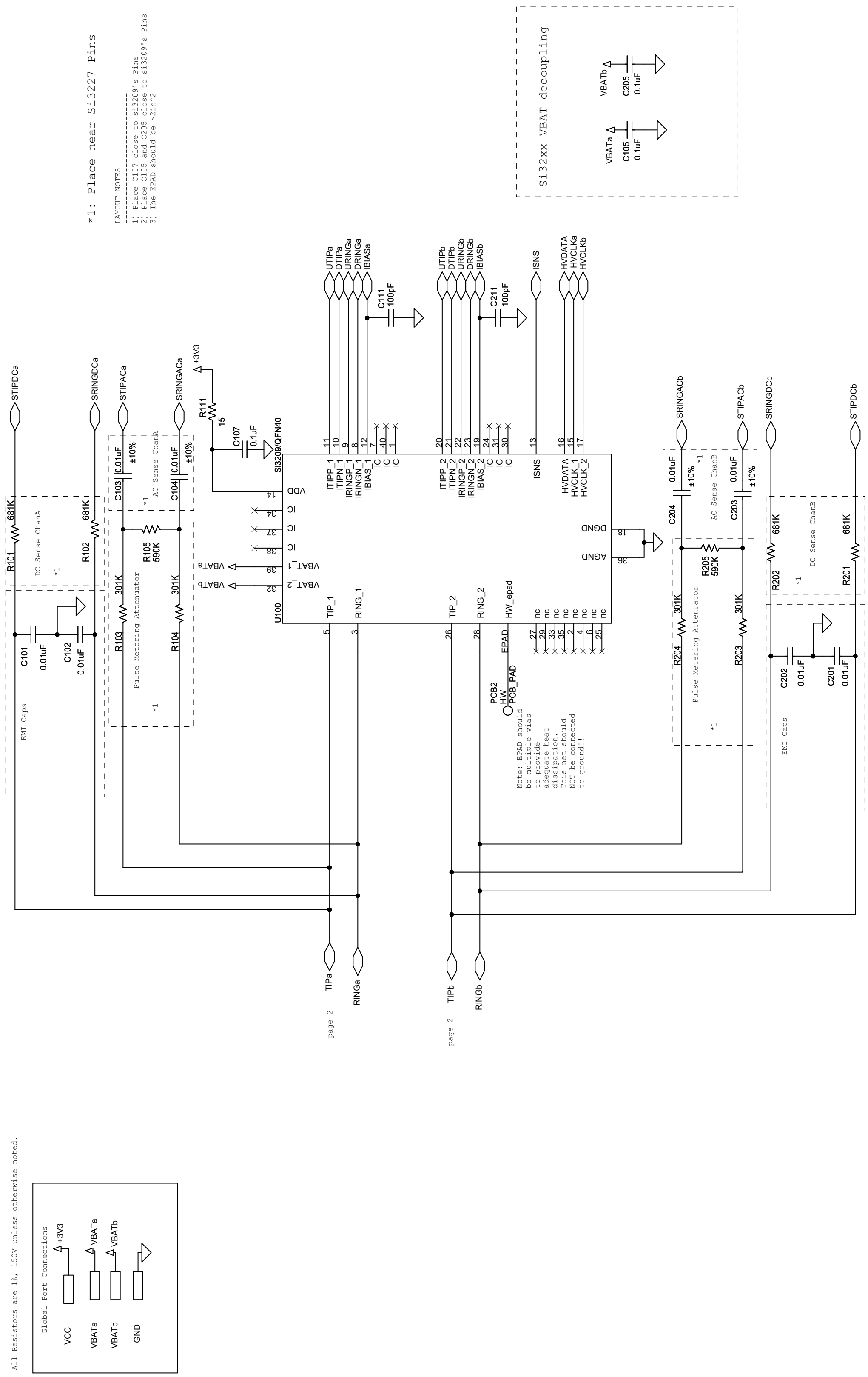


Figure 18. Linefeed (2 Lines)

3. Bill of Materials

Table 12. Si3226/7 Bill of Materials

Qty	Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part #	Mfr
1	C3	10uF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
2	C109 C110	5.6pF		50V	±0.25pF	NPO	C0402	C0402HQN500-5R6C	Venkel
2	C120 C220	10uF		25V	±20%	X7R	C1210	C1210X7R250-106M	Venkel
2	C128 C228	470pF		50V	±20%	X7R	C0402	C0402X7R500-471M	Venkel
4	D150 D151 D250 D251	P1101SC		-95V		Thyristors	DO-214AA	P1101SCL	Littelfuse
2	D152 D252	P1101CA2		-95V		Thyristors	DO-214AA-3	P1101CA2L	Littelfuse
2	D153 D253	ES1D	1.0A	200V		Single	DO-214AC	ES1D	Diodes Inc.
2	D154 D254	140V	500mW	140V		Zener	DO-35	1N5275B	Micro Commercial Co
2	D155 D255	BAV23A	400mA	200V		DUAL	SOT23-KKA	BAV23A	Diodes Inc.
2	Q120B Q220B	FQD7N20L	5.5A	200V		Nchan	DPAK-G2SD	FQD7N20L	Fairchild
4	RF150 RF151 RF250 RF251	1250T	1.25A	600V		TelCom	FUSE-F1250T	F1250T	Littelfuse
3	R4 R5 R6	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
5	R15 R16 R20 R21 R22	10K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-103J	Venkel
2	R136 R236	0	2A			ThickFilm	R1206	CR1206-4W-000	Venkel
2	R137 R237	15	1/4W		±5%	ThickFilm	R1206	CR1206-4W-150J	Venkel
3	TP14 TP20 TP21	WHITE				Loop	TESTPOINT	151-201-RC	Kobiconn
4	TP15 TP16 TP18 TP19	BLACK				Loop	TESTPOINT	151-203-RC	Kobiconn
2	U152 U252	LCP1521S		-150V		SLIC	SO8N6.0P1.27	LCP1521S	ST
2	C1 C6	10uF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
8	C2 C4 C5 C7 C60 C100 C107 C200	0.1uF		10V	±10%	X7R	C0402	C0402X7R100-104K	Venkel
1	C8	4.7nF		16V	±10%	X7R	C0402	C0402X7R160-472K	Venkel
10	C101 C102 C103 C104 C108 C201 C202 C203 C204 C208	0.01uF		200V	±10%	X7R	C0805	C0805X7R201-103K	Venkel
6	C105 C122 C132 C205 C222 C232	0.1uF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel

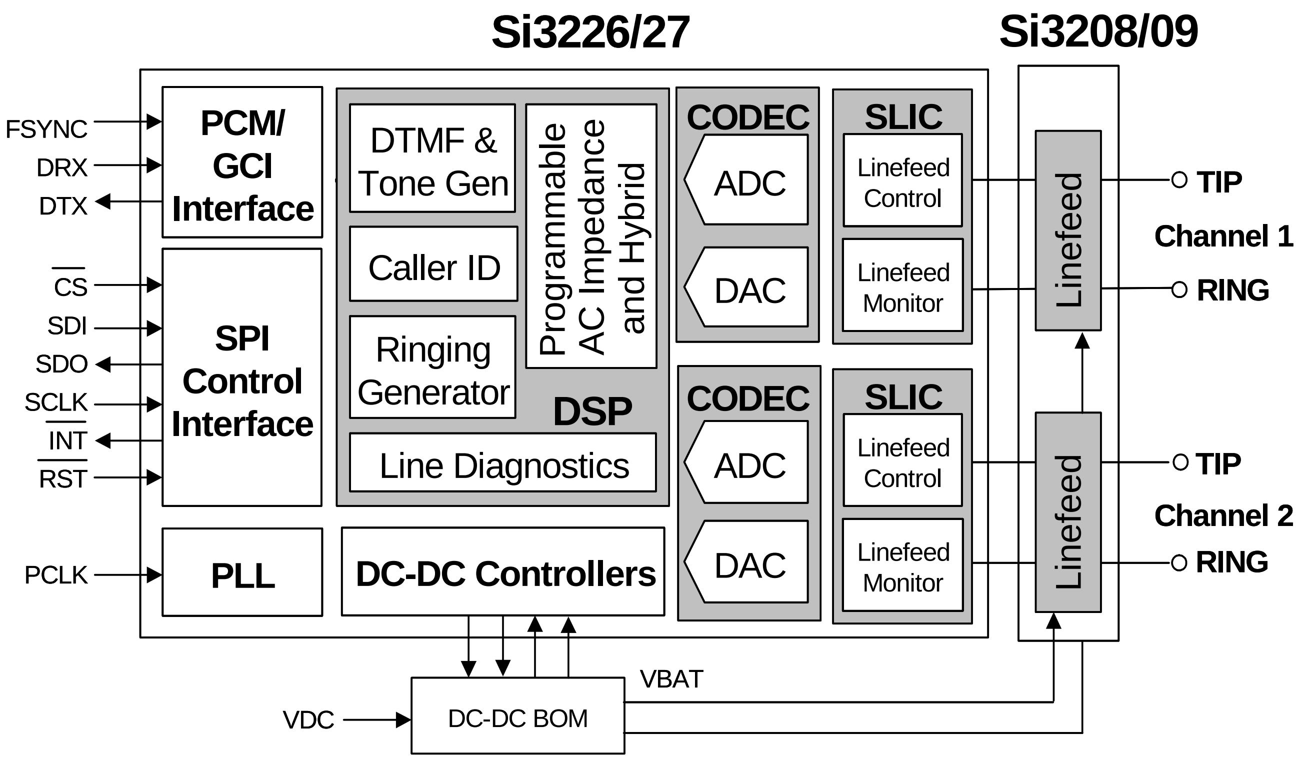
Table 12. Si3226/7 Bill of Materials

Qty	Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part #	Mfr
2	C111 C211	100pF		6V	±10%	X7R	C0402	C0402X7R6R0-101K	Venkel
4	C121 C126 C221 C226	0.1uF		25V	±10%	X7R	C0603	C0603X7R250-104K	Venkel
8	C123 C124 C125 C150 C223 C224 C225 C250	0.22uF		250V	±20%	X7R	C1812	C1812X7R251-224M	Venkel
2	C127 C227	470pF		50V	±20%	X7R	C0402	C0402X7R500-471M	Venkel
1	C130	220uF	555mA	25V	±20%	Alum_Elec	C3.5X8MM-RAD	EEUFC1E221	Panasonic
2	C131 C231	10uF		200V	±20%	Alum_Elec	C5X10MM-RAD	UVZ2D100MPD	Nichicon
2	C133 C233	68pF		200V	±5%	COG	C0805	C0805C0G201-680J	Venkel
2	D120 D220	ES1F	1.0A	300V		Single	DO-214AC	ES1F	Fairchild
4	JS1 JS4 JS5 JS6	CONN SOCKET 5x2				Socket	CONN2X5-SSQ	SSQ-105-24-F-D	Samtec
1	JS2	CONN SOCKET 2x2/SM				Socket	CONN-2X2-SSM	SSM-102-L-DV	Samtec
1	JS3	HEADER 2x2/SM				Header	CONN-2X2-TSM	TSM-102-02-T-DV	Samtec
2	J1 J2	RJ-11				RJ-11	RJ11-6-SMT	5555077-2	AMP
11	J5 J123 J124 J125 J150 J151 J223 J224 J225 J250 J251	JUMPER				Header	CONN-1X2	TSW-102-07-T-S	Samtec
2	Q120 Q220	FQT7N10	1.7A	100V		Nchan	SOT223-GDS	FQT7N10	Fairchild
2	Q121 Q221	MMBT3906-7-F	200mA	40V		PNP	SOT23-BEC	MMBT3906-7-F	Diodes Inc.
2	Q122 Q222	BSS138	200mA	50V		Nchan	SOT23-GSD	BSS138	Zetex
2	Q123 Q223	MMBT3904	200mA	40V		NPN	SOT23-BEC	MMBT3904	Fairchild
4	RT150 RT151 RT250 RT251	PTC	3A	250V		TelCom	PTC-MF-SM013	MF-SM013/250-2	Bourns
1	R2	49.9K	1/16W		±0.5%	ThickFilm	R0603	CR0603-16W-4992D	Venkel
6	R3 R7 R8 R64 R124 R224	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
3	R11 R121 R221	0.1	1/2W		±1%	ThickFilm	R1210	LCR1210-R100F	Venkel

Table 12. Si3226/7 Bill of Materials

Qty	Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part #	Mfr
5	R13 R19 R60 R61 R62	10K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-103J	Venkel
1	R17	137K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1373F	Venkel
2	R100 R200	825K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-8253F	Venkel
6	R101 R102 R125 R201 R202 R225	681K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-6813F	Venkel
4	R103 R104 R203 R204	301K	1/16W		±1%	ThickFilm	R0603	CR0603-16W-3013F	Venkel
2	R105 R205	590K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-5903F	Venkel
4	R106 R107 R206 R207	1.47M	1/8W		±1%	ThickFilm	R1206	CR1206-8W-1474F	Venkel
4	R108 R109 R208 R209	110K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1103F	Venkel
2	R110 R210	0	2A			ThickFilm	R0805	CR0805-10W-000	Venkel
5	R111 R150 R151 R250 R251	15	1/10W		±1%	ThickFilm	R0805	CR0805-10W-15R0F	Venkel
2	R122 R222	5.11	1/10W		±1%	ThickFilm	R0805	CR0805-10W-5R11F	Venkel
2	R123 R223	220	1/16W		±5%	ThickFilm	R0402	CR0402-16W-221J	Venkel
2	R126 R226	68K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-6802F	Venkel
2	R130 R230	150	1/4W		±1%	ThickFilm	R1206	CR1206-4W-1500F	Venkel
2	R132 R232	0.05	1/2W		±1%	ThickFilm	R1210	LCR1210-R050F	Venkel
4	R138 R156 R238 R256	0	2A			ThickFilm	R1206	CR1206-4W-000	Venkel
6	TP1 TP2 TP3 TP4 TP9 TP10	WHITE				Loop	TESTPOINT	151-201-RC	Kobiconn
1	TP17	BLACK				Loop	TESTPOINT	151-203-RC	Kobiconn
2	T120 T220	8uH	5A, 25W				XFMR-UTB01701s	UTB01701s	UMEC
1	U1	Si3227		3.3V		SLIC	QFP64N12X12P0.5	Si3227-D-FQ	SiLabs
1	U60	AT25010A		5V		Serial	SO8N6.0P1.27	AT25010A	ATMEL
1	U100	Si3209/ QFN40		–135V		SLIC	QFN40N6X6P0.5	Si3209-B-FM	SiLabs
2	U151 U251	TISP61089BDR		–150V		SLIC	SO8N6.0P1.27	TISP61089BDR	Bourns

4. Functional Description



The Dual ProSLIC® chipset includes the Si3226/27 low-voltage IC and the Si3208/09 high-voltage linefeed IC. The Dual ProSLIC provides all SLIC, codec, DTMF detection, and signal generation functions needed for two complete analog telephone interfaces. The Dual ProSLIC performs all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions; it also supports extensive metallic loop testing capabilities.

The Si3226 provides a standard voice-band (200 Hz–3.4 kHz) audio codec. The Si3227 provides an audio codec with both wideband (50 Hz–7 kHz) and standard voice-band (200 Hz–3.4 kHz) modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio. The Si3226/27 provides two independent, programmable, dc-dc converter controllers, each of which reacts to line conditions to provide the optimal battery voltage required for each line-state.

The linefeed ICs (Si3208/09) provide programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission. Loop current and voltage are continuously monitored using an A/D converter in the Si3226/27. The Si3208 supports battery voltages up to 110 V, sufficient for most ringing signals. The Si3209 supports battery voltages up to 135 V for higher-voltage ringing applications.

The Dual ProSLIC supports balanced 5 REN ringing with or without a programmable dc offset. The available offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements. Digital voice data transfer occurs over a standard PCM bus. Control data is transferred using a standard SPI.

The Si3226/27 is available in a 64-pin TQFP; the Si3208/09 are available in a 40-pin QFN.

4.1. DC Feed Characteristics

Dual ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics. Linefeed characteristics for each channel are independently configurable.

When in the active state, each ProSLIC channel operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 19. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

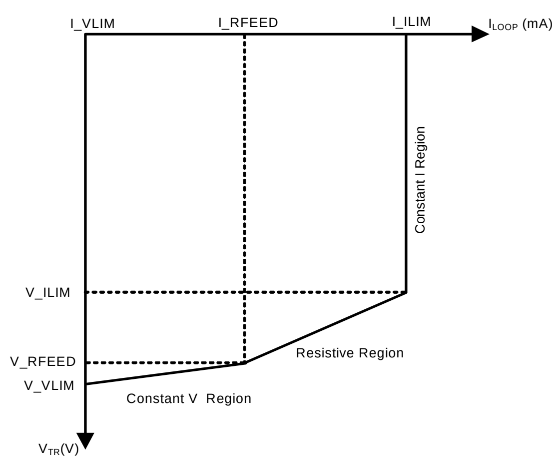


Figure 19. Dual ProSLIC DC Feed Characteristics

4.2. Linefeed Operating States

The linefeed interface includes eight different register-programmable operating states as listed in Table 13. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

4.3. Line Voltage and Current Monitoring

The Dual ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual register addresses. Additionally, the loop voltage (V_{TIP}–V_{RING}), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

4.4. Power Monitoring and Power Fault Detection

The Dual ProSLIC's line monitoring functions are used to continuously protect the linefeed IC (LFIC) against excessive power conditions. The LFIC contains an on-chip, analog sensing diode that provides real-time temperature data to the Si3226/27 and turns off the LFIC when a preset threshold is exceeded. The LFIC status is reflected in a Si3226/27 register bit.

If the Si3226/27 detects a fault condition or overpower condition on any channel, it automatically sets that channel to the open state and generates a "power alarm" interrupt. The interrupt can be masked, but the automatic transition to open is not recommended to be masked. The various power alarms and linefeed faults supporting automatic intervention are described below.

1. LFIC total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. LFIC thermal shutdown event; this event is automatically performed, and no intervention by the
4. Si3226/27 is required.

4.5. Thermal Overload Shutdown

If the LFIC die temperature exceeds the programmed junction temperature threshold, the LFIC will go to an open state without any assistance from the Si3226/27.

Table 13. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and all line supervision functions are powered down. Audio is powered down. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high-Z state during line-feed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel selected is put into diagnostic mode. In this mode, the selected channel has special diagnostic resources available.

4.6. Power Dissipation Considerations

The Dual ProSLIC is designed to source loops up to 20 kft as well as short loop applications. The LFIC provides all battery sourcing functions and is, therefore, the determining factor regarding power dissipation in a specific application. The Dual ProSLIC provides an on-chip dc-dc controller that can dynamically reduce the battery supply to ideally match the required line feed voltage.

4.7. Loop Closure Detection

The Dual ProSLIC provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.8. Ground Key Detection

The Dual ProSLIC provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.9. Ringing Generation

The Dual ProSLIC provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Using a balanced ringing scheme, the ringing signal is applied to both the TIP and RING leads using dual ringing waveforms that are 180° out of phase with each other. The resulting ringing signal seen across TIP-RING is twice the amplitude of the ringing waveform on either the TIP or RING lead, which allows the ringing circuitry to be forced to withstand only half the total ringing amplitude seen across TIP-RING.

4.10. Polarity Reversal

The Dual ProSLIC supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

4.11. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Dual ProSLIC to the impedance of the subscriber loop and minimize the receive path signal reflected back onto the transmit path. Most real or complex two-wire impedances can be generated by using the coefficient generator software to simulate the desired line conditions and generate the required register coefficients.

4.12. Transhybrid Balance Filter

The transhybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path. The coefficient generator software is used to optimize the filter coefficients.

4.13. Tone Generators

The Dual ProSLIC includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

4.14. DTMF Detection

In DTMF, two tones generate a DTMF digit. One tone is chosen from the four possible row tones, and one tone is chosen from the four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits. The Dual ProSLIC performs DTMF detection using an algorithm to compute the DFT for each of the eight DTMF frequencies and their second harmonics. At the end of the DFT computation, the squared magnitudes of the DFT results for the 8 DTMF fundamental tones are computed. The row and column results are sorted to determine the strongest tones, and checks are made to determine if the strongest row and column tones constitute a DTMF digit.

4.15. DC-DC Controller

The controller operates a dc-dc converter circuit that converts a single positive dc input voltage into an independent negative battery voltage for each channel. In addition to eliminating external high-voltage power supplies, the dc-dc controller allows the Dual ProSLIC to dynamically control the battery voltage to the minimum required for any given operating state according to the programmed linefeed parameters.

4.16. Wideband Audio

The Si3226 supports a narrowband (200 Hz–3.4 kHz) audio codec. The Si3227 supports a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The Si3227 wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. In wideband operation, two time slots are used to transmit the wideband signal and each slot contains 8-bits of the 16-bit sample. These two time slots are transmitted and received half a frame apart, but within the same 8 kHz frame.

4.17. SPI Control Interface

The controller interface to the Dual ProSLIC is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CS), serial data input (SDI), and serial data output (SDO). In addition, the Dual ProSLIC devices feature a serial data through output (SDITHRU) to support operation of up to 16 devices (up to 32 channels) using a single chip select line. The device operates with both 8-bit and 16-bit SPI controllers.

4.18. PCM Interface and Companding

The Dual ProSLIC contains a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from 8 to 128 8-bit time slots in each 125 µs frame, corresponding to a PCM clock (PCLK) frequency range of 512 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Dual ProSLIC supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

4.19. General Circuit Interface

The Dual ProSLIC supports an alternative communication interface to the SPI and PCM control and data interface. The General Circuit Interface (GCI) is used for transmission and reception of both control and data information onto a GCI bus. The PCM and GCI interfaces are both 4-wire interfaces and share the same pins. In GCI mode, the four-wire SPI control interface is used as hard-wired channel selector pins. The selection between PCM and GCI modes is performed when coming out of reset using the SDITHRU pin.

4.20. Metallic Loop Testing

The Dual ProSLIC includes the ability to detect multiple fault conditions within the line card as well as on the T/R pair.

1. Hazardous Potential Test—This test checks for ac voltage >50 V_{rms} or dc voltage >135 V on T-G or R-G. If a hazardous voltage is encountered, test access MUST release within two seconds of the time when it was initiated using a preset threshold.
2. Foreign ElectroMotive Force Test—Checks T-G or R-G for ac voltage >10 V_{rms}, dc voltage >6 V. Uses same threshold as for hazardous voltage test.
3. Resistive Faults Test—Checks for dc resistance from T-R, T-G or R-G. Any measurement <150 kΩ is considered a resistive fault.
4. Receiver-Off-Hook Test—Distinguishes between a T-R resistive fault and an off-hook condition.
5. Ringers Test—Checks for the presence of REN across T-R. Result are >0.175REN and <5REN for a valid load.
6. Ringing Voltage Verification—Uses current voltage sensing capability.
7. Test-In Diagnostics—The Dual ProSLIC can switch in a preset load impedance to test the SLIC/codec functionality using a known set of conditions.

5. Pin Descriptions: Si3226/27

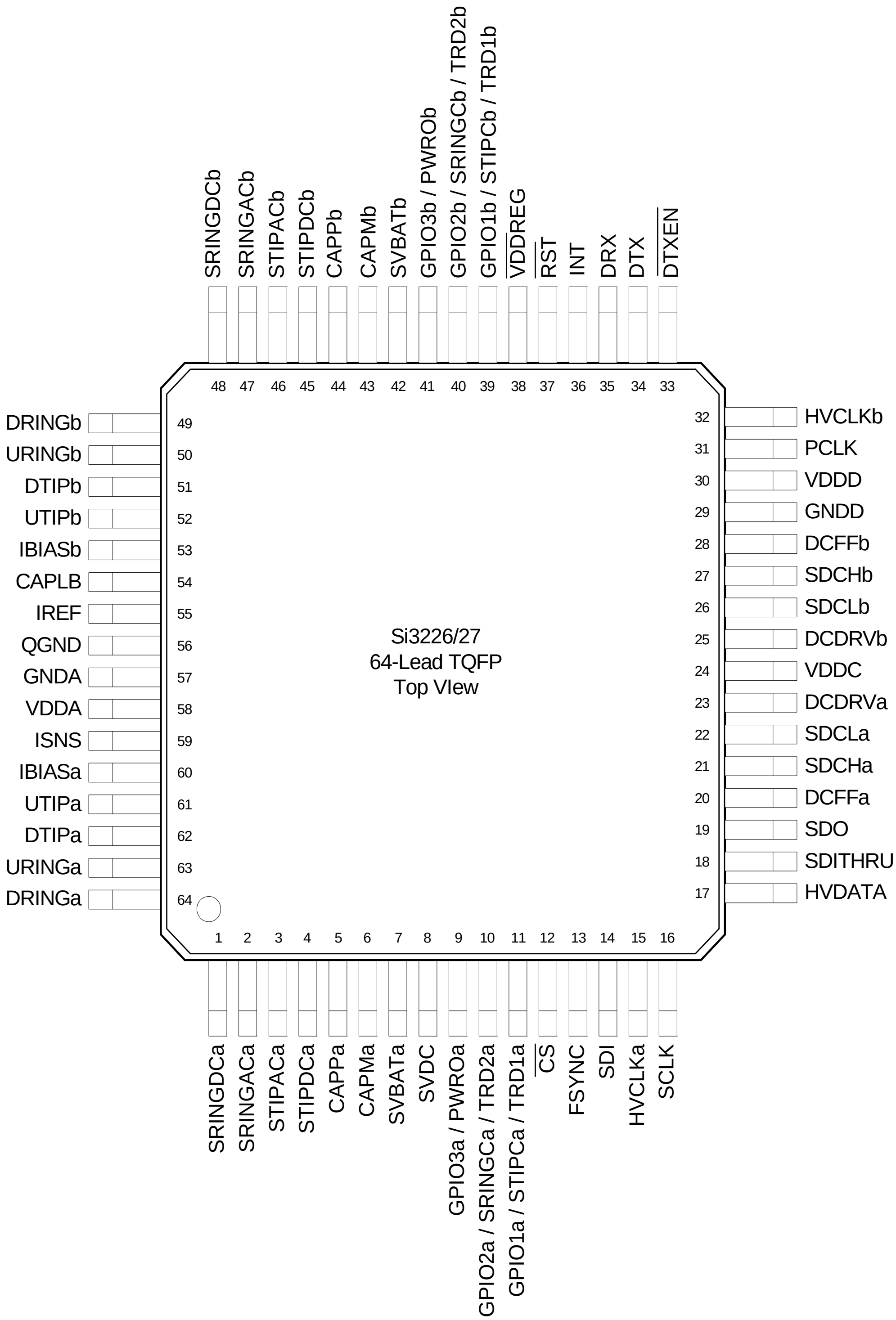


Table 14. Si3226/27 Pin Descriptions

Pin #	Symbol		Description
1	SRINGDCa		RING DC Sense Input.
2	SRINGACa		RING AC Sense Input.
3	STIPACa		TIP AC Sense Input.
4	STIPDCa		TIP DC Sense Input.
5	CAPPa		Metallic Loop Filter Capacitor-Positive Terminal.
6	CAPMa		Metallic Loop Filter Capacitor-Negative Terminal.
7	SVBATa		Battery Sensing Input.
8	SVDC		DC-DC Input Power Rail Sensor.
9	GPIO3a / PWROa		General Purpose I/O / Power Offloading Output.
10	GPIO2a / SRINGCa / TRD2a		5 V tolerant I/O General Purpose I/O / RING Coarse Sense Input / Test Relay Driver.
11	GPIO1a / STIPCa / TRD1a		5 V tolerant I/O General Purpose I/O / TIP Coarse Sense Input / Test Relay Driver.
12	$\overline{CS}$		Chip Select Input.
13	FSYNC		Frame Sync Clock Input.
14	SDI		Serial Port Data Input.
15	HVCLKa		Line-Driver IC Clock Output.
16	SCLK		Serial Port Bit Clock Input.
17	HVDATA		Line-Driver IC Data Output
18	SDITHRU		Serial Data Daisy Chain Output.
19	SDO		Serial Port Data Output.
20	DCFFa		DC Flexible Function I/O A.
21	SDCHa		DC-DC Current Monitor Input-High Terminal.
22	SDCLa		DC-DC Current Monitor Input-Low Terminal.
23	DCDRVa		DC-DC Drive Output.
24	VDDC		DC-DC Switch Driver Power Supply.
25	DCDRVb		DC-DC Drive Output.
26	SDCLb		DC-DC Current Monitor Input-Low Terminal.
27	SDCHb		DC-DC Current Monitor Input-High Terminal.
28	DCFFb		DC Flexible Function I/O B
29	GNDD		Digital Ground.
30	VDDD		Digital Supply Voltage.
31	PCLK		PCM Bus Clock Input.
32	HVCLKb		Line-Driver IC Clock Output.

Table 14. Si3226/27 Pin Descriptions (Continued)

Pin #	Symbol		Description
33	$\overline{\text{DTXEN}}$		Transmit PCM Enable Output.
34	DTX		Transmit PCM Data Output.
35	DRX		Receive PCM Data Input.
36	$\overline{\text{INT}}$		Interrupt Output.
37	$\overline{\text{RST}}$		Reset Input.
38	VDDREG		Regulated Core Power Supply.
39	GPIO1b / STIPCb / TRD1b		5 V tolerant I/O General Purpose I/O / TIP Coarse Sense Input / Test Relay Driver.
40	GPIO2b / SRINGCb / TRD2b		5 V tolerant I/O General Purpose I/O / RING Coarse Sense Input / Test Relay Driver.
41	GPIO3b / PWROb		General Purpose I/O / Power Offloading Output.
42	SVBATb		Battery Sensing Input.
43	CAPMb		Differential Loop Filter Capacitor-Negative Term.
44	CAPPb		Differential Loop Filter Capacitor-Positive Term.
45	STIPDCb		TIP DC Sense Input.
46	STIPACb		TIP AC Sense Input.
47	SRINGACb		RING AC Sense Input.
48	SRINGDCb		RING DC Sense Input.
49	DRINGb		RING Pull-Down Current Driver Output.
50	URINGb		RING Pull-Up Current Driver Output.
51	DTIPb		TIP Pull-Down Current Driver Output.
52	UTIPb		TIP Pull-Up Current Driver Output.
53	IBIASb		Line Driver IC Bias Current Output.
54	CAPLB		Longitudinal Balance Calibration Capacitor.
55	IREF		Current Reference Input.
56	QGND		Quiet Ground Reference Input.
57	GNDA		Analog Ground.
58	VDDA		Analog Supply Voltage.
59	ISNS		Line Current Sense Input.
60	IBIASa		Line Driver IC Bias Current Output.
61	UTIPa		TIP Pull-Up Current Driver Output.
62	DTIPa		TIP Pull-Down Current Driver Output.
63	URINGa		RING Pull-Up Current Driver Output.
64	DRINGa		RING Pull-Down Current Driver Output.

6. Pin Descriptions: Si3226/27 + Si3208/09

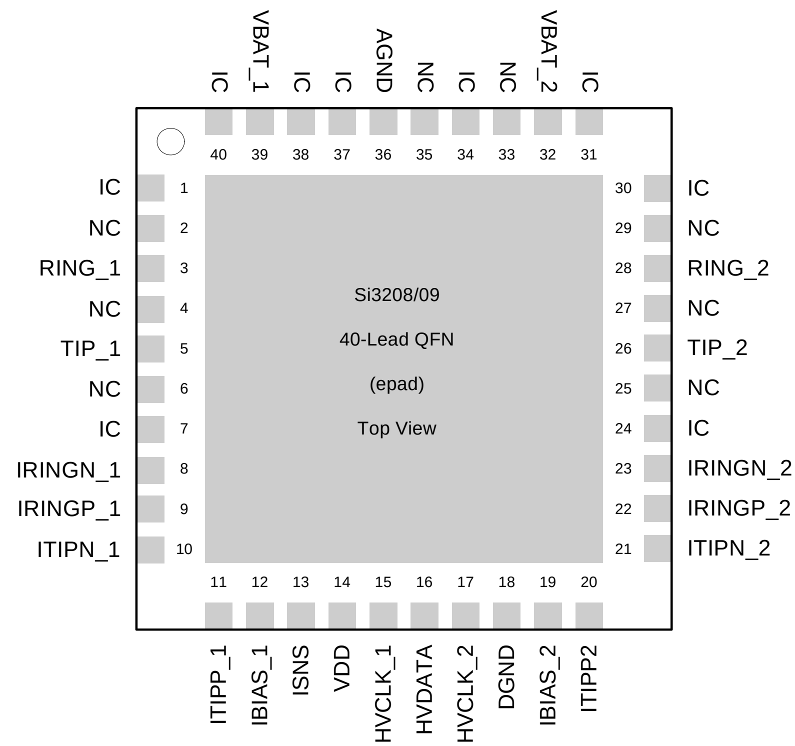


Table 15. Si3208/09 Pin Descriptions

QFN Pin #	Symbol	Description
1	IC	Internal connection; leave unbiased.
2	NC	No Connect. Leave unbiased.
3	RING_1	Ring Channel 1 Input/Output.
4	NC	No Connect. Leave unbiased.
5	TIP_1	Tip Channel 1 Input/Output.
6	NC	No Connect. Leave unbiased.
7	IC	Internal connection; leave unbiased.
8	IRINGN_1	Negative Ring Current Control Channel 1 Input.
9	IRINGP_1	Positive Ring Current Control Channel 1 Input.
10	ITIPN_1	Negative Tip Current Control Channel 1 Input.
11	ITIPP_1	Positive Tip Current Control Channel 1 Input.
12	IBIAS_1	Current Bias Channel 1 Input.
13	ISNS	Current Sense Output.

Table 15. Si3208/09 Pin Descriptions (Continued)

QFN Pin #	Symbol	Description
14	VDD	IC Supply Voltage Input.
15	HVCLK_1	High-Voltage IC Clock Channel 1 Input.
16	HVDATA	High-Voltage IC Data Input/Output.
17	HVCLK_2	High-Voltage IC Clock Channel 2 Input.
18	DGND	Digital Ground.
19	IBIAS_2	Current Bias Channel 2 Input.
20	ITIPP_2	Positive Tip Current Control Channel 1 Input.
21	ITIPN_2	Negative Tip Current Control Channel 2 Input.
22	IRINGP_2	Positive Ring Current Control Channel 2 Input.
23	IRINGN_2	Negative Ring Current Control Channel 2 Input.
24	IC	Internal connection; leave unbiased.
25	NC	No Connect. Leave unbiased.
26	TIP_2	Tip Channel 2 Input/Output.
27	NC	No Connect. Leave unbiased.
28	RING_2	Ring Channel 2 Input/Output.
29	NC	No Connect. Leave unbiased.
30	IC	Internal connection; leave unbiased.
31	IC	Internal connection; leave unbiased.
32	VBAT_2	Operating Battery Voltage Channel 2 Input.
33	NC	No Connect. Leave unbiased.
34	IC	Internal connection; leave unbiased.
35	NC	No Connect. Leave unbiased.
36	AGND	Analog Ground.
37	IC	Internal connection; leave unbiased.
38	IC	Internal connection; leave unbiased.
39	VBAT_1	Operating Battery Voltage Channel 1 Input.
40	IC	Internal connection; leave unbiased.
epad		Exposed Die Attach Paddle. For adequate thermal management, the exposed die paddle should be soldered to a printed circuit board pad that is connected to an electrically-isolated low-impedance inner layer and/or backside thermal plane(s) using multiple thermal vias. Do not connect this pad to ground.

7. Ordering Guide

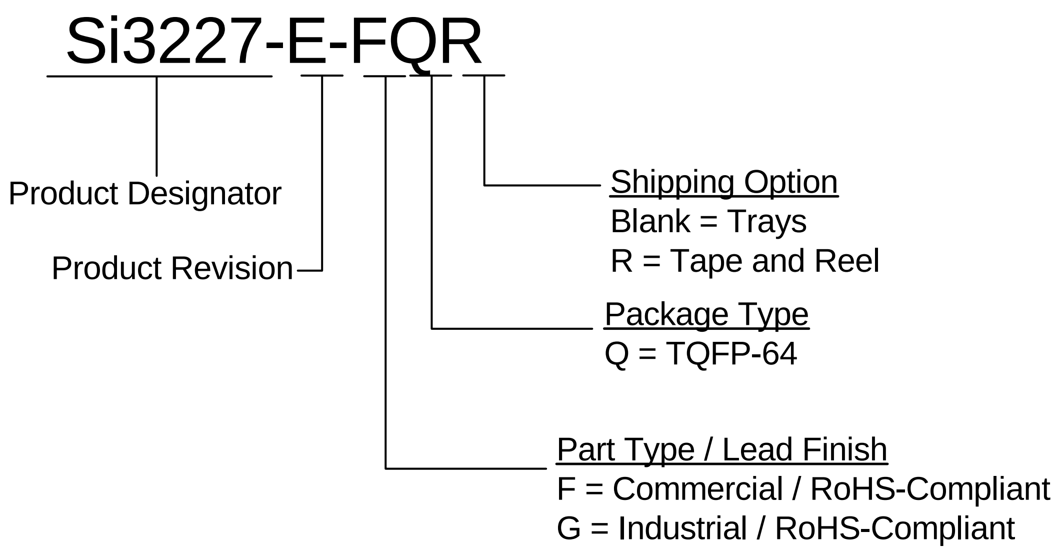
Part Number[1]	Description	Package[2]	Temperature Range
Si3226-E-FQ	Dual ProSLIC	TQFP-64	0 to 70° C
Si3226-E-GQ	Dual ProSLIC	TQFP-64	–40 to 85° C
Si3227-E-FQ	Dual ProSLIC, wideband	TQFP-64	0 to 70° C
Si3227-E-GQ	Dual ProSLIC, wideband	TQFP-64	–40 to 85° C
Si3208-B-FM	–110 V line-feed IC	QFN-40	0 to 70° C
Si3208-B-GM	–110 V line-feed IC	QFN-40	–40 to 85° C
Si3209-B-FM	–135 V line-feed IC	QFN-40	0 to 70° C
Si3209-B-GM	–135 V line-feed IC	QFN-40	–40 to 85° C

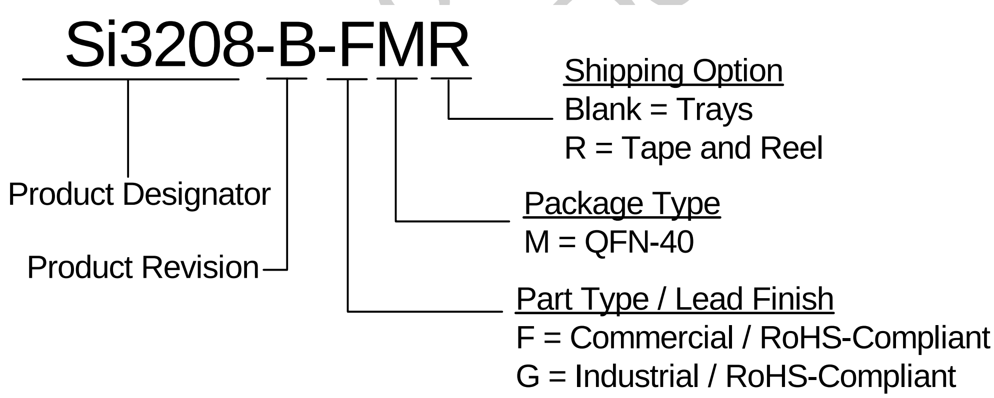
Notes:
1. Adding the suffix "R" to the end of the part number (e.g., Si3226-E-FQR) denotes tape-and-reel packaging.
2. All packages are RoHS-compliant.

8. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:





9. Package Outline: 64-Pin TQFP

Figure 20 illustrates the package details for the Si3226/27. Table 16 lists the values for the dimensions shown in the illustration.

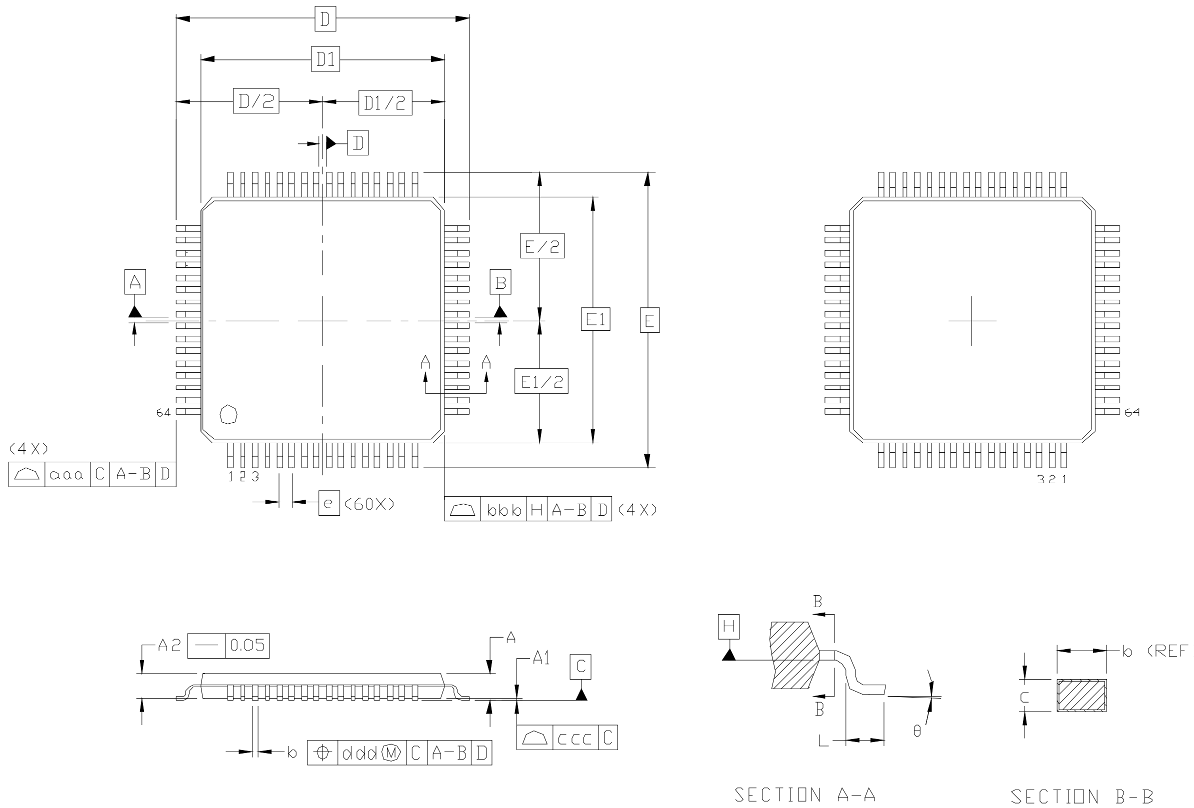


Figure 20. 64-pin Thin Quad Flat Package (TQFP)

Table 16. 64-pin TQFP Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC.		

Dimension	Min	Nom	Max
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08
Θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

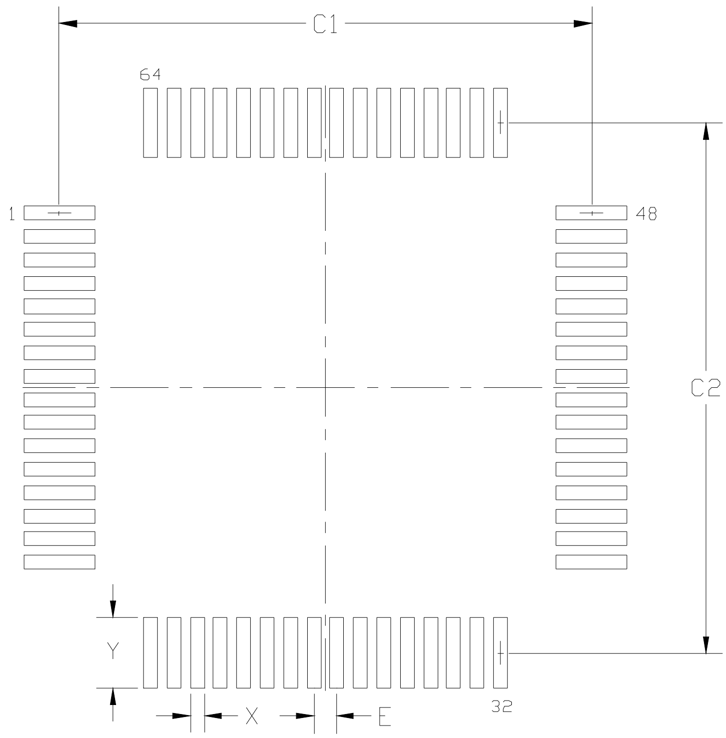


Figure 21. 64-pin TQFP Land Pattern

Table 17. 64-pin TQFP Land Pattern Dimensions

Dimension	MIN	MAX
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Package Outline: 40-Pin QFN

Figure 22 illustrates the package details for the Si3208/09. Table 18 lists the values for the dimensions shown in the illustration.

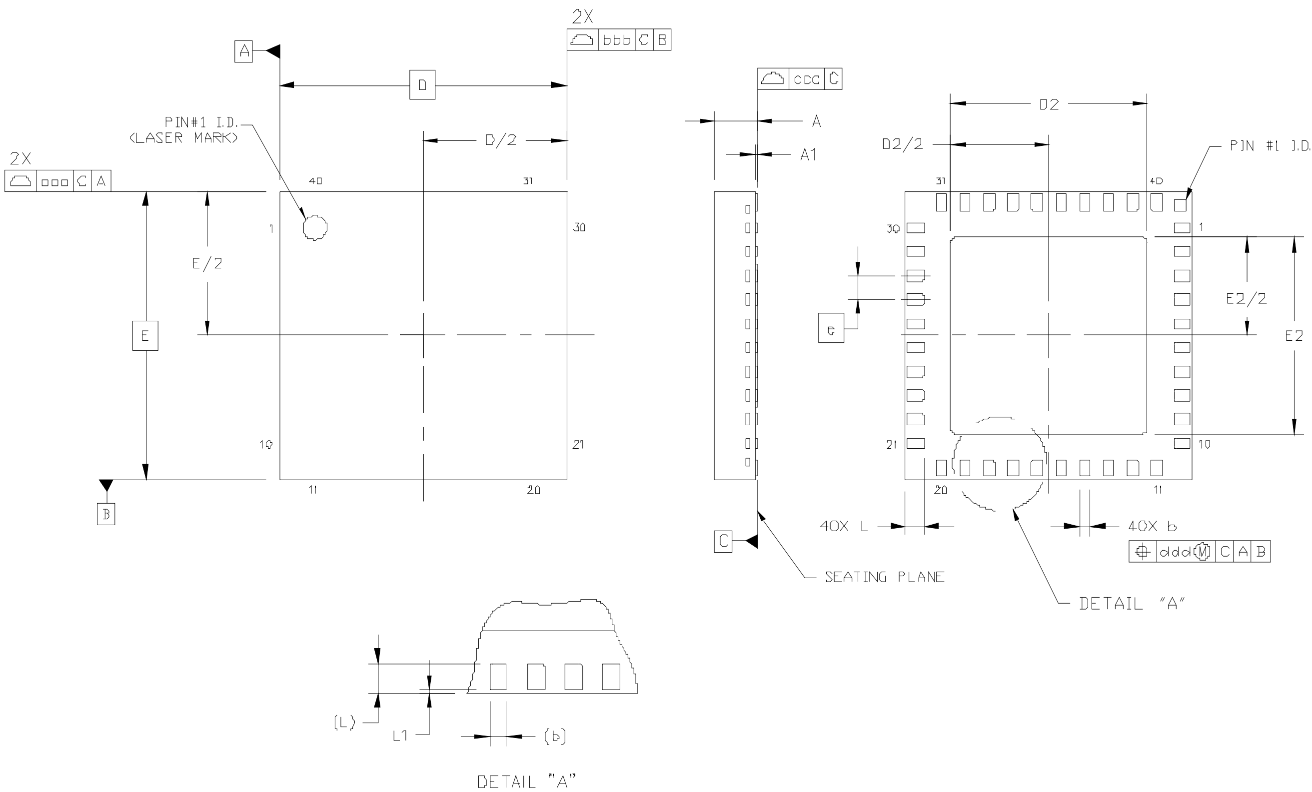


Figure 22. 40-pin QFN Package

Table 18. 40-pin QFN Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	0.80	0.85	0.90	E2	4.00	4.10	4.20
A1	0.00	0.02	0.05	L	0.30	0.40	0.50
b	0.18	0.25	0.30	L1	0.03	0.05	0.08
D	6.00 BSC.			aaa	—	—	0.10
D2	4.00	4.10	4.20	bbb	—	—	0.10
e	0.50 BSC.			ccc	—	—	0.08
E	6.00 BSC.			ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD-2.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

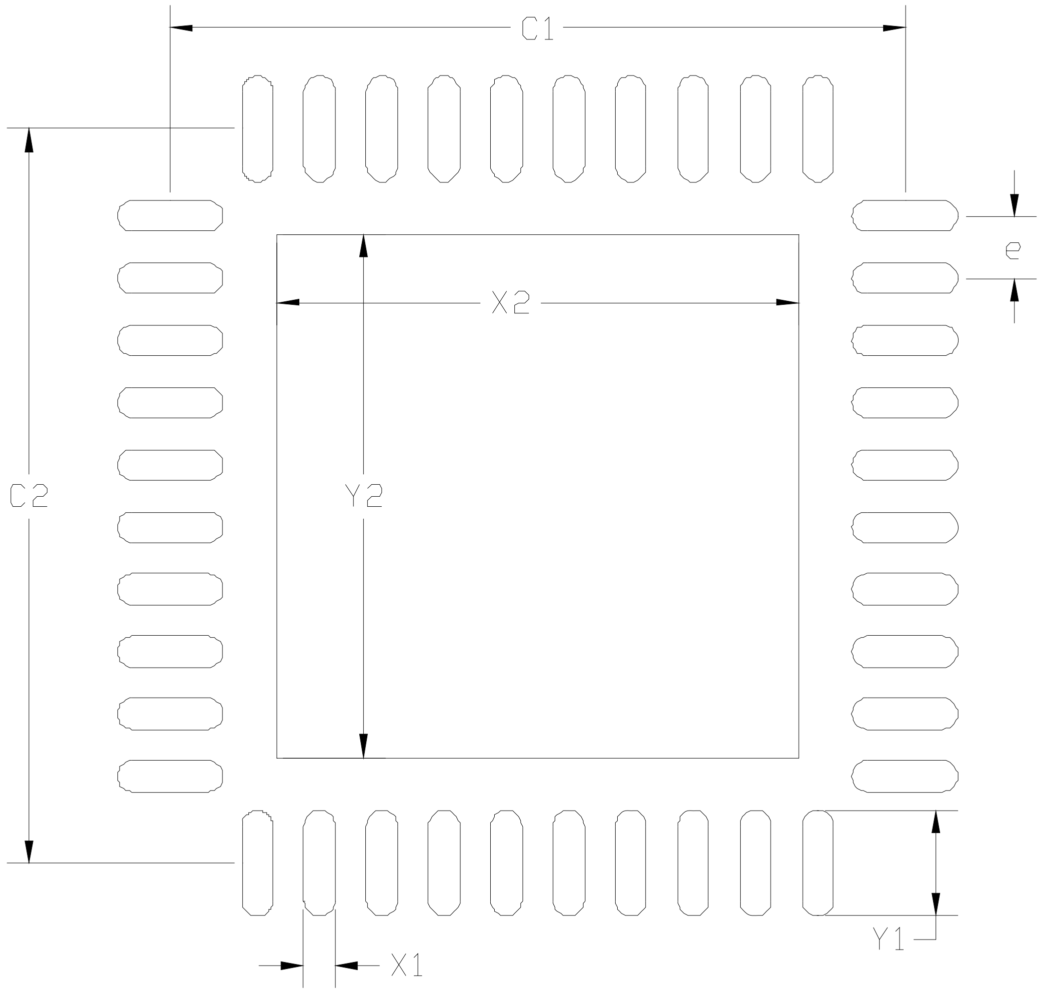


Figure 23. 40-Pin QFN Land Pattern

Table 19. 40-pin QFN Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
C1	5.80	5.90
C2	5.80	5.90
X1	0.15	0.25
X2	4.10	4.20
Y1	0.75	0.85
Y2	4.10	4.20

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4x4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Document Change List

Revision 0.2 to Revision 0.32

- Added Si3208 and Si3209.
- Removed Si3203, Si3205, and Si3206.
- Added pin-outs and package drawings for Si3208 and Si3209.
- Updated pin-out for Si3226.
- Updated bill of materials.
- Updated “2. Typical Application Circuits” and added dc-dc converter schematics.
- Updated tables.

Revision 0.32 to Revision 0.33

- Changed package type for Si3208.
- Deleted QFN-32 drawing.
- Updated dc-dc converter schematic.
- Updated bills of materials.
- Updated max V_{BAT} values.
- Updated thermal shutdown thresholds.
- Updated Si3208/09 pin descriptions.

Revision 0.33 to Revision 1.0

- Added pin-out diagrams for Si3226/27 and Si3208/09
- Updated schematic and BOM in section “3. Bill of Materials”.
- Updated former Tables 1-9. Removed former Table 7. See AN317 Section 2.2.1 for DC Feed characteristics detail.
- Added Figure 7, “RX Attenuation Distortion.”Figure 8, “TX Attenuation Distortion.”Figure 9, “Transmit Group Delay Distortion.”Figure 10, “Receive Group Delay Distortion.”.
- Updated section “4. Functional Description”.
- Updated section “5. Pin Descriptions: Si3226/27” and section “6. Pin Descriptions: Si3226/27 + Si3208/09”.
- Updated section “9. Package Outline: 64-Pin TQFP” and section “10. Package Outline: 40-Pin QFN”.
- Deleted LFIC 48-pin eTQFP and 32-pin QFN package references.
- Added REG 73 = 0x0B to Longitudinal test conditions

Revision 1.0 to Revision 1.1

- Updated Ordering Guide for revision E silicon.
- Updated Maximum Ringing Amplitude values and DC Differential Output Resistance in Table 5 Linefeed Characteristics.
- Added Powerup and Initialization Sequence diagram to section 1.
- Added Reset timing diagram to section 1.
- Added PCKLK Jitter tolerance to Table 10, “Switching Characteristics—PCM Highway Interface,” on page 14.
- Added PCKLK Jitter tolerance to Table 11, “Switching Characteristics—GCI Highway Serial Interface,” on page 15.
- Updated the number of devices that can be daisy chained in section "4.17. SPI Control Interface," on page 32.
- Added land pattern, solder mask, stencil and card assembly guidelines.
- Updated Application Circuit and Bill of Materials in sections 2 and 3.

Revision 1.1 to Revision 1.2

- Updated schematics in “2. Typical Application Circuits”
- Updated Bill of Materials in “3. Bill of Materials”.
- Updated power up sequence diagram in “1. Electrical Specifications”
- Updated section “4.16. Wideband Audio”
- Added powerdown sequence

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