Extended Line Driver for DSLAM applications

Key Features

- Using standard CMOS technologies
- Seven power modes (0.4 W - 1 W) enables optimized line card power dissipation
- Typically 0.8 W (V_{BAT}= 10 V) power dissipation during full rate CO-operation and 0.2 W when the device is operating in idle mode
- Analog echo cancellation (better than 20 dB) relaxes the requirements of the DSP and the AD/DA converter
- A high integration level requires minimum external components and a more robust design
- 32 pin LQFP package (0°C - 85°C)

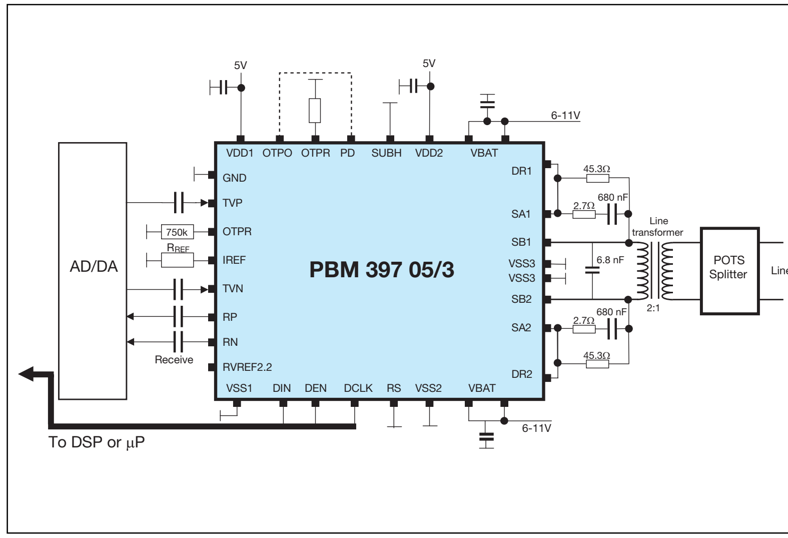

Figure 1. Line driver application.

Description

The Ericsson Analog Receive/Transmit Interface Circuit (ARTIC) for DSLAM applications is an analog line driver and receiver circuit providing the driving and terminating functions needed for implementation of an ADSL transceiver. The DSL interface circuit includes line driver, receiver, echo cancellation, termination and programmable gain controllers. The ARTIC line driver serve both full rate ADSL and ADSL Lite, according to the ITU recommendations G.dmt and G.Lite respectively, it supports annex A (ADSL over POTS) and annex B (ADSL over ISDN). The ARTIC line driver is designed for CO-applications.

Power consumption is minimized by the line driver architecture and by a design optimized for ADSL. The optimized design of the ARTIC line driver also ensures a compact board design with minimum area and wiring.

On a CO-application, a dual power supply is used to provide full line drive capability. The applied supply voltage on the driver output can be varied between 6 V and 11 V, depending on the required output swing (up to 16.5 Vpp differential).

Further, the design of the ARTIC line driver relaxes the requirements on the mixed signal and DSP part of the ADSL transceiver, with an integrated analog echo cancellation, which cancel more than 20 dB of the transmitted signal, and an intelligent programmable feedback loop providing an optimal line termination.

To further reduce power dissipation, seven power modes are introduced, which can be used on shorter lines to reduce power dissipation or when bitrate demands are lower.

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Absolute Maximum Ratings

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Comment
Storage Temperature Range		T_{Stg}	-60		+150	°C	
Operating Junction Temperature Range		T_J	0		+120	°C	
Operating Ambient Temperature Range		T_{Amb}	0		+85	°C	
Thermal Resistance, junction to ambient, LQFP-32		Θ_{JA}		42.1		°C/W	On Multilayer card @ 1m/s flow
Supply Voltages V_{DD1}, V_{DD2}, with respect to V_{SS1}	0°C< T_{Amb} <+85°C	V_{DDx}	-0.3		+6.5	V	
Supply Voltages V_{BAT}, with respect to V_{SS1}	0°C< T_{Amb} <+85°C	V_{BAT}	-0.3		+11.5	V	
Analog Voltage Input Range, with respect to V_{SS1}	0°C< T_{Amb} <+85°C	V_{Analog}	-0.3		V_{DD1}+0.3	V	
Digital Voltage Input Range, with respect to V_{SS1}	0°C< T_{Amb} <+85°C	$V_{Digital}$	-0.3		V_{DD1}+0.3	V	
Continuous Power Dissipation	T_{Amb} = +85°C	P_{Dmax}			1.2	W	

Recommended Operating Conditions

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Comment
Operating Ambient Temperature Range		T_{Amb}	0		+85	°C	See figure 2
Supply Voltage	With respect to V_{SS1}	V_{DD1}	4.75	5	5.25	V	
	With respect to V_{SS2}	V_{DD2}	4.75	5	5.25	V	
	With respect to V_{SS3}	V_{BAT}	V_{DD1} + 1	10.5	11.0	V	

Maximum Ambient Temperature

Maximum power dissipation in LQFP 32 when transmitting multitone, assumed that maximum junction temperature is 120 °C, and maximum ambient temperature is 85 °C.
Rthja = 47.9 °C/W with airflow of 0 liters/min
Rthja = 42.1 °C/W with airflow of 200 liters/min
Rthja = 39.4 °C/W with airflow of 500 liters/min

P_{dmax}

Temp.	Flow (l/min) 0	200	500
TA = 85 °C	730	830	890
TA = 80 °C	840	850	1020
TA = 75 °C	940	1070	1140
TA = 70 °C	1040	1190	1270

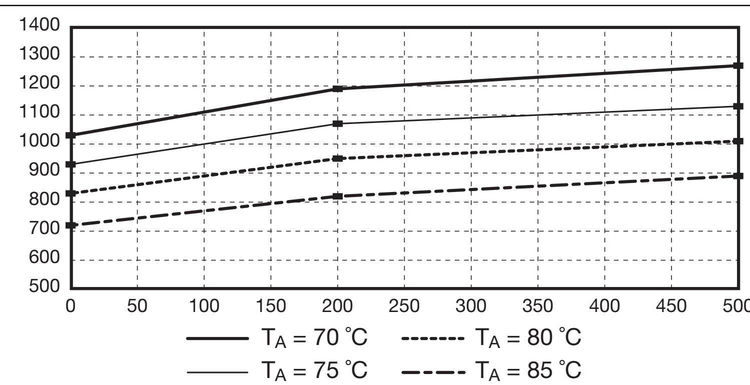


Figure 2. Ambient temperature.

Default Conditions

Unless otherwise noted the specification applies for the default general conditions using the default external components and default device programming.

General Conditions

Condition	Symbol	Value	Unit	Comment
Power Supplies except V_{BAT}	V_{DD1}, V_{DD2}	5	V	
Power Supply	V_{DD3}	10	V	
Receive bias voltage	V_{RRef}	2.2	V	
Ambient Temperature	T_{Amb}	25	°C	

External Components in application

Component	Symbol	Value	Unit	Tol.	Comment
Line Transformer	T_1*	2:1			At least 45dB balance
Line Capacitors	C_{LA}, C_{LB}	68	nF	10%	5% for better echo cancellation
Z_S series resistors	R_{SA}, R_{SB}	2.7	Ω	1%	0.25W
Z_S shunt resistors	R_{SHA}, R_{SHB}	45.3	Ω	1%	0.25W
Z_S series capacitors	C_{SA}, C_{SB}	680	nF	5%	63V, tan $\delta < 0.03$ @80kHz
Bias Current Setting Resistor	R_{REF}	24.3	kΩ	1%	0.1W
C_{OB} out of band Filter Capacitor	C_{OB}	6.8	nF	10%	
Receive Path DC Capacitor	C_{RX}	68	nF	10%	
C_{VDD} Decoupling Capacitor for V_{DD1}	C_{VDD1}	220	nF	10%	
C_{VDD} Decoupling Capacitors V_{DD2},	V_{BAT}, C_{VDD2}, C_{VBAT}	220	nF	10%	
Transmit Input Coupling Capacitor	C_{TP}, C_{TN}	22	nF	10%	
Receive Output Coupling Capacitor	C_{RP}, C_{RN}	22	nF	10%	

* For example Schott 32828 or Bel Fuse S560-6600-AB: The C_{LA} and C_{LB} values are given for an application where this Schott transformer is used.

External components in application

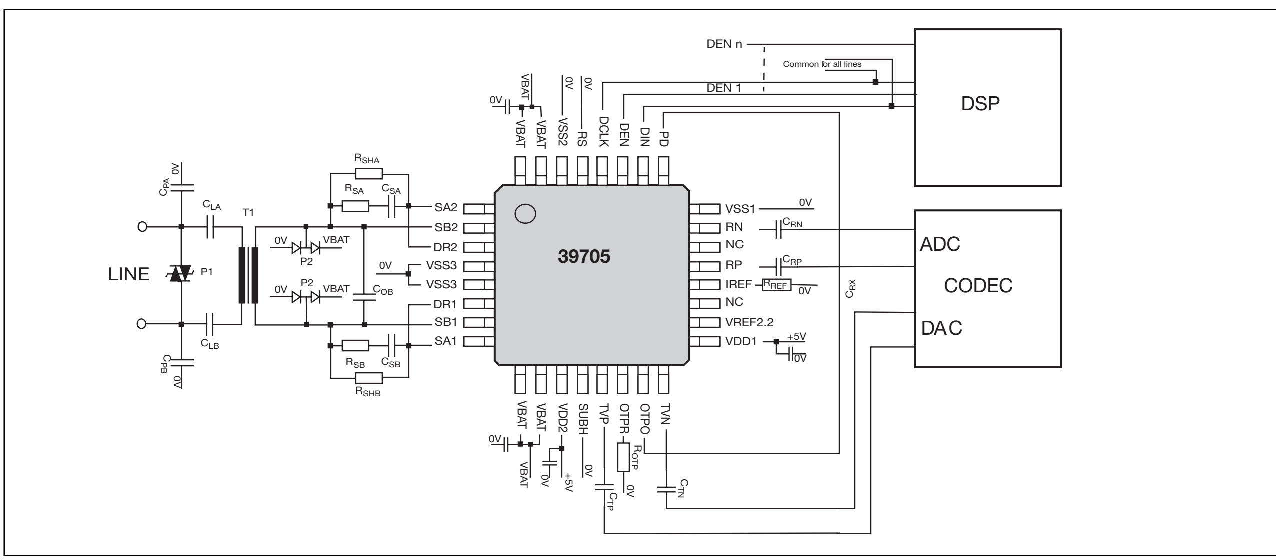


Figure 3. External components in application.

External components during test

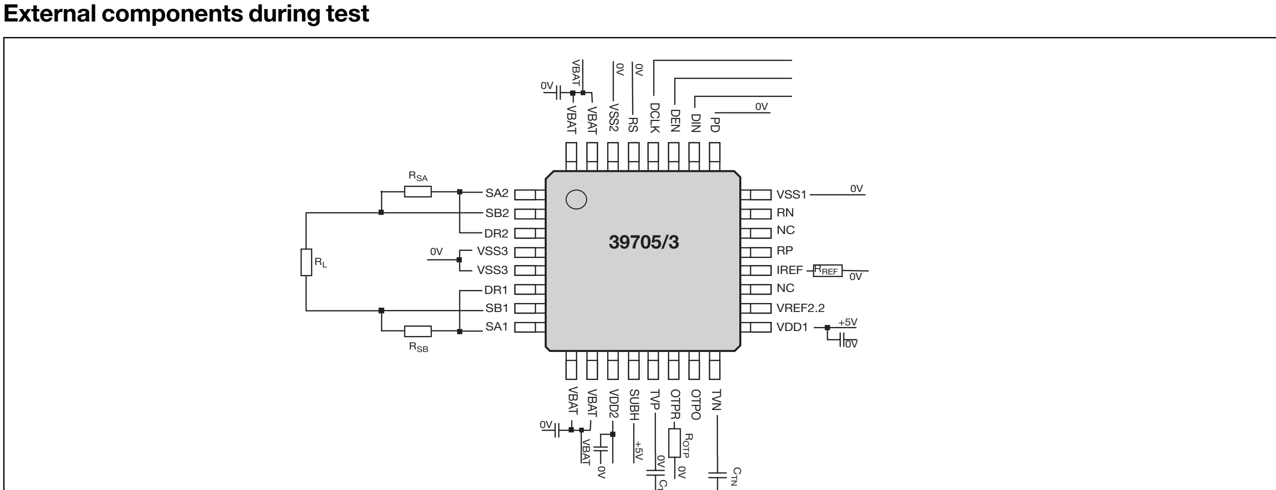


Figure 4. External components during setup.

External Components During Test

Component	Symbol	Value	Unit	Tol.	Comment
Line Load	R_L	25	Ω	1%	0.25W
R_S series resistors	R_{SA}, R_{SB}	2.7	Ω	1%	0.25W
Bias Current Setting Resistor	R_{REF}	24.3	kΩ	1%	0.1W
C_{VDD} Decoupling Capacitor for V_{DD1}	C_{VDD1}	220	nF	10%	
C_{VDD} Decoupling Capacitors V_{DD2}, V_{BAT}	C_{VDD2}, C_{VBAT}	220	nF	10%	
Transmit Input Coupling Capacitor	C_{TP} , C_{TN}	47	nF	10%	

Electrical Characteristics

Power Dissipation & Supply Currents

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Supply Currents	V_{BAT} = 10.0V or 6.0V Power Down mode (PD=5V), no ADSL signal RL = 25Ω	I_{DD1} I_{DD2} I_{BAT}		2.7 4.0 0	5.0 10.0 10.0	mA mA mA
On-chip Power Consumption	$P = \Sigma(I_{DD} \times V_{DD} + I_{BAT} \times V_{BAT})$	P_d		32		mW
Supply Currents	V_{BAT} = 10.0V Power mode 7 (PD=0V), no ADSL Tx signal P2P1P0 = “111”	I_{DD1} I_{DD2} I_{BAT}		11.5 11.5 10.0	12.5 12.5 15	mA mA mA
On-chip Power Consumption	$P = \Sigma(I_{DD} \times V_{DD} + I_{BAT} \times V_{BAT})$	P_{d7}		210		mW
Supply Currents	V_{BAT} = 10.0V Power mode 0 (PD=0V), no ADSL signal	I_{DD1} I_{DD2} I_{BAT}		24.0 23.0 69.0	25.0 24.5 73.0	mA mA mA
On-chip Power Consumption	$P = \Sigma(I_{DD} \times V_{DD} + I_{BAT} \times V_{BAT})$	P_{d0}		922		mW
Supply Currents	V_{BAT} = 10.0V Power mode 2, transmitting ADSL signal PSD = -40dBm/Hz, 0.15–1.1MHz, PAR = 3.8 TX-PGC = +16.5dB	I_{DD1} I_{DD2} I_{BAT}		20.0 25.0 72.0		mArms mArms mArms
On-chip Power Dissipation	$P = \Sigma(I_{DD} \times V_{DD} + I_{BAT} \times V_{BAT}) - I_L^2 \times Z_L$ (1)	P_{d2}		845		mW

Note 1: The power dissipated in the external Z_S impedances are included in the On-Chip power, since this power is dissipated on the board.

Power Supply Rejection Ratio

Parameter	Fig	Condition	Symbol	Min	Typ	Max	Unit	Comment
Tx PSRR (to Line)		V_{PSRR}=0.1V_{PP}, f=550kHz RX-PGC=”00000"=+25.2dB, TX-PGC=”00000"=+21.5dB						
		from V_{DD}	$PSRR_{TDD}$		35		dB	GBD
		from V_{BAT}	$PSRR_{TBAT}$		100		dB	GBD
Rx PSRR (to Receive output)		V_{PSRR}=0.1V_{PP}, 25kHz < f <138kHz, RX-PGC=”00000"=+25.2dB, TX-PGC=”00000"=+21.5dB						
		from V_{DD}	$PSRR_{RDD}$		54		dB	GBD
		from V_{BAT}	$PSRR_{RBAT}$		>80		dB	GBD

Digital Interface, levels

Parameter	Fig	Condition	Symbol	Min	Typ	Max	Unit	Comment
Input Voltage Low			V_{IL}			0.8	V	
Input Voltage High		V_{DD1} = 5 V	V_{IH}	2.4			V	
Input Current		I_{IL} (@V_{IL}), I_{IH}(@V_{IH})	I_{IL}, I_{IH}	-10		10	mA	
Input Capacitance			C_I			10	pF	GBD
Output Voltage Low		@ I_{OL} = 3.2 mA	V_{OL}			0.4	V	GBD
OutputVoltage High		@ I_{OL} = 3.2mA	V_{OH}	2.8			V	GBD

Digital Interface, timing

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Comment
Data clock frequency	Applicable range with rise and fall times <10ns	fM_{CLK}	0.1		35	MHz	GBD
Rise and fall times	Of digital input waveforms	τ_r, τ_f	TBD			ps	GBD

Reference Voltages and Currents

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VREF2.2 voltage		$V_{VRef2.2}$	$0.429 \times V_{DD1}$	$0.440 \times V_{DD1}$	$0.447 \times V_{DD1}$	V
IREF voltage		V_{IRef}	1.20	1.25	1.30	V

Line Driver DC Characteristics

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Comment
Differential Output Offset Voltage*	No input signal, Input offset V_{VTXIN}-V_{VTXINB} = 0 TX-PGC="00000"=21.5dB Output Offset voltage, V_{SB1}-V_{SB2}, open circuit load	V_{LIN}	-1000	240	1000	mV	
Longitudinal Output Offset Voltage	No input signal, Input offset V_{VTXIN}-V_{VTXINB} = 0, Relative VBAT/2, TX-PGC="00000"=21.5dB $V_{Long} = (V_{SB1} + V_{SB2})/2$	V_{OLine}	-150	0	150	mV	
Differential Input Offset Voltage at TXIN		V_{TXINO}	-15	0	15	mV	
Common Mode input Offset Voltage at TXIN	Relative VREF2.2	$V_{TXInLong}$	-15	0	15	mV	

Note : In above table 'LINE' refers to currents or voltages on primary (25Ω) side of 1:2 line output transformer.

* The DC current flowing through the transformer can easily be calculated from the open circuit DC offset by using the Equation below.

$$Ik = \frac{U_O}{11.5 \times R_{SH} + R_L}$$

U_O = Open circuit offset voltage
R_{SH} = Shunt Resistor in the complex impedance network Z_S
R_L = Resistance in the transformer winding

Receive Path DC Characteristics

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Commemt
RP-RN Differential Output Voltage	No Input signal, RX-PGC = "00000" (+25.2dB), Measured with R_{Load} = 0Ω	V_{RXDiff}	-200	0	200	mV	
RP, RN Longitudinal Output Voltage	No input signal, Relative VRREF, RX-PGC = "00000" (+25.2dB)	V_{RXLong}	-50	0	+50	mV	

Line Driver Termination Impedance

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Comment
Differential output impedance	Measured differentially across load pins (SB1, SB2) with R_{AB}=2.2Ω and f=25kHz						
	Control word = “10000” (default)	$ZT_{LINE(10000)}$	25	27	29	Ω	
	Control word = “00000” (min)	$ZT_{LINE(00000)}$	17	18	19	Ω	GBD
	Control word = “11111” (max)	$ZT_{LINE(11111)}$	32	36	40	Ω	
Output impedance step size	Measured differentially across load pins (SB1, SB2) with R_{SX}=2.2Ω and f=500kHz Default control word =”10000"	ΔZT_{LINE}		0.5		Ω	GBD
Termination impedance frequency response	Impedance @ 1.1MHz relative impedance @ 25kHz Default control word =”10000"	$ZT_{f1.1M}$		2.4		Ω	GBD
Termination impedance phase shift	Impedance phase @ 1.1MHz relative impedance @ 25kHz Default control word =”10000"	$\Phi ZT_{f1.1M}$		21		°	GBD

Over Temperature Protection

Parameter	Condition	Symbol	Min	Typ	Max	Unit
ON Temperature		T_{ON}	140	145	150	°C
OFF Temperature		T_{OFF}	125	130	135	°C

Line Driver Transmission Characteristics

Parameter Comment	Fig	Condition	Symbol	Min	Typ	Max	Unit	
Driver output Clip voltage		Max V_{TXIN}, TX-PGC = “00000” (+21.5dB), V_{DD1}=V_{DD2}=5.0V, V_{BAT} = 10.0V, measure V_{SB1}-V_{SB2}	V_{OLCLIP}	15.1	15.2		V	GBD
Slew rate		2Vpp input square wave, Output measured differentially at SB1, SB2 . Slew rate measured for rising and falling edges between 10% and 90% levels.	SR_{LINE}	40	150		V/µs	GBD
Absolute differential voltage gain, TXIN to LINE		V_{in}=0.1Vrms						
		f_{sine} = 25kHz, Max PGC = “00000” (21.5dB)	G_{TX25}	21.4	21.8	22.2	dB	
		f_{sine} = 1.1MHz, Max PGC = “00000” (21.5dB)	$G_{TX1.1M}$	21.6	22.0	22.4	dB	GBD
		f_{sine} = 25kHz, Nom PGC = “01110” (7.5dB)	G_{TX25}	7.4	7.8	8.2	dB	
		f_{sine} = 1.1MHz, Nom PGC = “01110” (7.5dB)	$G_{TX1.1M}$	7.2	7.6	8.0	dB	GBD
		f_{sine} = 25kHz, Min PGC = “10101” (0.5dB)	G_{TX25}	0.4	0.8	1.2	dB	GBD
		f_{sine} = 1.1MHz, Min PGC = “10101” (0.5dB)	$G_{TX1.1M}$	0.2	0.6	1.0	dB	GBD
		Signal TXIN to LINE						
Frequency response		V_{in}=0.1Vrms, f_{sine}=1.1MHz ΔG_{TX}=G_{TX}(25kHz) - G_{TX} (1100kHz) Signal TXIN/TXINB to SB1/SB2	ΔG_{TX}		-0.15		dB	GBD
TX-PGC step size			TX_{STP}		1.0		dB	GBD
Phase response		V_{in}=0.1Vrms, fsine=1.1MHz $\Delta\phi_{TXD}$=ϕ_{TX}(25kHz) - ϕ_{TX}(1100kHz) Signal TXIN/TXINB to SB1/SB2	ϕ_{TXD}		-6		°	GBD
Differential phase error*		Vin=0.1Vrms, fsine=1100kHz, phase at V_{OLDC}=40%of V_{OLCLIP} rel. phaseatV_{OLDC}=0V	ϕ_{TXDE}		2.5		°	GBD

Line Driver Transmission Characteristics continued ...

Parameter	Fig	Condition	Symbol	Min	Typ	Max	Unit	Comment
SFDR, sine at output, single tone		TX-PGC= "00111" (+14.5dB)						
		f_{sine} =25kHz, 8.0Vpp on output	$SFDR_{25k}$	53	58	70	dB	
		f_{sine} =138kHz, 8.0Vpp on output	$SFDR_{138k}$	51			dB	
		f_{sine} =250kHz, 8.0Vpp on output	$SFDR_{250k}$	47			dB	GBD
		f_{sine} =400kHz, 8.0Vpp on output	$SFDR_{400k}$	44			dB	GBD
		f_{sine} =400kHz, 14.0Vpp on output	$SFDR_{14}$	42			dB	
		f_{sine} =400kHz, 1.0Vpp on output	$SFDR_{1}$	57			dB	GBD
MTPR transmit multitone		$f_{multitone}$=150kHz - 1.1MHz, MTPR measured relative notches, Power Mode=2						
		TX-Band : 150kHz-1.1MHz @bin37=160kHz, bin57=245kHz, bin117=504kHz bin174=750kHz, bin234=1MHz, PAR=5.0	$MTPR_{5.0TX}$	44	47		dB	
		bin37=160kHz, bin57=245kHz, bin117=504kHz, bin174=750kHz,bin234=1MHz, PAR=3.8	$MTPR_{3.8TX}$	47	50		dB	
		PAR=3.8, PSD=-40dBm/Hz (11.7Vpp), TX-PGC=15.5dB PAR=5.0, PSD=-40dBm/Hz (15.4Vpp), TX-PGC=17.5dB						
MTPR transmit multitone -into Rx band		$f_{multitone}$=150kHz - 1.1MHz, MTPR measured relative Rx-band, Power Mode=2						
		300Hz-4.3kHz, PAR=5.0 (Speech Band)	$MTPR_{5SP}$	49	55		dB	
		25-138kHz, PAR=5.0 (RX Band)	$MTPR_{5RX}$	31	42		dB	
		300Hz-4.3kHz, PAR=3.8 (Speech Band)	$MTPR_{3SP}$	51.5	59.0		dB	
		25-138kHz, PAR=3.8 (RX Band)	$MTPR_{3RX}$	41.0	51.5		dB	
		on driver output PAR=3.8, PSD=-40dBm/Hz (11.7Vpp), TX-PGC=15.5dB PAR=5.0, PSD=-40dBm/Hz (15.4Vpp), TX-PGC=17.5dB						
MTPR transmit multitone -into "out of band" band		$f_{multitone}$=150kHz - 1.1MHz, MTPR measured relative Out Of-band: > 1.1MHz on driver output Power Mode=2	$MTPR_{5.0OB}$	39	42		dB	
		PAR=3.8, PSD=-40dBm/Hz (11.7Vpp)	$MTPR_{3.8OB}$	36.0	39.0		dB	
		PAR=5.0, PSD=-40dBm/Hz (15.4Vpp)						
Idle noise floor at output		No input signal. TXP, TXN connected to VREF2.2. Noise floor measured across SB1, SB2, TX-PGC= "00111" (+14.5dB)						
		300Hz-4.3kHz	$NF_{LINEidle}$		-92.0	-87.0	dBm/Hz	into 25Ω
		25kHz-138kHz			-104.0	-101.0		
		150kHz-1.1MHz			-107.5	-106.0		
		1.1MHz-11.04MHz			-109.0	-107.5		GBD
Unbalance_TL	6	V_{in}=1Vrms, R_L = 2×12.5Ω, measured at load midpoint, ratio (dB) to Differential signal across load.						
		25kHz	UNB_{TL}			-34.5	dB	GBD
		500kHz				-34.5	dB	
		1.1MHz				-31.0	dB	GBD
Unbalance_LT	6	$V_{in\ load\ mid}$ = 1Vrms, R_L = 2×12.5Ω, measure VSB1-VSB2, ratio (dB) to Differential signal across load.						
		25kHz	UNB_{LT}			-30	dB	GBD
		500kHz				-28	dB	GBD
		1.1MHz				-23	dB	GBD
TX input impedance		f < 1.1 MHz	Z_{inTX}		4.9		kΩ	GBD

Receive Path Transmission Characteristics

Parameter	Fig	Condition	Symbol	Min	Typ	Max	Unit	Comment
Receive output clip voltage		V_{LINE}=2Vpp, f_{sine}=25kHz, RxPGC = “00000” (25.2dB), measured differentially at ROUTP/ROUTN, *)VBAT = 10V.	$V_{RXOCLIP}$	5			Vpp	GBD
Receive output slew rate		2Vpp input square wave, Output measured differentially at ROUTP/ROUTN. Slew rate measured for rising and falling edges between 10% and 90% levels, RX-PGC=”10100" (6.2dB)	SR_{RO}	20	50		V/ms	GBD
Absolute differential voltage gain		V_{LINE}=0.2Vpp (input to SB1/SB2), f_{sine}=25kHz, RX-PGC=”10111" (3.2dB), measure LINE to Receive output ROUTP/ROUTN, TX-PGC = “00111” (+14.5dB)	G_{RX}	1.3	1.7	2.1	dB	
		RX-PGC = “00000” (+25.2dB), @25kHz	G_{RX}	23.2	23.6	24.0	dB	GBD
Frequency response		V_{LINE}=0.2Vpp, f_{sine}=138kHz, RX-PGC=”00110" (20.2dB) ΔG_{RX}=G_{RX} (25kHz) - G_{RX} (138kHz) measure gain LINE to ROUTP/ROUTN	ΔG_{RX}	0.3	0.0	-0.3	dB	GBD
Phase response		V_{in}=0.2Vpp, f_{sine}=138kHz, RX-PGC=”10001" (+9.2dB) $\Delta\phi_{RX}$ = ϕ_{RX}(25kHz) - ϕ_{RX} (138kHz) measure phase LINE to ROUTP/ROUTN	$\Delta\phi$RX		-3	TBD	°	GBD
Differential phase error*		0.2Vpp sine wave at f=138kHz, RX-PGC=”10001" (+9.2dB), phase at $V_{RXOUTDC}$ = 40% of $V_{RXOCLIP}$ relative phase at $V_{RXOUTDC}$ = 0V	ϕ_{RXE}		0.25		°	GBD
Rx_{PGC} step size			Rx_{PGC_stp}		1.0		dB	GBD
Rx SFDR, sine		TX-PGC = “00111” (+14.5dB) a) RX-PGC=”00000" (+25.2dB)						
		f_{sine} = 25kHz, U_{LINE} = 0.11Vpp, U_{RX} = 2.0Vpp	$SFDR_{RA25k}$			54	dB	GBD
		f_{sine} =138kHz, U_{LINE} = 0.11Vpp, U_{RX} = 2.0Vpp	$SFDR_{RA138k}$			54	dB	GBD
		c) RX-PGC=”00000" (+25.2dB)						
		f_{sine} = 138kHz, U_{LINE} = 0.22Vpp, U_{RX} = 4.0Vpp	$SFDR_{RC4}$		71.5	68.0	dB	
		f_{sine} =138kHz, U_{LINE} =0.165Vpp, U_{RX} =3.0Vpp	$SFDR_{RC3}$			68.0	dB	GBD
		f_{sine} =138kHz, U_{LINE} =0.055Vpp, U_{RX} =1.0Vpp	$SFDR_{RC1}$			68.0	dB	GBD
Rx MTPR-into Rx band, multitone		V_{inLINE} = 0.39Vpp, PAR = 3.8, RX-PGC=”00110" (+20.2dB) $f_{multitone}$ = 25kHz - 138kHz MTPR measured relative notches @bin13=56063kHz and @bin24=103.5kHz	$MTPR_{R6}$	53	55		dB	GBD
Rx idle noise floor		No input signal, RxPGC= “00000” (+25.2dB) Noise Floor transformed to LINE						
		300Hz - 4.3kHz				-122.0	dBm/	GBD
		25kHz - 138kHz	$NFidle_{RX}$			-121.0	Hz into	
		150kHz - 1.1MHz				-125.0	25Ω	
		1.1MHz - 11.0MHz				-128.0		GBD

Transmit to Receive Path AC Characteristics (Echo Cancellation)

Parameter	Fig	Condition	Symbol	Min	Typ	Max	Unit	Comment
Echo cancellation multitone		TX: multitone = 150kHz-1.1MHz applied to TXP/TXN, U_{in} = 2.0Vpp, PAR=5.0, PSD_{LINE} = -40dBm/Hz, TX-PGC=”00100" (+16.5dB), RxPGC= “00000” (+25.2dB) Power Mode = 2 Echo_cancellation = spectrum(LINE)-spectrum(RXOUT)						
		Echo Canc, @f=150kHz,	EC_{150k}		24		dB	GBD
		Echo Canc, @f=500kHz,	EC_{500k}		14		dB	GBD
		Echo Canc, @f=1.1MHz,	$EC_{1.1M}$		8		dB	GBD
MTPR transmit multitone -into Rx band		$f_{multitone}$=150kHz-1.1MHz, MTPR measured relative Rx-band: Power Mode=2						
		25kHz, PAR=5.0	$MTPR_{5RA1}$		TBD		dB	GBD
		138kHz, PAR=5.0	$MTPR_{5RA2}$		TBD		dB	GBD
		25kHz, PAR=3.8	$MTPR_{3RA1}$		TBD		dB	GBD
		138kHz, PAR=3.8	$MTPR_{3RA2}$		TBD		dB	GBD
		on RX Output, RX-PGC=”00000" (+25.2dB) PAR=3.8, PSD=-40dBm/Hz (11.7Vpp), TX-PGC=+15.5dB PAR=5.0, PSD=-40dBm/Hz (15.4Vpp), TX-PGC=+17.5dB						
Echo cancellation singletone		TX:single tone with fs applied to TXP/TXN, U_{in} = 1.5Vpp, TX-PGC = ”00111"(+14.5dB), RxPGC = ”00000" (+25.2dB) Echo_cancellation at RXOUT, transformed to LINE						
		Echo Canc, @fs = 150kHz, fundamental, fs	EC_{150k0}	25.5	30.0		dB	
		first spurious, 2xfs	EC_{150k1}	19.5	31.0		dB	
		second spurious, 3xfs	EC_{150k2}	30.5	33.0		dB	
		Echo Canc, @fs = 400kHz,	EC_{40k0}	28.0	34.0		dB	
		fundamental, fs	EC_{400k1}	26.0	40.0		dB	
		first spurious, 2xfs	EC_{400k2}	35.0	41.0		dB	
		second spurious, 3xfs						

1. Apply the multitone at TX, measure the fundamental levels on LINE
2. Transform this fundamental level to RXOUT by adding the RX-PGC factor
3. Measure the spectrum at RXOUT and calculate MTPR from the fundamental level calculated in 2.

Transmitter Output Spectral Mask

The required spectral mask from the standard is met, provided that the driver is connected to the line via the proposed hybrid (transformer and LINE capacitor combination) and provided that the driver is driven from a DAC with at least 6dB lower distortion and noise floor than the PBM 39705/3 TX path. See figure 5.

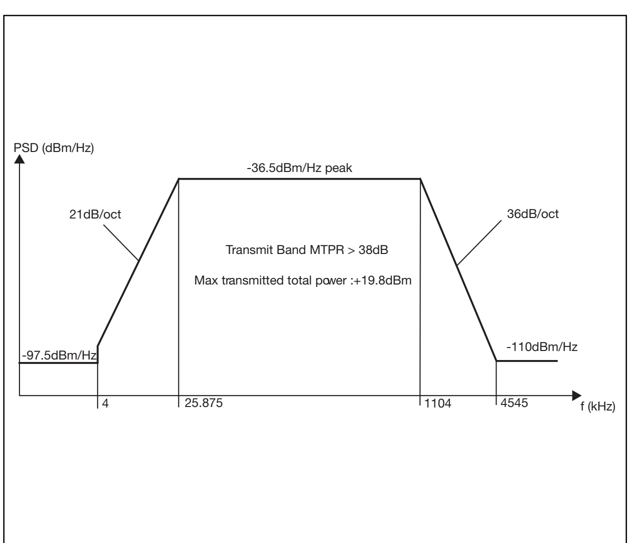


Figure 5. Transmitted spectral mask.

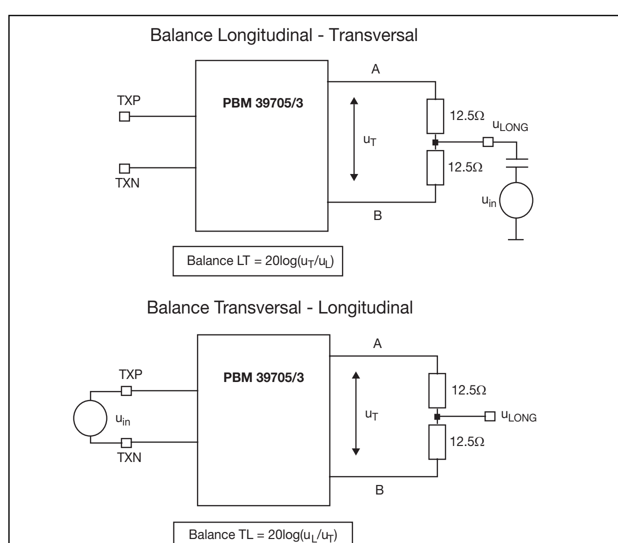
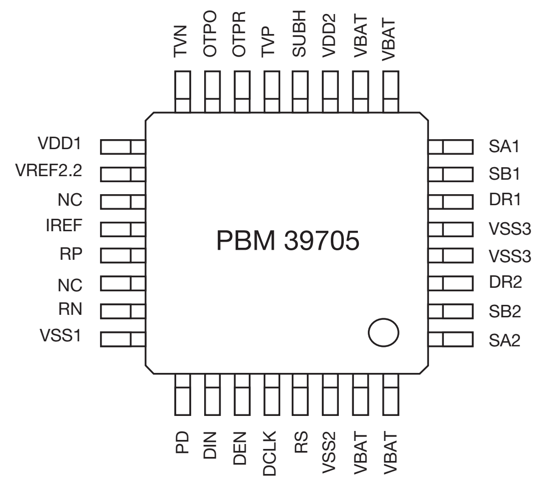


Figure 6. Longitudinal balance measurement.

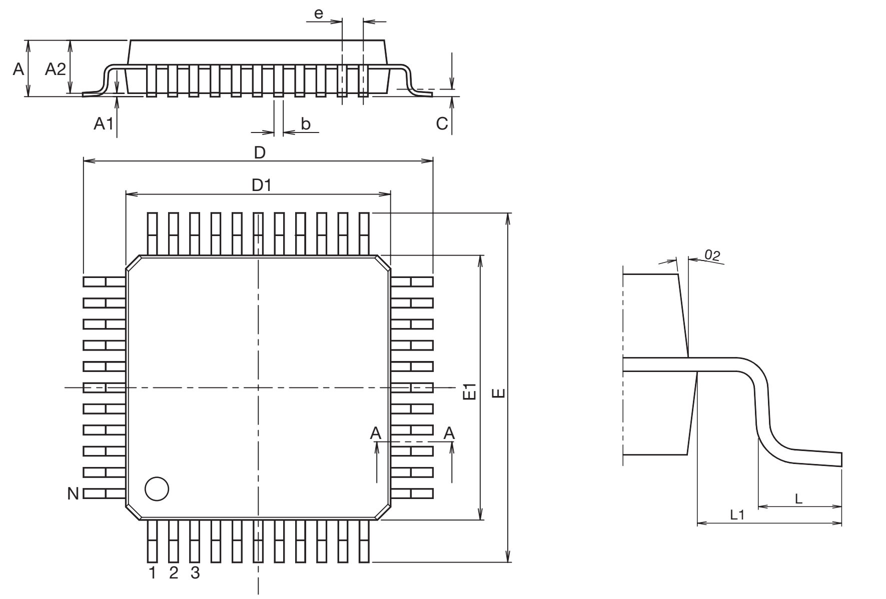
Pin Description



Pin	Name	Description	Supply/GND	A/in	A/out	D/in	Misc
1	SA2	1 of 2 current sense input pins for B-wire to define current gain.		x			Sensitive
2	SB2	Current and voltage sense input for B-wire to define current gain and impedance.		x			Sensitive
3	DR2	Drive output to line, B-wire.			x		High Cur
4	VSS3	Ground For Driver High Current Output Stage.	x				High Cur
5	VSS3	Ground For Driver High Current Output Stage.	x				High Cur
6	DR1	Drive output to line, A-wire.			x		High Cur
7	SB1	Current and voltage sense input for A-wire to define current gain and impedance.		x			Sensitive
8	SA1	1 of 2 current sense input pins for A-wire to define current gain.		x			Sensitive
9	VBAT	Battery sourcing drive output current (VBAT).	x				High Cur
10	VBAT	Battery for setting half supply voltage level on drive output pins 3 & 6. This is normal connected to the same supply as VBAT.	x				High Cur
11	VDD2	Main positive supply input for signal currents, except for drive output currents.	x				High Cur
12	SUBH	Connection to substrate used to isolate high voltage and high current output transistors from low voltage side to reduce crosstalk via the substrate.	x				Sensitive
13	TVP	Transmit input voltage, ~2.4kΩ to internal 2.2V reference		x			Sensitive
14	OTPR	Over temperature protection resistor			x		
15	OTPO	Over temperature protection output indicator, active high, can be used directly to power down the chip or to indicate high chip temperature.			x		
16	TVN	Transmit input voltage, ~2.4kΩ to internal 2.2V reference.		x			Sensitive
17	VDD1	5V supply for bias network and for digital serial bus and register.	x				High Cur
18	VREF2.2	Buffered output of internal 2.2Volt reference, used to bias tx input circuit via package bond-out arrangement and also to provide receive reference voltage, to pin22, for the receive output.			x		Sensitive
19	NC	Do not use.					
20	IREF	Current bias generation. A resistor to ground, pin 24, sets the bias current for all the internal circuits. Nominal resistor value used is 25kΩ, but could be nearest preferred value.			(x)		Sensitive
21	RP	Receive output signal, differential with signal from pin 23. The receive signal appearing at pins 21 and 23 is echo cancelled to ~>20dB from the transmit signal for frequencies up to 300KHz.			x		
22	NC	Do not use.					
23	RN	Receive output signal differential to that on pin 21.			x		
24	VSS1	Ground for all dc chip biasing and for connection to substrate on the low voltage side of the chip. It is also the ground for the digital and the main ESD ground for the chip.	x				High Cur
25	PD	Active high, 3.3V or 5V compatible input to power down the chip except for the bandgap, on-chip temperature monitor and a few other low current circuits.				x	
26	DIN	Serial DATA signal input. 3.3V and 5V compatible				x	
27	DEN	Active pulsed low DATA ENABLE input. 3.3V and 5V compatible. All settings are updated on the falling edge of this signal.				x	
28	DCLK	DATA CLOCK input. 3.3V and 5V compatible.				x	
29	RS	Active high RESET input. 3.3V and 5V compatible. Resets defaults values for Transmit gain, Receive gain, Impedance and Standby on the negative edge. DEN must be pulsed low during reset.				x	
30	VSS2	Main signal ground for chip, except for drive output currents.	x				High Cur
31	VBAT	Battery sourcing drive output current (VBAT).	x				High Cur
32	VBAT	Battery sourcing drive output current (VBAT).	x				High Cur

LQFP package outline

Common dimensions			
	Min	**Typ**	**Max**
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	–	0.20
e		0.8 BSC	
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 Ref	
O2	11°	12°	13°



Functional Description

The PBM 397 05/3LQ is a complete ADSL line interface circuit, optimized to be used at the Central Office (CO) side.

Standard Requirements

The PBM 397 05/3LQ is a complete integrated Analog line driver and receiver for ADSL (Assymetrical Digital Subscriber Line). The device handles both full-rate ADSL (G.DMT as standardized in ITU G.992.1 and ANSI T1.413 Issue 2) and ADSL-Lite (G.Lite as standardized in ITU G.992.2) .

Two Power Supplies

The PBM 397 05/3LQ requires two power supplies: VBAT (6-11V) for the final drive output stage, and VDD (5V) for the rest of the device.
VDD shall always be set to 5.0V. For applications with long lines , it is recommended to use a typical supply voltage V_{BAT} of 10.5V, but as the line gets shorter, the power supply (and thus the power consumption) can be reduced. The recommended power supply voltage for different output voltages is given in the table 1. The drive outputs are centred on $V_{BAT}/2$ DC level using a longitudal loop. See figure 7.

Serial digital control interface

The driver is programmable in order to maximize the performance and minimize the Power consumption. The programmability is controlled via a serial control interface. The interface has a chip select signal (DEN), that enables the same digital bus to be used for all line drivers on a line card, reducing board area. The digital interface can be programmed from either 3.3V or 5V circuits. See Figure 8.

The following functions can be programmed :
- Transmit gain (-1.7db to +21.3dB in 1dB steps). In order to be able to perform Power Cut Back in 1dB steps between -38dBm/Hz to -52dBm/Hz, according to the ADSL standard.
- Receive gain (-4.7dB to +25.3dB in 1dB steps) in order to give a high SNR (Signal to Noise Ratio) before the AD converter for all line lengths.

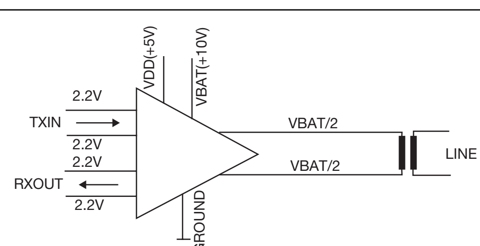


Figure 7. Power supplies and DC levels for the PBM 397 05/3LQ.

Line Length (AWG 26)	U_{out} tot (Vpp)	$VBAT_{min}$ (V)
> 800m	16.4	10.5
600m	13.3	8.7
500m	10.7	7.2
400m	8.8	6.0
< 300m	7.4	6.0

Table 1. Line length.

- Termination impedance (17-32.5Ω in 0.5Ω steps) in case the user wants to be able to tune the impedance without changing any external components. However, it is recommended, to achieve the best performance to set the programmable impedance to 25Ω and use the complex termination impedance described in the application drawing.
- Power mode : The device can be set in either power mode 0-2 for full ADSL transmission. In the remaining power modes (3-7), ADSL transmission is also possible, but with limited performance (could be used for example on short lines or lines which are very noisy or when no data is sent). See figure 10.

Power Down

PBM 397 05/3LQ has a power down function (through the PD pin), that completely shuts down the circuit. This pin can be directly connected to the OTPO pin (the Over Temperature detection Output), so that the circuit is automatically shut down during error conditions.

Integrated Over Temperature Protection

In order to protect the circuit from damage during error conditions, such as short circuit, there is an on-chip over temperature detection circuit (OTP). During overtemperature conditions the digital over temperature detector output (OTPO) is set high and can either be monitored by the system processor or connected directly to the Power Down pin of the PBM 397 05/3LQ. The OTP has 15 degrees centigrade built-in hysteresis to avoid thermal oscillation effects. See figure 9.

Active Drive/Termination Impedance

The circuit is able to deliver 15.5Vpp into a 25Ω load, enough to transmit ADSL signals between 150kHz and 1.1MHz with a Power Spectral Density (PSD) of -40dBm/Hz into 100Ω via a 2:1 transformer or a total power of 19.8dBm (3.08Vrms) with a PAR (Peak to Average Ratio) value up to 5.2, while receiving an upstream band between 25kHz and 138kHz, according to the ANSI (T1.413 Issue 2) and ETSI ADSL standards.

The line driver manages to meet this performance with an output stage fed between 0 and 10.5V and a total power consumption of 850mW. This is possible by the use of Ericsson Microelectronics patented active termination/drive impedance scheme for ADSL. See figure 11.

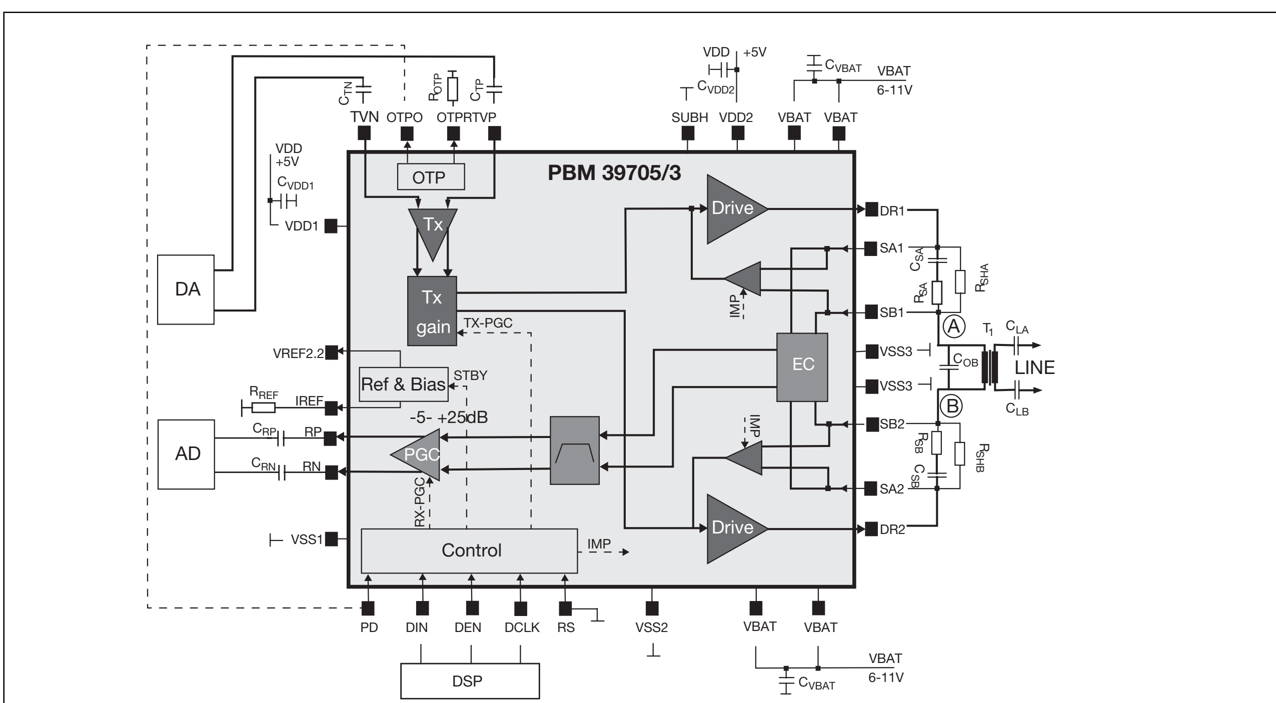
The active drive/termination impedance principle.

The active termination concept means that no high ohmic series resistors are needed in series with the driver output, which reduces the power suppy voltage needed to transmit a given power to the line. All that is needed is a low-ohmic (in the ADSL band) sense impedance in series with the output.

Programmable transmit gain

Programmable transmit gain enables power cut-back according to standard and easy implementation of extended power cut-back.

ANSI T1.413 requires that the Transmitted Power Spectral Density (PSD) to the line should be reduced in 2dB steps from -40dBm/Hz down to -52dBm/Hz when the line length (and the line damping) is reduced.



Overview.

The PBM 397 05/3LQ has been designed to meet this requirement when connected to DA converters (or amplifiers) with a max output swing between 1.5Vpp and 4.0Vpp. It is also possible to adjust the transmit power, since the TX-PGC step is 1dB.
The TX-PGC is controlled through the serial control interface. The principle for calculating the internal Transmit Gain is shown in figure 12.

Differential Input- and Output Interfaces
The transmit input interface is a differential voltage interface. The driver should be connected to the output from the DAC via AC coupling capacitors. The maximum transmit input swing is 4Vpp, and the TX inputs have a common-mode level of 2.2V. See figure 13.
The Receive output interface is also differential and of voltage type. The RX outputs should be connected via external AC-coupling capacitors to the AD converter input. The maximum output swing is 4Vpp. The RX outputs have a common mode level of 2.2V.
See figure 14.

Integrated echo cancellation circuit
In an ADSL system, the key performance parameter is the MTPR (Multi Tone Power Ratio) of the receive signal. In order to maximize the MTPR, the PBM 397 05/3LQ has an integrated echo canceller that removes around 25dB of the transmitted signal from the Receive Path. In order to further reduce the transmitted echo signal to the receiver, a first order low pass filter with a corner frequency of 300kHz has been integrated. A 10kHz high pass filter is also integrated in the receive path to reduce POTS signals.
It is important to note that it is not only the fundamental transmitted tones that are echocancelled, but also noise and distortion from the driver will be cancelled to the receive path. This enables higher transmit distortion and noise in the transmit path without sacrificing bitrate. See figure 15 and 16.

How to choose Z_S

A good echo cancellation is achieved when the drive/termination impedance of PBM 39705 matches the load impedance (the line seen through the transformer and the high-pass filter LINE capacitors). The expression for the termination impedance is given by:

$Z_{Out} = 11.5\ Z_S$

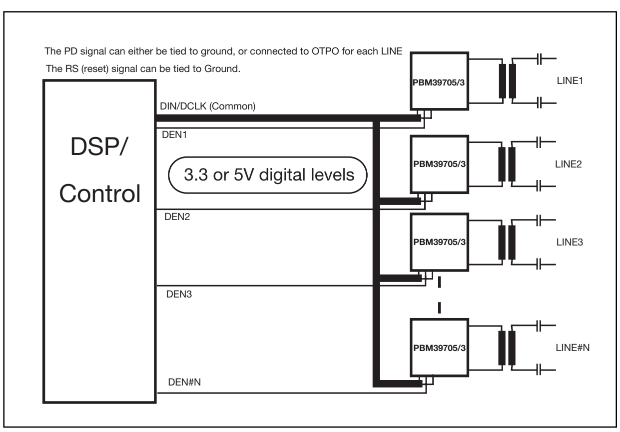


Figure 8. Digital control routing on a multiline board.

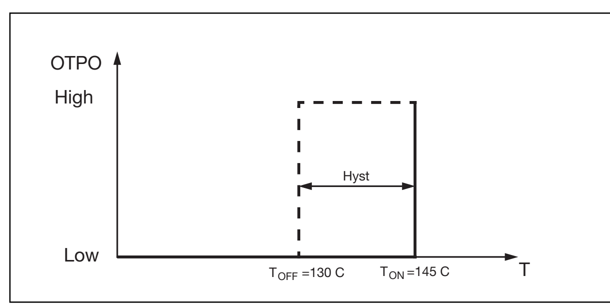


Figure 9. Over Temperature Protection (OTP).

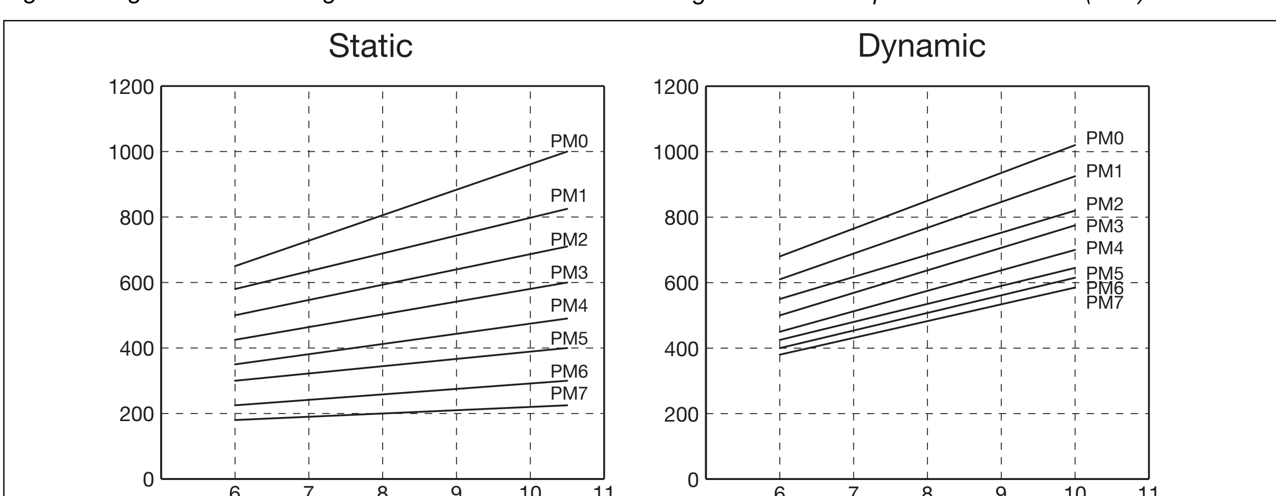


Figure 10. Static and dynamic power consumption in active mode vs VBAT (VDD=5.0V).

To get the optimum performance, Z_S must be chosen for a specific transformer and line capacitor combination. The proposed solution from Ericsson Microelectronics is to use the Schott transformer 32828 in combination with two 150nF LINE high pass filter capacitors. Ericsson Microelectronics can also provide Z_S for other transformer/LINE capacitor combinations on request.
The propsed Z_S is optimized to give the best impedance matching in the ADSL-band for the AWG26 (0.4mm) cable, but the proposed Z_S will work fine for the AWG24 (0.5mm) cable as well.
See figure 17 and 21.
The termination/drive impedance of the PBM 39705/3LQ is obtained by using:

$$Z_{Out} = \frac{11.5 \times Rsh \times (1+2\pi f \times Cs \times Rs)}{1 + 2\pi f \times Cs \times (Rs + Rsh)}$$

The factor 11.5 is valid for the nominal impedance setting: “10000” and can be varied between 7.8 and 15.0.

The impedance in equation above shall now be matched with the load impedance of the driver, ie the terminated transmission line seen through the transformer and the LINE high-pass filter capacitors.

High range Receive Programmable Gain (PGC)

The signal levels after echo cancellation is very low. In order to get a maximal MTPR at the AD converter input, the signal level must be boosted up to match the optimal input swing for the AD converter.
This is achieved by using a Programmabe Receive Gain (PGC). The RX gain from the line driver output to the Receive outputs can be varied via the serial digital interface in 1dB steps between -4.7dB and +25.3dB. Normally the lower PGC values are used for shorter lines and higher PGC’s are used for longer lines. The PGC to be used will be set from the DSP during the training sequence of the ADSL connection.

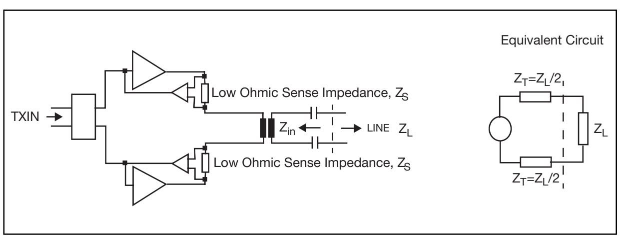


Figure 11. Drive impedance.

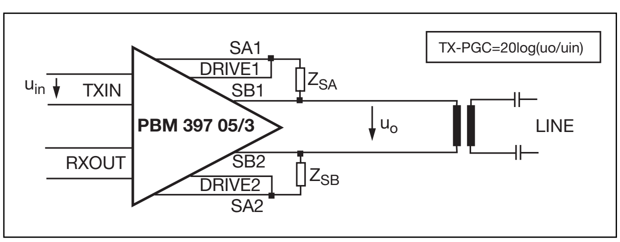


Figure 12. Calculating the transmit gain (TX-PGC).

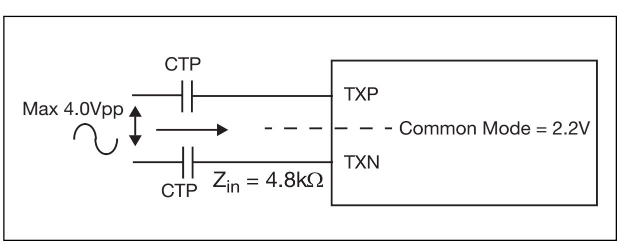


Figure 13. The differential transmit input interface.

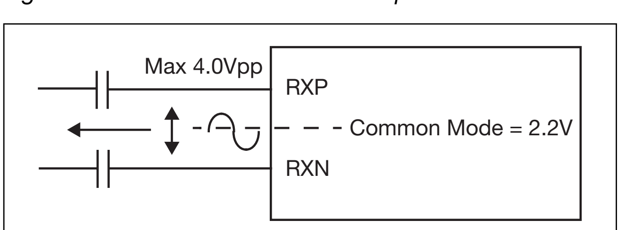


Figure 14. The differential receive output interface.

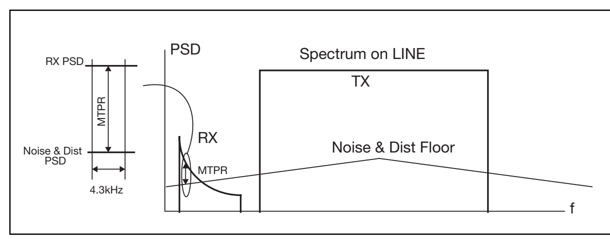


Figure 15. The spectrum on the LINE.

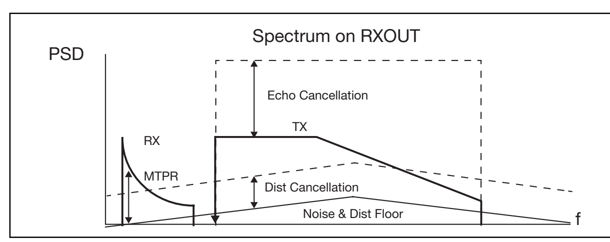


Figure 16. The spectrum on the receive output.

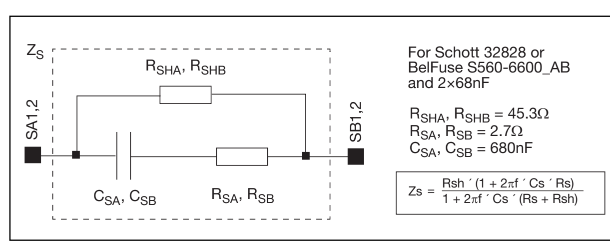


Figure 17. Proposed Z_S.

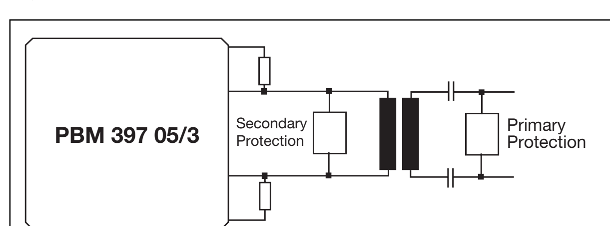


Figure 18. Over Voltage Protection.

Over Voltage Protection

In a Central Office protection, it is recommended to use a primary protection outside the transformer and a secondary protection inside the transformer, see fig 18. At the moment, Ericsson Microelectronics has a proposal for an OVP scheme for the PBM 39705/3LQ, but this scheme need to be verified practically.

Programming The Device

The device is programmed by using the Serial Data Control Interface (DIN, DCLK & DEN).

The Serial Control Word is 18 bits wide. Bit 17 is sent first and Bit 0 is sent last. Data is clocked in on each clock cycle, positive edge. After all bits have been read in, the DEN signal should be pulsed low for the new settings to take effect. See figure 19.

Important! On a board with many lines : All DEN must be set high, before a new serial data word could be sent.

Resetting the device

There is a default programming for the device. This default word is automatically loaded into the register when the device is reset. See figure 20.

There are two ways of resetting the device without sending any serial data :

1. Power -On Reset : Once the power supply VDD is applied to the device, the PBM 397 05/3LQ will be reset automatically.
2. Reset via the RS pin : Provided that DEN is held low, the PBM 397 05/3LQ is reset once the RS pin is set high. Once the reset has been made, the RS pin must be brought low again, to ensure proper function of the programming.

Transmit Gain (5 bits)					Receive Gain (5 bits)					Term. Impedance (5 bits)					Power (3 bits)		
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	R4	R3	R2	R1	R0	I4	I3	I2	I1	I0	P2	P1	P0

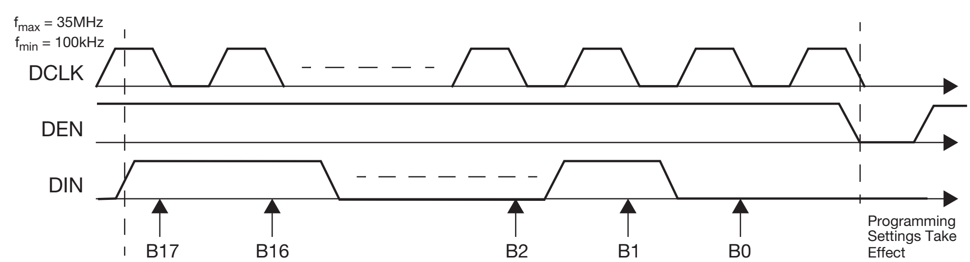


Figure 19. The function of the serial control interface.

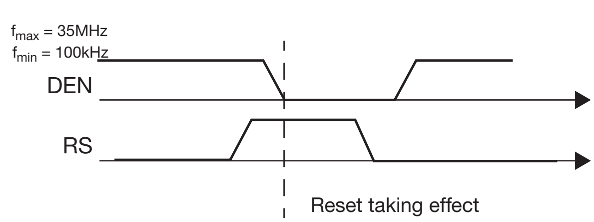


Figure 20. Resetting the device.

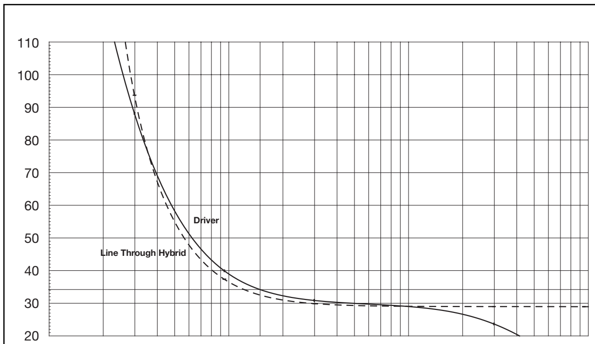


Figure 21. Impedance matching between line driver and the line (AWG 26 cable) seen through the transformer and high pass filter capacitors.

Transmit Gain Control (TX-PGC) Supporting Full Power Cut Back

[T4 .. T0]	Tx_{PGC} (res Z_S)	Tx_{PGC} (complex Z_S)	Comments
00000	21.5 dB	21.3 dB	@ 150kHz
00001	20.5 dB	20.3 dB	
00010	19.5 dB	19.3 dB	
00011	18.5 dB	18.3 dB	Use when transmitting 150 kHz - 1.1 MHz with -40 dBm/Hz and PAR = 5.3x from a 2.0 Vpp DAC
00100	17.5 dB	17.3 dB	
00101	16.5 dB	16.3 dB	
00110	15.5 dB	15.3 dB	Default when reset
00111	14.5 dB	14.3 dB	
01000	13.5 dB	13.3 dB	
01001	12.5 dB	12.3 dB	Use when transmitting 150 kHz - 1.1 MHz with -40 dBm/Hz and PAR = 5.3x from a 4.0 Vpp DAC
01010	11.5 dB	11.3 dB	
01011	10.5 dB	10.3 dB	
01100	9.5 dB	9.3 dB	
01101	8.5 dB	8.3 dB	
01110	7.5 dB	7.3 dB	
01111	6.5 dB	6.3 dB	Use when transmitting 150 kHz - 1.1 MHz with -52 dBm/Hz and PAR = 5.3x from a 2.0 Vpp DAC
10000	5.5 dB	5.3 dB	
10001	4.5 dB	4.3 dB	
10010	3.5 dB	3.3 dB	
10011	2.5 dB	2.3 dB	
10100	1.5 dB	1.3 dB	
10101	0.5 dB	0.3 dB	Use when transmitting 150 kHz - 1.1 MHz with -52 dBm/Hz and PAR = 5.3x from a 4.0 Vpp DAC
10110	-0.5 dB	-0.7 dB	
10111	-1.5 dB	-1.7dB	
11000	-	-	Not Valid
11001	-	-	- " -
11010	-	-	- " -
11011	-	-	- " -
11100	-	-	- " -
11101	-	-	- " -
11110	-	-	- " -
11111	-	-	- " -

Receive Gain Control (RX-PGC)

[R4 .. R0]	Rx $_{PGC}$ (res Z_s)	Rx $_{PGC}$ (complex Z_s)	Comments
00000	+25.2 dB	+25.3 dB	@ 80kHz (f_c for the upstream Receive Band)
00001	+25.2 dB	+25.3 dB	To be used on long lines
00010	+24.2 dB	+24.3 dB	
00011	+23.2 dB	+23.3 dB	
00100	+22.2 dB	+22.3 dB	
00101	+21.2 dB	+21.3 dB	
00110	+20.2 dB	+20.3 dB	
00111	+19.2 dB	+19.3 dB	
01000	+18.2 dB	+18.3 dB	
01001	+17.2 dB	+17.3 dB	
01010	+16.2 dB	+16.3 dB	
01011	+15.2 dB	+15.3 dB	
01100	+14.2 dB	+14.3 dB	
01101	+13.2 dB	+13.3 dB	
01110	+12.2 dB	+12.3 dB	
01111	+11.2 dB	+11.3 dB	
10000	+10.2 dB	+10.3 dB	
10001	+9.2 dB	+9.3 dB	
10010	+8.2 dB	+8.3 dB	
10011	+7.2 dB	+7.3 dB	
10100	+6.2 dB	+6.3 dB	
10101	+5.2 dB	+5.3 dB	
10110	+4.2 dB	+4.3 dB	
10111	+3.2 dB	+3.3 dB	Default when reset
11000	+2.2 dB	+2.3 dB	
11010	+0.2 dB	+0.3 dB	
11011	-0.8 dB	-0.7 dB	
11100	-1.8 dB	-1.7 dB	
11101	-2.8 dB	-2.7 dB	To be used on a 0m line when using a ADC with U_{inmax} = 4.0Vpp
11110	-3.8 dB	-3.7 dB	
11111	-4.8 dB	-4.7 dB	To be used on a 0m line when using a ADC with U_{inmax} = 3.0Vpp

A high Receive PGC is needed to take full advantage of the built-in echo cancellation and echo filtering of the PBM 39705. The Receive PGC to be used should be decided by the DSP during the ADSL training sequence. The total signal on the line is dominated by the transmitted downstream signal compared to the received upstream signal, except for very short lines.
The fully integrated echo cancellation circuitry effectively removes around 30dB of the transmitted signal from the receiver, which means an improved dynamic range for the upstream receive signal at the AD convertor, relaxing the requirements on the AD converter linearity and resolution. The lowest PGC shall ensure that the ADSL connection can run at a 0m line without clipping the RX output signal.

Termination Impedance Control (ZT)

[I4 .. I0]	Z_T after 2:1 transformer.	Z_T, no transformer.	Comment
00000	68.0Ω	17.0Ω	
00001	70.0Ω	17.5Ω	
00010	72.0Ω	18.0Ω	
00011	74.0Ω	18.5Ω	
00100	76.0Ω	19.0Ω	
00101	78.0Ω	19.5Ω	
00110	80.0Ω	20.0Ω	
00111	82.0Ω	20.5Ω	
01000	84.0Ω	21.0Ω	
01001	86.0Ω	21.5Ω	
01010	88.0Ω	22.0Ω	
01011	90.0Ω	22.5Ω	
01100	92.0Ω	23.0Ω	
01101	94.0Ω	23.5Ω	
01110	96.0Ω	24.0Ω	
01111	98.0Ω	24.5Ω	
10000	100.0Ω	25.0Ω	Default when reset
10001	102.0Ω	25.5Ω	
10010	104.0Ω	26.0Ω	
10011	106.0Ω	26.5Ω	
10100	108.0Ω	27.0Ω	
10101	110.0Ω	27.5Ω	
10110	112.0Ω	28.0Ω	
10111	114.0Ω	28.5Ω	
11000	116.0Ω	29.0Ω	
11001	118.0Ω	29.5Ω	
11010	120.0Ω	30.0Ω	
11011	122.0Ω	30.5Ω	
11100	124.0Ω	31.0Ω	
11101	126.0Ω	31.5Ω	
11110	128.0Ω	32.0Ω	
11111	130.0Ω	32.5Ω	

The impedances given in the table are achieved when using a pure resistive Z_{SA} and Z_{SB} of 2.2Ω.
In order to achieve higher upstream bitrate, it is recommended to use a complex termination impedance by making Z_{SA} and Z_{SB} complex (as in figure 1). By doing so, the echo cancellation is improved considerably, enabling a higher RX-PGC and increasing the MTPR at the AD converter, relaxing the AD converter resolution requirements.
When using a complex termination impedance scheme, the target should be to make the output impedance equal to the impedance of the line seen through the transformer and LINE capacitors.
The proposed values from figure 1 is set to give the best impedance matching for an AWG 26 cable in the ADSL band and the values used are assumed that the programmable impedance code is set to “10000” (or 25Ω).
When using a complex termination impedance, the value of a programmable impedance is less.

Power modes

[S2 ..S0]		I_{BATqui}*	I_{DDqui}**	Function	Comment
000	76mA	40mA	Power 0	Allowing full transmission in both directions	
001	67mA	36mA	Power 1	Full transmission	
010	58mA	32mA	Power 2	Recommended for high end applications (lines with low noice), Default when reset	
011	49mA	29mA	Power 3	Full transmission	
100	40mA	25mA	Power 4	Good enough for 400kbit/s, 4Mbit/s on 3 km AWG 26 with ETSI noise	
101	31mA	22mA	Power 5	Slight degradation in bitrate	
110	21mA	18mA	Power 6	Only recommended as "sleep mode"	
111	13mA	14mA	Power 7	Tx-path disabled, Rx-path active, Should not be used	

* Standing Current in high voltage part

** Standing Current in low voltage part

In order to save power in sleep mode, the "100" code is recommended : The power consumption is then reduced to 525mW. In this mode, it is still possible to receive a wake-up signal from the CPE.

Terminology

ADDA: Analogue to Digital, Digital to Analogue converter circuit

ADSL: Assymetric Digital Subscriber Line

CO: Central Office

CPE: Customer Premises Equipment

EC: Echo Cancellation

FDM: Frequency Division Multiplex

GBD: Guaranteed by Design

MTPR: Multi-Tone Power Ratio

OTP: Over-Temperature Protection

OVP: Over Voltage Protection

PAR: Peak-to-Average Ratio

PGC: Programmable Gain Control

POTS: Plain Old Telephony System

RX: Receive Direction

SFDR: Spurious Free Dynamic Range

SNR: Signal to Noise Ratio

TBD: To Be Defined

Ordering Information

Package	temp range	part no
32-pin LQFP	0 - 85 °C	PBM 397 05/3LQ

Ericsson Microelectronics
SE-164 81 Kista, Sweden
Telephone: +46 8 757 5000
Internet: www.ericsson.com/microelectronics
For local sales contacts, please refer to our website
or call: Int + 46 8 757 4700, Fax: +46 8 757 4776

Preliminary Data Sheet
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