SSI 32D539
Data Synchronizer & 1, 7 RLL Endec

Advance Information

July, 1990

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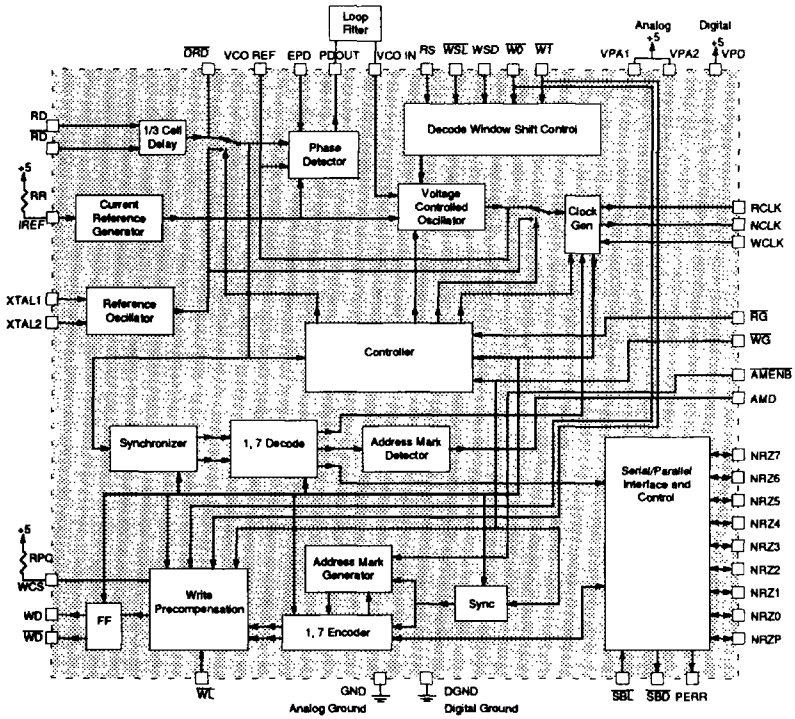
DESCRIPTION

The circuit is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in hard disk drive systems with a +5V supply.

FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **9-bit bi-directional data bus interface**
  - **8 data bits plus 1 parity bit**
  - **Parity generation during read operation**
  - **Parity checking during write operation**
- **Up to 48 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Programmable Sync-Byte pattern detection**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

BLOCK DIAGRAM



OPERATION

DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

RR = (TBD/DR) - TBD kΩ

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D460 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (read mode) selects the $\overline{RD}$ input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets

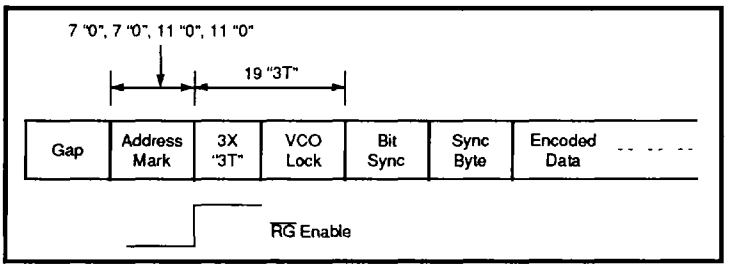


FIGURE 1: Disk Operation Lock Sequence in Read Mode Soft Sector Operation

of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMENB}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 $\overline{RD}$ bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low.

PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts negative transitions of the incoming read data ($\overline{RD}$) looking for 3 consecutive 3T preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the read reference clock. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 negative transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

BYTE SYNC AND NRZ OUT

As the data is decoded, it is compared to a Sync Byte that was loaded prior to the read operation. When a match is found, RCLK and NCLK are resynchronized to the correct byte boundary. NRZ data then appears at the byte output beginning with the sync byte. The $\overline{SBD}$ output is also set low at this time. It remains low until the end of the read operation. A parity bit (NRZP) is also generated for each output byte (even parity).

HARD SECTOR OPERATION

In hard sector operation AMD remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern. In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

Serial NRZ data is clocked into the circuit and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the RRC.

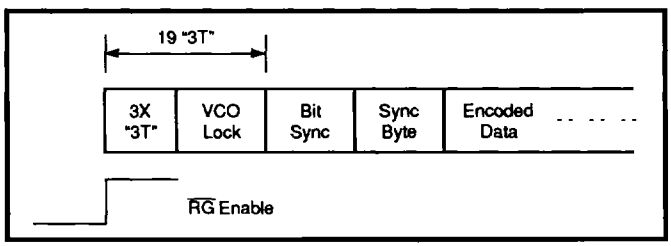


FIGURE 2: Disk Operation Lock Sequence In Read Mode Hard Sector Operation

WRITE MODE (Continued)

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

SOFT SECTOR

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC source switch from $\overline{RD}$ and VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMENB}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ byte. The first non-zero NRZ byte input is assumed to be the sync byte. After a delay of 5 NRZ time periods, non-preamble data begins to toggle out WD. Finally, at the end of the write cycle, 2 bytes of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 2 NRZ time periods after $\overline{WG}$ goes high.

As each NRZ byte is input for encoding, its parity is checked against the parity bit (NRZP). If a parity error is detected the PERR output flag is set high. It remains high until WG goes high.

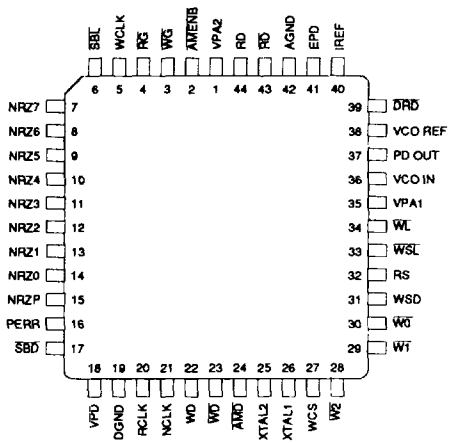
HARD SECTOR

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMENB}$ (address mark enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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