D2684, DECEMBER 1982 – REVISED JUNE 1989

- 8-Bit Serial-In, Parallel-Out Shift
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Shift Register has Direct Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

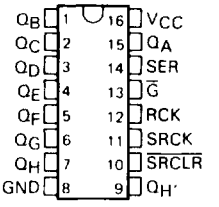
description

These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

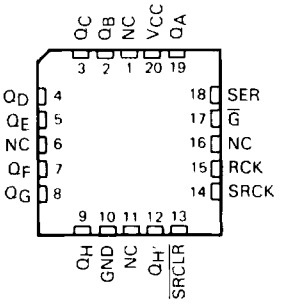
Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

The SN54HC595 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC595 is characterized for operation from −40°C to 85°C.

SN54HC595 . . . J PACKAGE
SN74HC595 . . . D† OR N PACKAGE
(TOP VIEW)



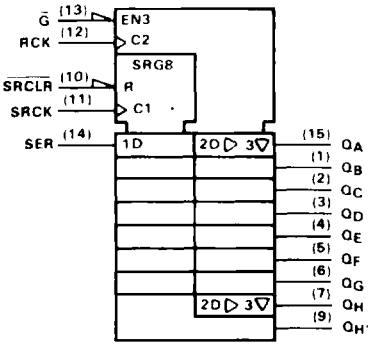
SN54HC595 . . . FK PACKAGE
(TOP VIEW)



NC No internal connection

†Contact the factory for D availability.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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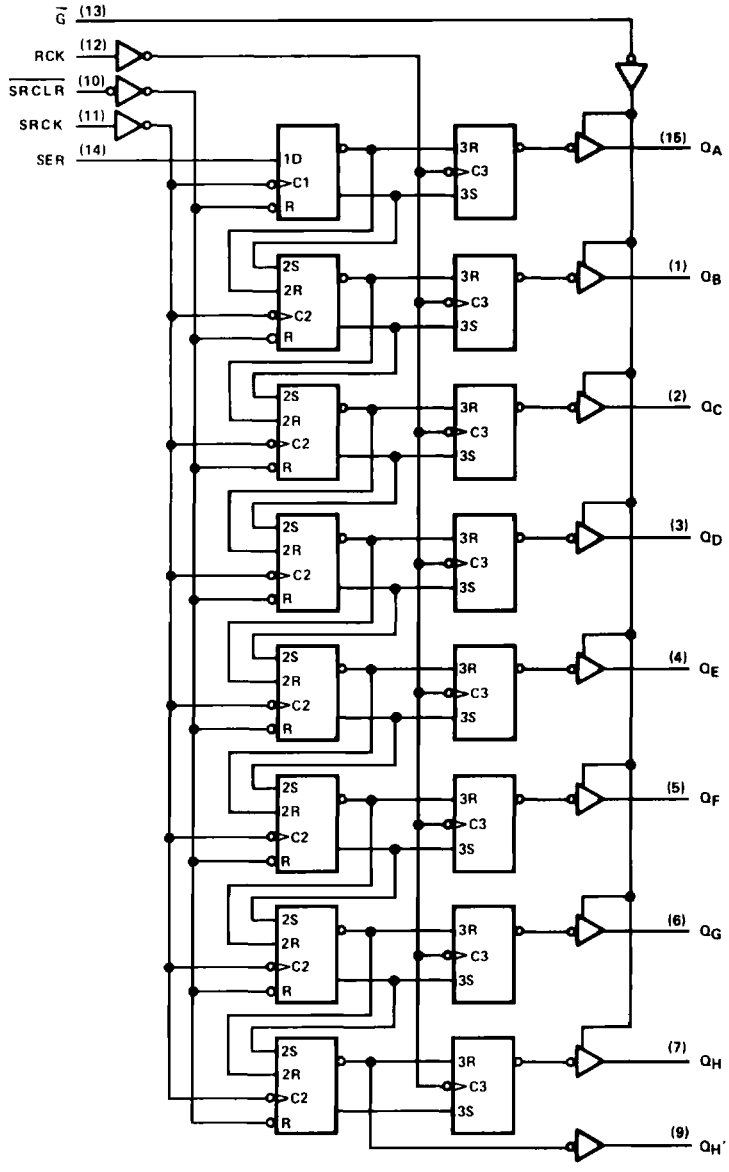
logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC595			SN74HC595			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}	Q_H', I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		Q_A-Q_H, I_{OH} = −6 mA									
	V_I = V_{IH} or V_{IL}	Q_H', I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
		Q_A-Q_H, I_{OH} = −7.8 mA									
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}	Q_H', I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 6 mA									
	V_I = V_{IH} or V_{IL}	Q_H', I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 7.8 mA									
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160		80	μA
C_i			2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC595		SN74HC595		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, SRCK		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	SRCK or RCK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{SRCLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SER before SRCK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		SRCK↑ before RCK↑ (see Note 1)	2 V	75		113		94		ns
			4.5 V	15		23		19		
			6 V	13		19		16		
		$\overline{SRCLR}$ low before RCK↑	2 V	50		75		65		ns
			4.5 V	10		15		13		
			6 V	9		13		11		
		$\overline{SRCLR}$ high (inactive) before SRCK↑	2 V	50		75		60		ns
			4.5 V	10		15		12		
			6 V	9		13		11		
t_h	Hold time	SER after SRCK↑	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

Note 1: This setup time ensures the output register will see stable data from the shift-register outputs. The clocks may be tied together in which case the output register will be one clock pulse behind the shift register.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SRCK	Q_H'	2 V	6	26		4.2		5		MHz
			4.5 V	31	38		21		25		
			6 V	36	42		25		29		
t_{pd}	SRCK	Q_H'	2 V		50	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
t_{pd}	RCK	Q_A to Q_H	2 V		50	150		225		187	ns
			4.5 V		17	30		45		37	
			6 V		14	26		38		32	
t_{PHL}	$\overline{SRCLR}$	Q_H'	2 V		51	175		261		219	ns
			4.5 V		18	35		52		44	
			6 V		15	30		44		37	
t_{en}	$\overline{G}$	Q_A to Q_H	2 V		40	150		225		187	ns
			4.5 V		15	30		45		37	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Q_A to Q_H	2 V		42	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		20	34		51		43	
t_t		Q_A to Q_H	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	
t_t		Q_H'	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	400 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCK	Q_A to Q_H	2 V		60	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t_{en}	$\overline{G}$	Q_A to Q_H	2 V		70	200		298		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q_A to Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.