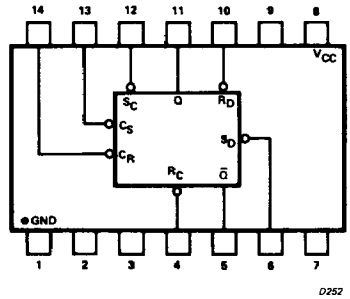
PIN CONFIGURATION



SP629A

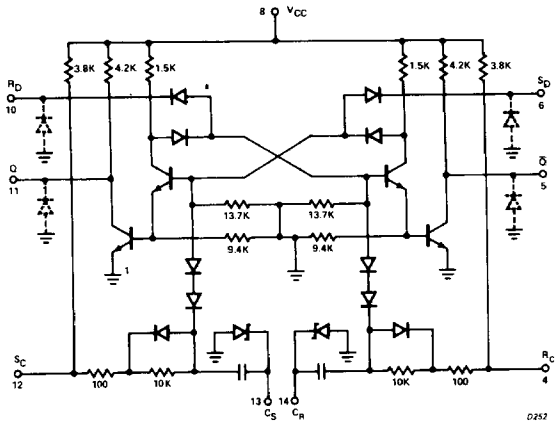
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage					
"1" Level	I_{out} =-200μA, Driven Input	3.8			V
"0" Level	I_{out} = 20mA, Driven Input			0.6	V
	I_{out} = 12.5mA Driven Input			0.4	
Input Current					
input high					
S_D, R_D, clock	V_{in} = 5.0V			25	μA
S_C, R_C	V_{in} = 5.0V			25	μA
input low					
S_D, R_D, S_C, R_C	V_{in} = 0.6V			-2.5	mA
Clock Effective Capacitor			75		pF
Power Supply Current	V_{in} = 5.0V, T_A = 25°C			10	mA
Turn on Delay					
clocked	See Test Figure 1, T_A = 25°C			100	ns
direct	See Test Figure 2, T_A = 25°C			100	ns
Turn off Delay					
clocked	See Test Figure 1, T_A = 25°C			100	ns
direct	See Test Figure 2, T_A = 25°C			100	ns
Fan-out					
–To sink loads (2.5mA/load)				8	
–To source loads (180μA/load)				1	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

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TRUTH TABLES

629A

CLOCK SET/RESET

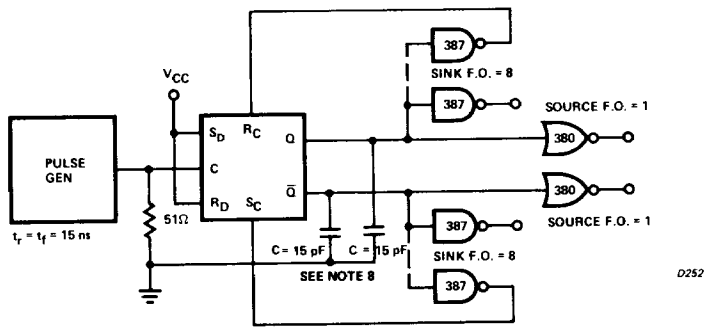
S_C	R_C	Q
0	0	?
0	1	1
1	0	0
1	1	No Change

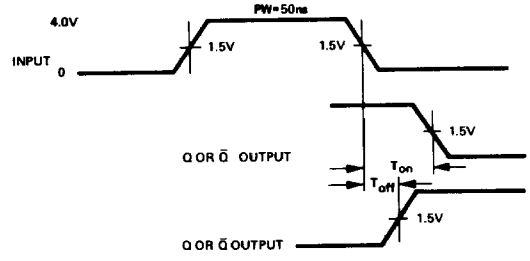
DIRECT SET/RESET

S_D	R_D	Q
0	0	*
0	1	1
1	0	0
1	1	No Change

*Both Q and $\bar{Q}$ remain in "1" state until S_D or R_D rises.

TEST CIRCUIT AND WAVEFORM

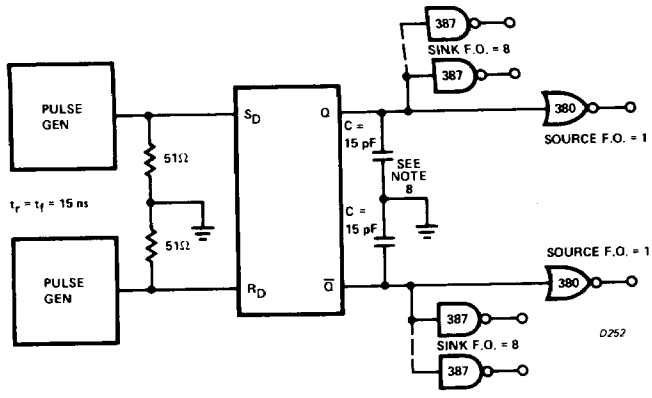


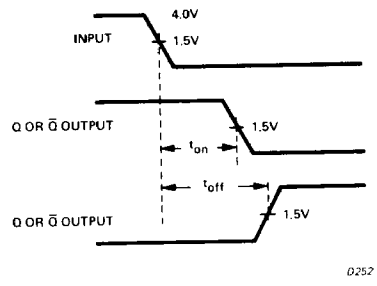


Max. clock fall time = 75ns

Figure 1

TEST CIRCUIT AND WAVEFORM





Max. clock fall time = 75ns

Figure 2