FAIRCHILD
A Schlumberger Company

F100117
Triple 2-Wide OA/OAI Gate

F100K ECL Product

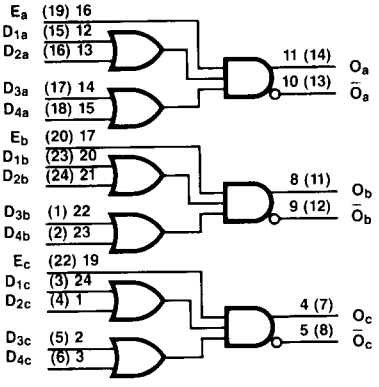
Description

The F100117 is a monolithic triple 2-wide OR/AND gate with true and complement outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_{na} - D_{nc}	Data Inputs
E_a - E_c	Enable Inputs
O_a - O_c	Data Outputs
$\overline{O}_a$ - $\overline{O}_c$	Complementary Data Outputs

Logic Symbol



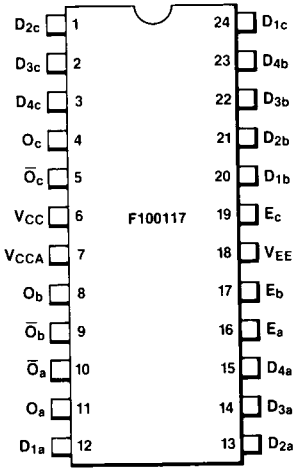
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information

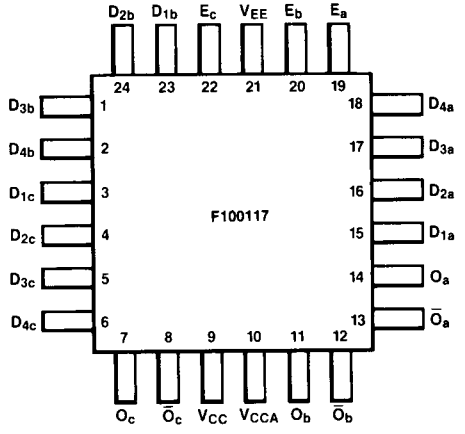
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			260	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−79	−54	−37	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

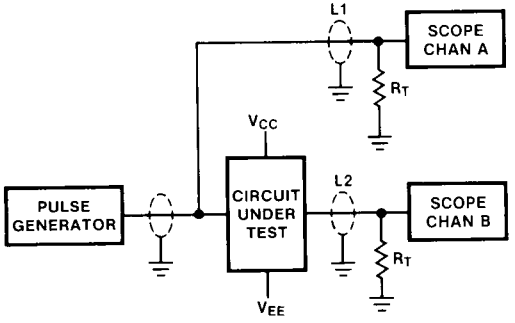
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.60	0.90	2.50	0.90	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.40	0.90	2.30	0.90	2.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.20	0.45	1.10	0.45	1.20	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.20	ns	

*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance < 3 pF

Fig. 2 Propagation Delay and Transition Times