1.25Gbps Fiber-Optic Pre-Amplifier

GENERAL DESCRIPTION

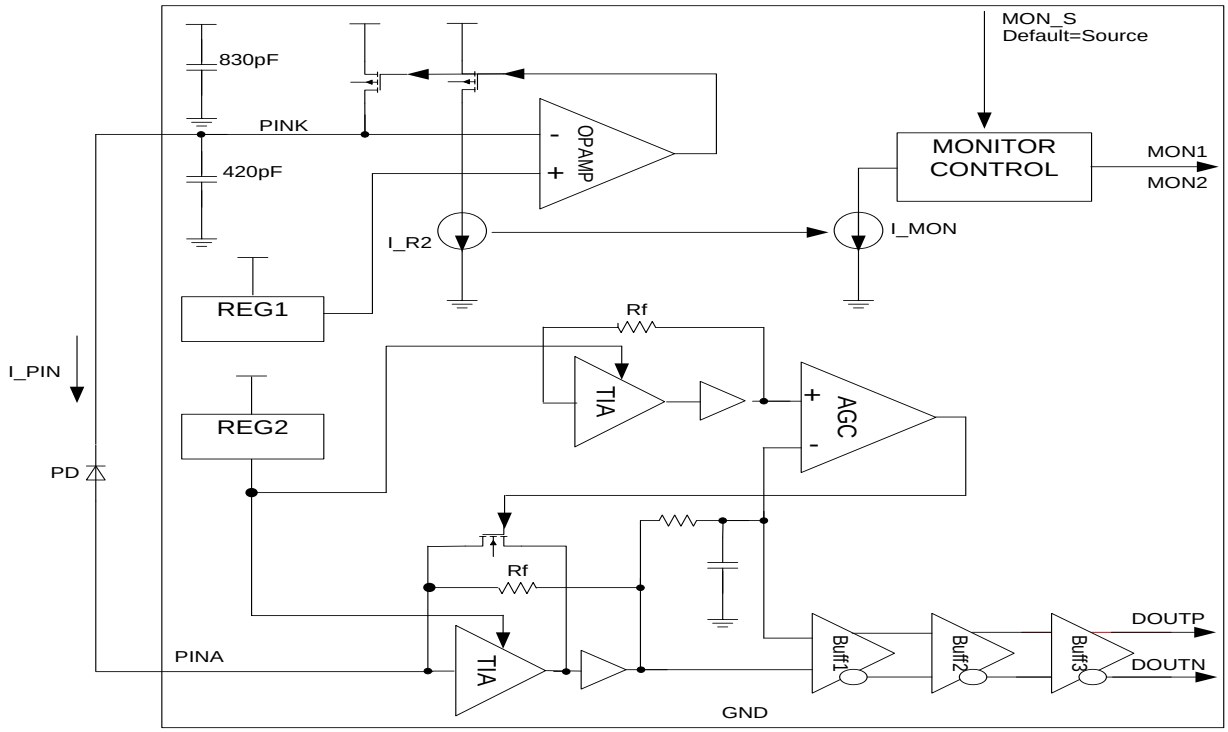
CS6720 is a low noise trans-impedance amplifier designed for 1.25Gbps fiber optical applications. In typical applications, it is connected to a PIN type photo diode or avalanche photodiode, and amplifies the photo current into a differential voltage output. CS6720 uses advanced CMOS process and achieves typical input sensitivity of -32dBm. And with AGC control, the typical overload limit is at +3dBm.CS6720 uses AGC circuits that minimize the input circuit components to achieve lower noise and higher sensitivity. CS6720 also includes on-chip decoupling capacitors for both PINK and VCC that can reduce TO assembly configurations. There is also monitor output that mirrors the photo diode current. and the output can be selectable

FEATURES

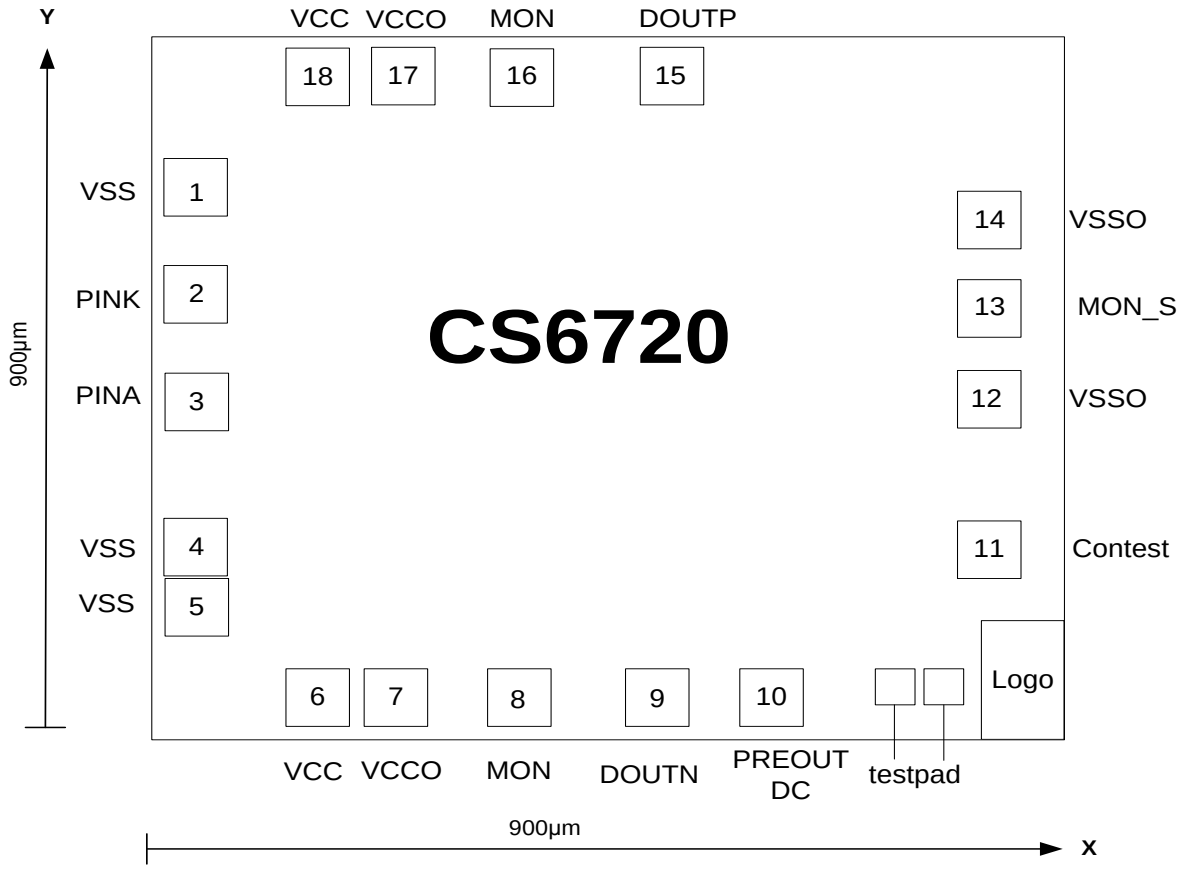
- 3.3V operation
- 30K-Ohm differential trans-impedance gain
- 1000MHz bandwidth
- -30dBm optical sensitivity
- +3dBm overload
- Current monitor output Sink/Source
- On-chip PINK (220pF) and VCC (400pF) decoupling capacitor
- Available as dice

APPLICATIONS

- Fiber Channel
- OC48/STM16
- SDH/SONET
- Gigabit Ethernet

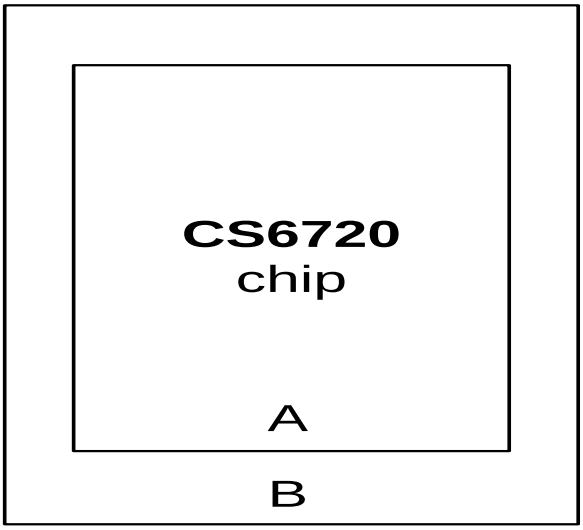


1 PAD CONNECTION DIAGRAM



DIE DIAGRAM

2 DIE SIZE



Area A: Total chip size in 1000um*1000um including seal ring.

Area B: Scribe line residue after die saw, X=17.5±2.5 um per side

Actual size after die-saw: Max: 1020*1020um, Min: 980*980um

Chip Thickness: 12mil±1mil

3 PAD LOCATION COORDINATE

Pad Number	Pad Name	X (μm)	Y (μm)
1	VSS	63	763.5
2	PINK	63	630.3.
3	PINA	67.16	493.8
4	VSS	63	364.9
5	VSS	63	264.9
6	VCC	209.6	63
7	VCCO	309.6	63
8	MON	441.1	63
9	DOUTN	569.3	63
10	PREOUTDC	761.6	63
11	CONTEST	938	206.2
12	VSSO	938	483.2
13	MON_S	938	617.3
14	VSSO	938	750.5
15	DOUTP	569.3	937
16	MON	441.1	937
17	VCCO	309.6	937
18	VCC	209.6	937

Note1: The coordinates start from the left bottom of the die to the center of the pad.

Note2: All GND pad should be bonded to VSS together for best performance.

Note3: NO need extra off-chip capacitance for PINK.

4 PAD DESCRIPTION

Name	Pin	Description
VSSO VSS	1, 4, 5,12,14	Ground pin. Connect to most negative supply voltage.
DOUTP	15	Data output pin. This pin goes high when current flows into pin PINA.
VCC VCCO	6, 7, 17, 18	Power pin. Connect to most positive supply voltage.
MON	8,16	Received Signal Strength Indicator. Sinks or sources current equal to PD current.
PINK	2	PIN Cathode bias pin. Connect to the cathode of the photodiode. Connect an external capacitor between this pin and ground.
PINA	3	PIN Anode pin. Connect to the anode of the photodiode.
DOUTN	9	Inverting data output pin. Complementary to pin DOUTP.
MON_S	13	Selects whether MON output is a current sink or source. This pin has internal pull-up resistor. Leave this pin floating will configure MON output as a current source, connecting this pin to ground configures MON output as current sink.
PREOUTDC	10	Front-end TIA output DC for testing
CONTEST	11	AGC control voltage for testing

Note: PINA is an ESD sensitive pin should be handled with care.

5 FUNCTIONAL DESCRIPTION

CS6720 is a trans-impedance pre-amplifier fabricated by CMOS process. The CS6720 consists of a trans-impedance amplifier, an output buffer, two voltage regulators, an AGC block and a monitor block.

5.1 Voltage Regulator and PINK bias

Two on-chip regulators are used to provide a clean supply voltage to the front-end amplifier. There is also an on-chip PINK decoupling capacitor of 220pF, therefore external decoupling capacitor for PINK can be omitted.

5.2 Low Noise Trans-Impedance Amplifier

The first stage of CS6720 is a low-noise trans-impedance amplifier. The input current is fed into an inverting amplifier with a variable feedback resistor. The feedback resistor converts the input photo current to voltage at the output node. The feedback resistance is reduced by AGC control when the input is large. The typical input referred noise current (integrated to 1000MHz) is 80nA when AGC is not turned-on.

5.3 AGC Block

The AGC control block receive the information of the input photo-diode current level then set the trans-impedance gain accordingly. The higher the input current, the lower the gain is set to prevent the overload saturation of the first stage amplifier. The AGC defines variable trans-impedance gain according to the input current as shown in Figure-1. The input power is calculated from 0.9A/W photo-diode conversion efficiency. Typically, for low power input, the differential trans-impedance gain is set to 30KOhm. At -22dBm, the AGC function turned on, and the trans-impedance is reduced as the input power is increased. With AGC reducing the trans-impedance gain, CS6720 can have up to +3dBm input without overloading the front-end amplifier.

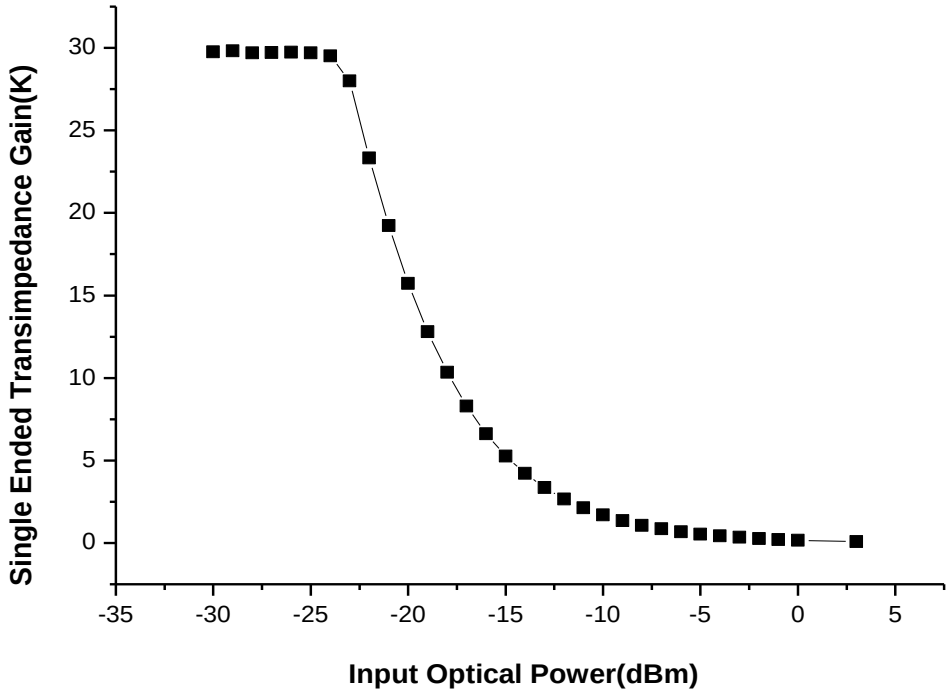


Figure-1 TIA Gain versus Input Power

5.4 Output Buffer

The single-ended output of trans-impedance amplifier is converted to differential signal through output buffer stage (Figure-2). The conversion is accomplished through the extraction of the DC average level by a RC low pass filter shown in the figure. This low-pass filter 3dB frequency is set at 50KHz.The output buffer has internal pull down current sources and is able to drive 100Ohm load.The output should be AC coupled to the post-amplifier input, and termination resistors be placed after the coupling capacitor. Please note the external AC coupling capacitor and the external termination resistor also set another 3dB lower frequency.

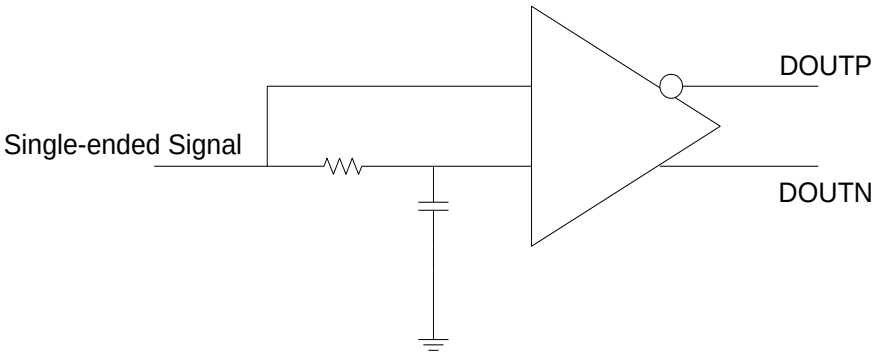


Figure-2 Single-ended to Differential Signal conversion

Because the AGC effects described above, the output amplitude is limited when the input power is higher than the AGC setting. The typical output amplitude of CS6720 is shown in Figure-3.

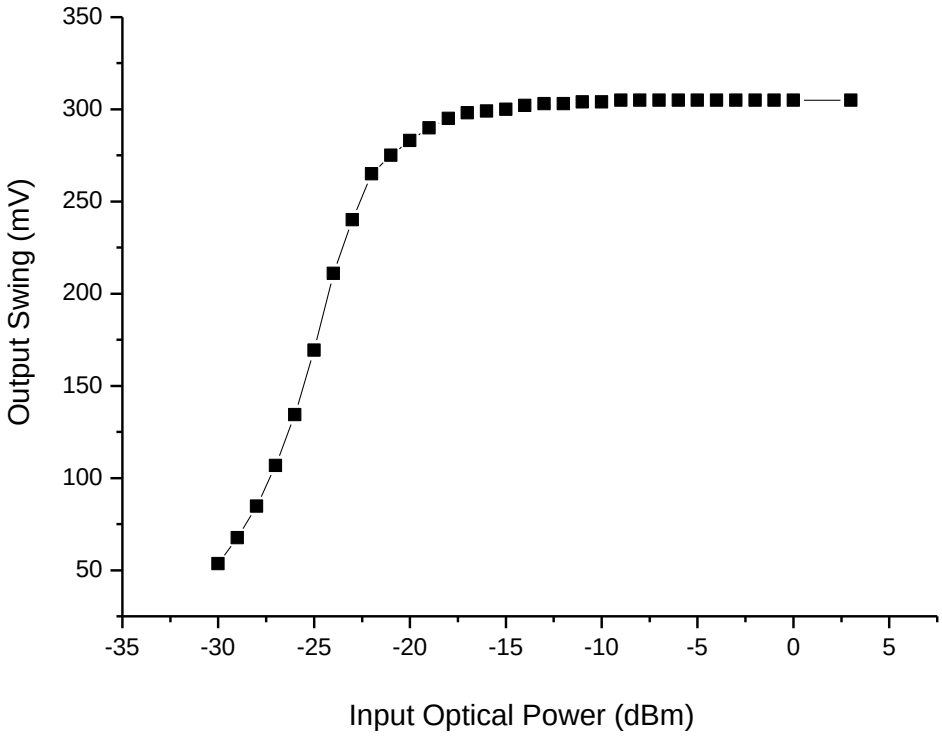


Figure-3 Differential Output Swing versus Input Power

(Ta=25ºC, C_{PD}=0.4pF, data is collected by differential output with 50ohm termination).

5.5 Monitor Block

The MON output provides a copy of the photodiode mean input current. The MON output can be configured as either a current sink or a current source to suit the application requirement. By connecting a resistor between the MON output and either VCC (+3.3 V) or ground (GND) a voltage proportional to the photodiode current can be generated. If MON_S is left open the MON output is configured as a current source. In this case, the resistor R_{MON} should be terminated to ground to develop a ground referenced voltage across it directly proportional to the photodiode mean current. If MON_S is tied to ground, the MON output is configured as a current sink and the resistor R_{MON} should be connected to VCC (+3.3V). The typical the input optical power to the MON output current of CS6720 is shown in Figure-4.

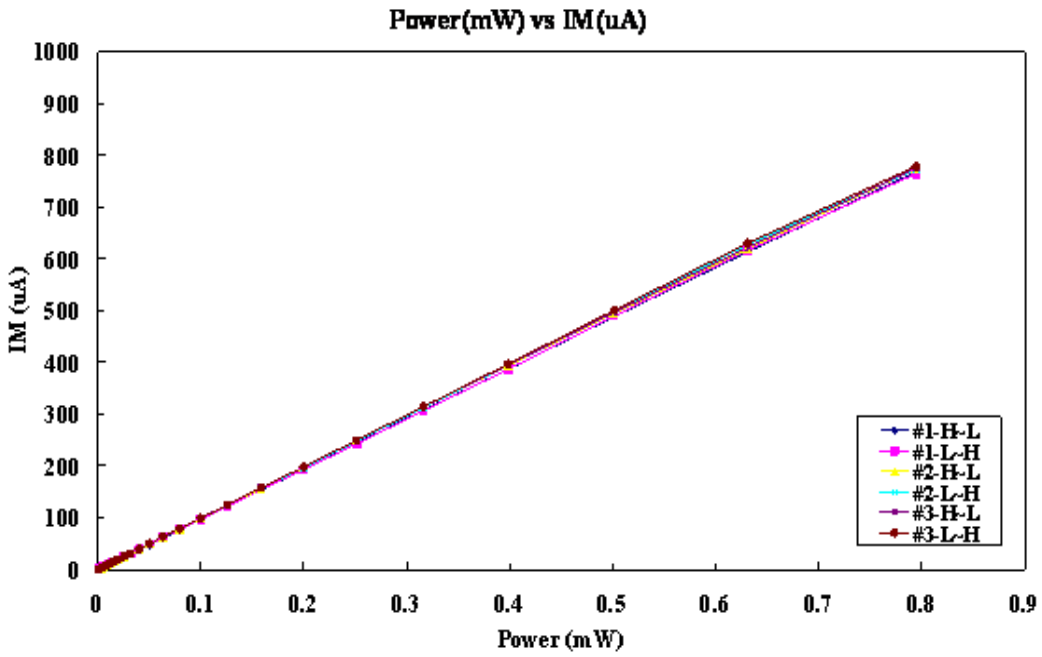


Figure-4 Monitor current versus Input Power

6 ELECTRICAL CHARATERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VCC	Power Supply (VCC - GND)	5	V
T storage	Storage Temperature	-65 to +150	°C

6.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
VCC	Power Supply (VCC - GND)	3.0-3.6	V
TA	Operating Ambient	-40 to 85	°C

6.3 AC/DC ELECTRICAL CHARACTERISTICS

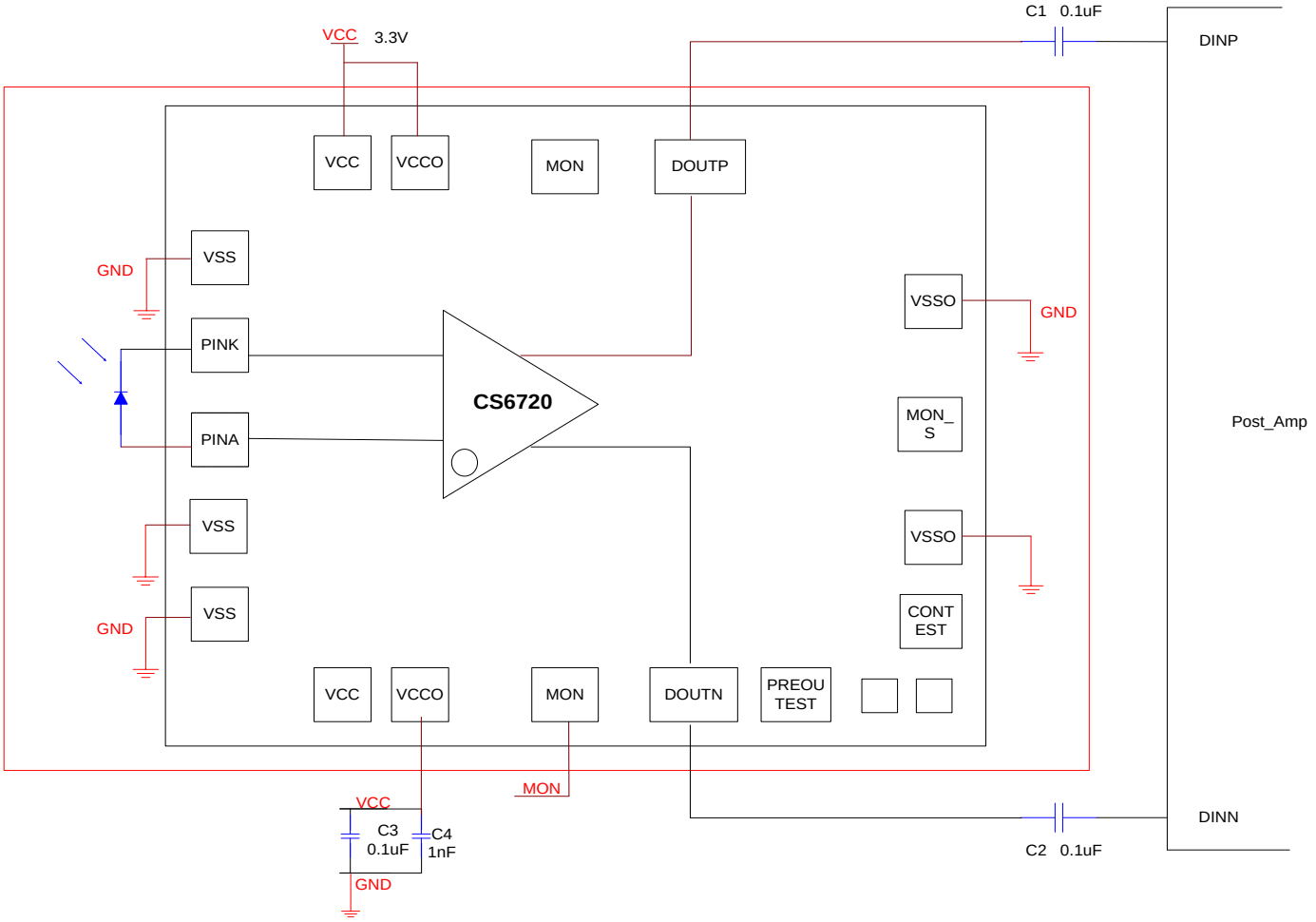
Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VIN	Input bias voltage		0.5	0.6	0.7	V
I_{CC}	Supply current		-	30		mA
RO	Output impedance	Single ended	-	50	-	Ohm
G	Small signal trans-impedance Input = $2uA_{P-P}$(Note 1)	Differential (R_L = 100 differential)	-	30K	-	
IAC,MAX	Maximum AC input current		2	-	-	mA p-p
IDC,MAX	Maximum DC input current		1	-	-	mA
VDF	Maximum differential output voltage	I input = $1mA_{P-P}$, (R_L = 100,differential)	-	300	-	mV
BW	Small signal bandwidth	C_{PD} = 0.4pF (Note 2)		1000	-	MHz
BWL	Cutoff frequency	-3dB	-	50	100	KHz
IN	Input referred RMS noise	C_{PD} = 0.4pF	-	80	-	nA
Sensitivity	Optical sensitivity	(Note 1)	-	-32	-	dBm
PIN(max)	Optical saturation	(Note 1)	-	+3	-	dBm

PSRR	Power supply rejection ratio	F < 4MHz (Note 2)	30	-	-	dB

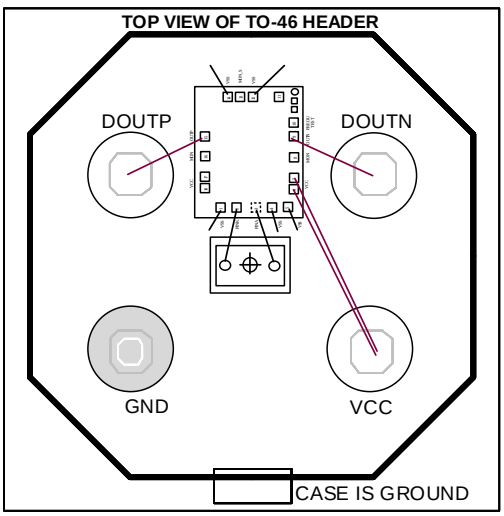
Note1: Assuming photodiode of 0.9A/W conversion, extinction ration of 10 dB and BER of 10^{-10}, C_{PD}=0.4pF

Note2: The result is guaranteed by design simulation.

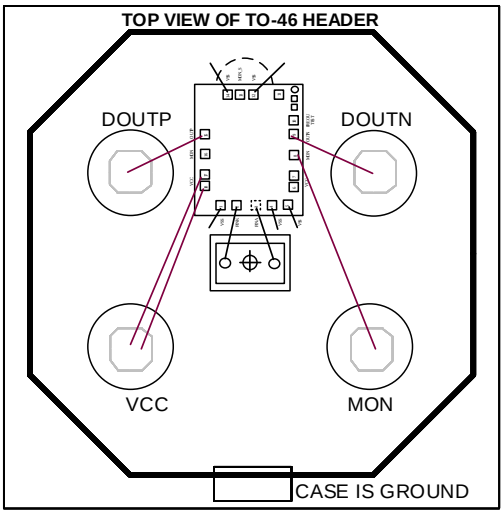
7 TYPICAL APPLICATION



Typical Application Circuit



Typical 4-pin Assembly Circuit



Typical 5-pin Assembly Circuit Using PIN

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