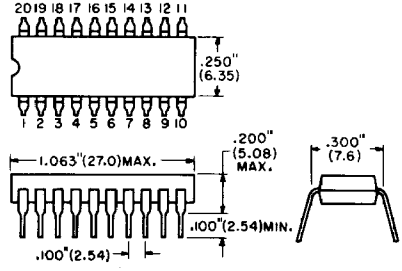
ECG® Semiconductors

ECG2053

8-Bit MPU Compatible Analog to Digital Converter

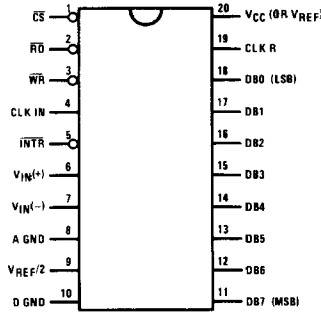


Features

- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet TTL voltage level specifications
- Works with 2.5 V ECG952 voltage reference
- On-chip clock generator
- 0 V to 5 V analog input voltage range with single 5 V supply
- No zero adjust required

Key Specifications

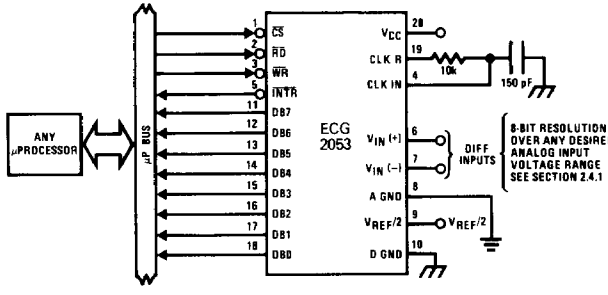
- Resolution — 8 Bits
- Total Error — ±1/2 LSB
- Conversion Time — 100 μs
- Access Time — 135 ns
- Single Supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference



The ECG2053 is a CMOS, 8-bit, successive approximation A/D converter which uses a modified potentiometric ladder—similar to the 256R products. It is designed to meet the ECG8080A standard to allow operation with the ECG8080A control bus, and the output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Typical Application



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5 V
Voltage at Any Input	-0.3 V to (V_{CC} $+0.3$ V)
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$	875 mW

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$ $0°C \leq T_A \leq 70°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.3 V_{DC}

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.

Electrical Characteristics

Converter Specifications:

$V_{CC} = 5$ V_{DC}, $V_{REF}/2 = 2.500$ V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640$ kHz unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC0801:					
Total Adjusted Error (Note 8)	With Full-Scale Adj.			±1/2	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	$V_{CC} = 5$ V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±1/8	LSB

Electrical Characteristics

Timing Specifications: $V_{CC} = 5$ V_{DC} and $T_A = 25°C$ unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	$V_{CC} = 6$V, (Note 5)	100	640	1280	kHz
		$V_{CC} = 5$V	100	640	800	kHz
T_C	Conversion Time	(Note 6)	66		73	$1/f_{CLK}$
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS} = 0$ V_{DC}, $f_{CLK} = 640$ kHz			8770	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS} = 0$ V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1H}, t_{0H}	3-State Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L = 10$ pF, $R_L = 10$k (See 3-State Test Circuits		125	250	ns
t_{WI}	Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	3-State Output Capacitance (Data Buffers)			5	7.5	pF

Electrical Characteristics

Digital Levels and DC Specifications:
$V_{CC}=5\ V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS (Note: CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
$V_{IN}(1)$	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
$V_{IN}(0)$	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
V_{T+}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
$I_{IN}(1)$	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
$I_{IN}(0)$	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK} = 640 kHz, T_A = 25°C and $\overline{CS}$ = "1"		1.3	2.5	mA
DATA OUTPUTS AND $\overline{INTR}$						
$V_{OUT}(0)$	Logical "0" Output Voltage	I_O = 1.6 mA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	I_O = −360 μA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
I_{OUT}	3-State Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
	Output Short Circuit Current	T_A = 25°C				
I_{SOURCE}		V_{OUT} Short to Gnd	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}	9.0	16		mA_{DC}

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5 V), as high level analog inputs (5 V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With V_{CC} = 6 V, the digital logic interfaces are no longer TTL compatible.

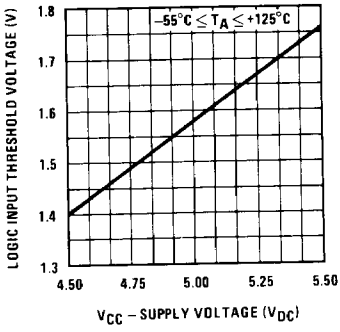
Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

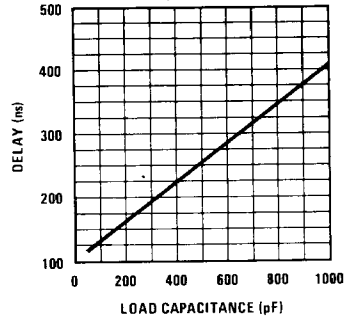
Note 8: None of these A/Ds requires a zero adjust. However, if an all zero code is desired for an analog input other than 0.0 V, or if a narrow full-scale span exists (for example: 0.5 V to 4.0 V full-scale) the $V_{IN}(-)$ input can be adjusted to achieve this.

Typical Performance Characteristics

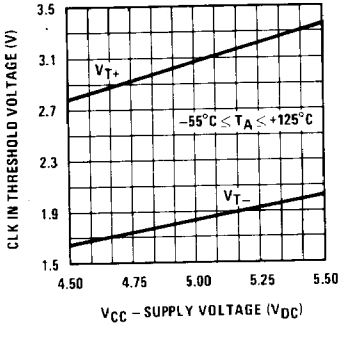
Logic Input Threshold Voltage vs. Supply Voltage



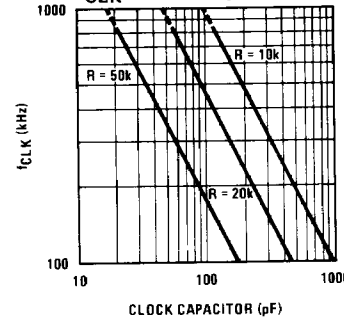
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



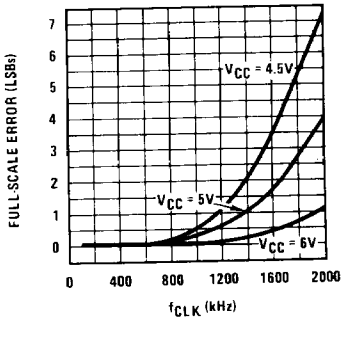
CLK IN Schmitt Trip Levels vs. Supply Voltage



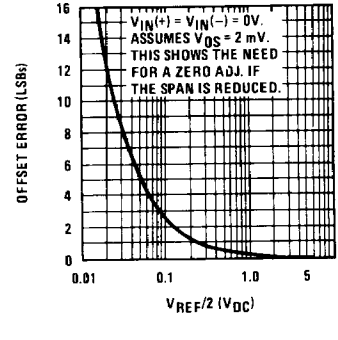
f_{CLK} vs. Clock Capacitor



Full-Scale Error vs f_{CLK}



Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



FUNCTIONAL DESCRIPTION

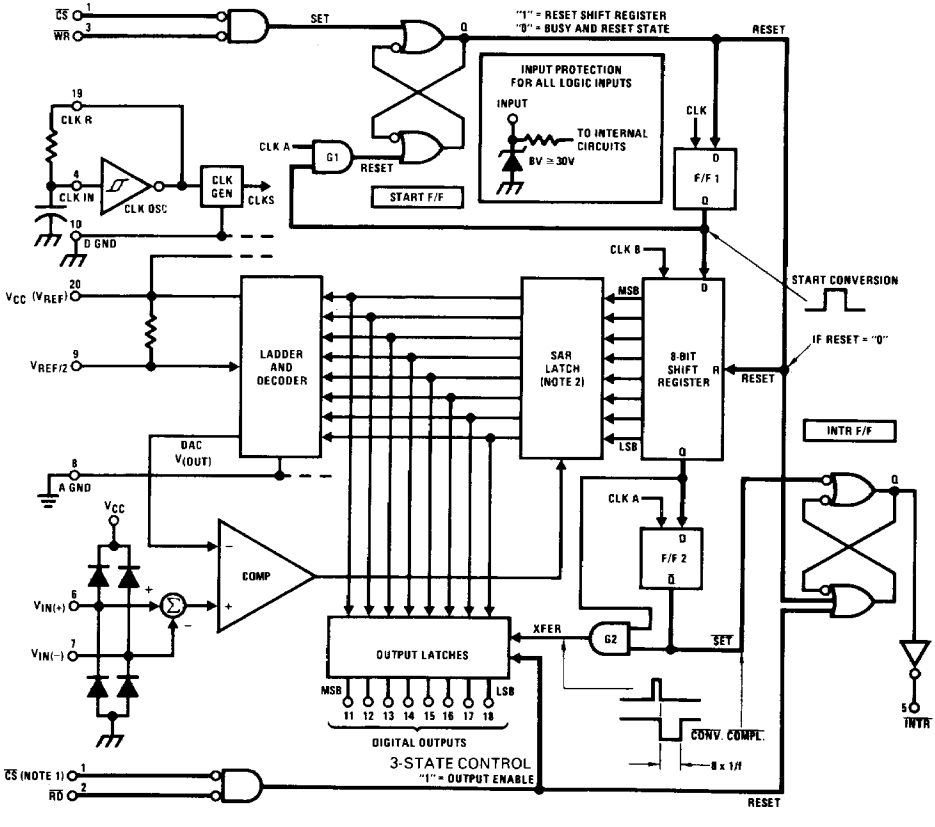
The ECG2053 contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To insure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in Figure 1. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Figure 1. ECG2053 Block Diagram



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D flop, F/F 2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When F/F 2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard TTL logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (Vp)\,(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

Vp is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, Vp, which is given by:

$$Vp = \frac{[\Delta V_{e(MAX)}\,(f_{CLK})]}{(2\pi f_{cm})\,(4.5)}$$

or

$$Vp = \frac{(5 \times 10^{-3})\,(640 \times 10^{3})}{(6.28)\,(60)\,(4.5)}$$

which gives

$$Vp \cong 1.9V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see section 2.4 Reference Voltage Flexibility).

2.3 Analog Inputs

2.3.1 Input Current

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground. The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\lesssim$ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\lesssim$ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.3). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure* 2.

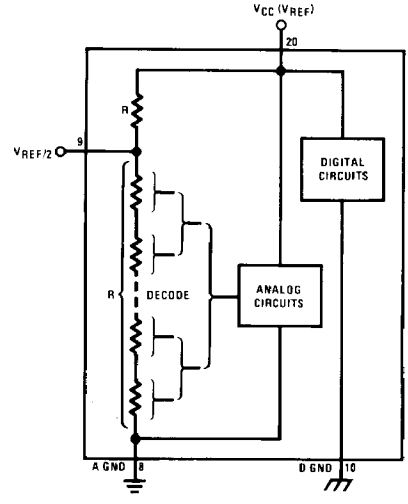
Notice that the reference voltage for the IC is either 1/2 of the voltage which is applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the $V_{REF}/2$ voltage.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V. With 0.5 V_{DC} applied to the V_{IN} (−) pin to absorb the offset, the reference voltage can be made equal to 1/2 of the 3V span or 1.5 V_{DC}. The A/D now will encode the V_{IN} (+) signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input

Figure 2. The $V_{REFERENCE}$ Design on the IC



voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The ECG952 2.5 V IC reference diode is available which operates with a 5 V input voltage and has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$.

2.5 Errors

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D V_{IN} (−) input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V (−) input and applying a small magnitude positive voltage to the V (+)

input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1-1/2 LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the V_{IN} (−) input of the A/D and applying a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+)\ fs\ adj = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right]$$

where:

V_{MAX} = The high end of the analog input range

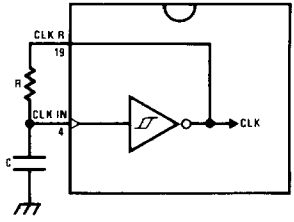
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure* 3.

Figure 3. Self-Clocking the ECG2053



$$f_{CLK} \simeq \frac{1}{1.1\ RC}$$

$R \geq 10\ k\Omega$

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to insure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in the high impedance 3-state mode. Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (ECG8080A) or using clock extending circuits (ECG6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended such as the ECG74LS240) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate ECG977, TO-92, 5 V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with the ECG8080A and ECG6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored at location 0200 to 020F. All Data and Addresses will be given in hexadecimal form. Hardware details are provided separately for each type of microprocessor.

4.1 Interfacing the ECG8080A Microprocessor

This converter has been designed to directly interface with an ECG8080A. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O}$ $\overline{R}$ and $\overline{I/O}$ $\overline{W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in Figure 4.

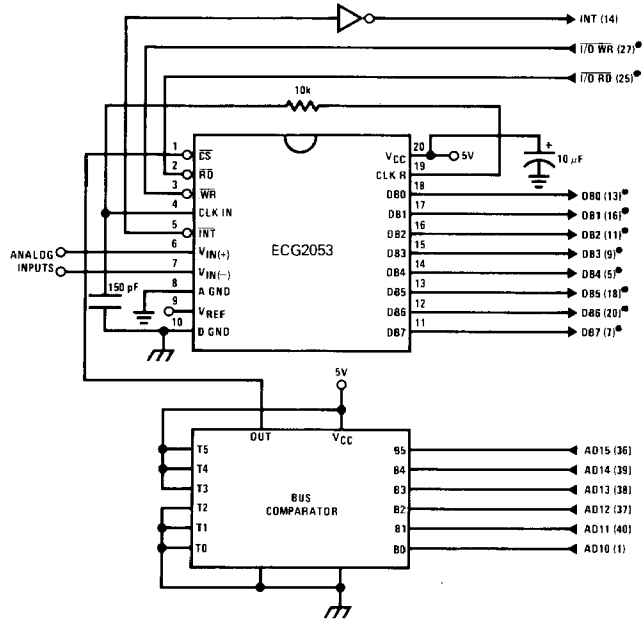
The standard control bus signals of the ECG8080A ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample ECG8080A CPU Interfacing Circuitry

The following hardware may be used to input data from the converter to the ECG8080A CPU chip set (comprised of the ECG8080A microprocessor, the ECG8228 system controller and the ECG8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bidirectional port located at an arbitrarily chosen port address, E0. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs--one for each I/O device.

Figure 4. ECG2053 to ECG8080A CPU Interface



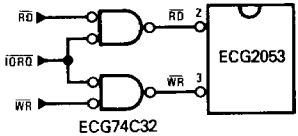
Note 1: • Pin numbers for the ECG8228 system controller, others are ECG8080A.

Note 2: Pin 23 of the ECG8228 must be tied to +12 V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

4.2 Interfacing the ECG3880

The ECG3880 control bus is slightly different from that of the ECG8080A. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent ECG8080A signals. An advantage of operating the A/D in I/O space with the ECG3880 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 5.

Figure 5. Mapping the A/D as an I/O Device for Use with the ECG3880 CPU



ECG74C32

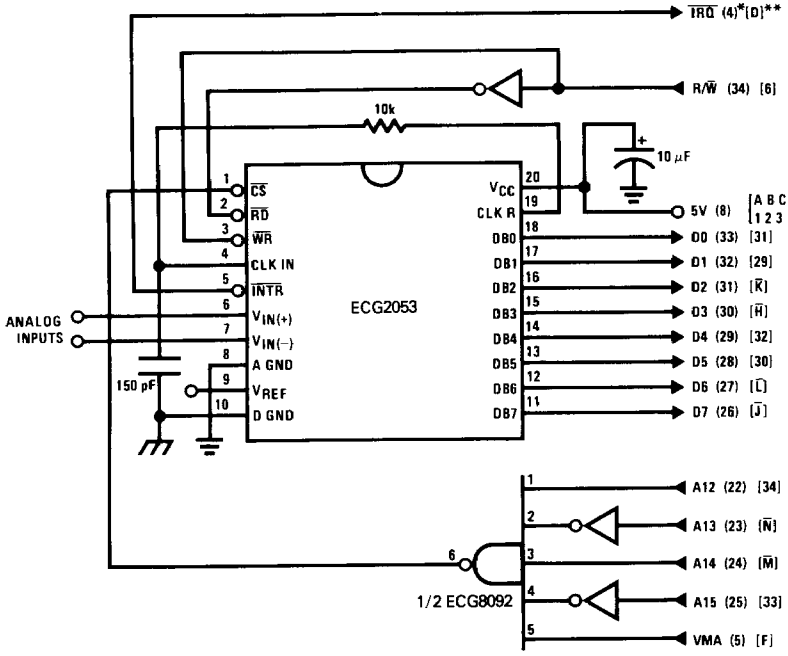
Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing the ECG6502, 6800, 6802 and 6809 Microprocessors

The control bus for these microprocessors does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the Ø2 clock. All I/O devices are memory mapped in the system, and a special signal, VMA, indicates that the current address is valid. Figure 6 shows an interface schematic where the A/D is memory mapped in the system. For simplicity, the $\overline{CS}$ decoding is shown using 1/2 ECG8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 7 the ECG2053 is interfaced to the microprocessor through (the arbitrarily chosen) Port B of the ECG6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

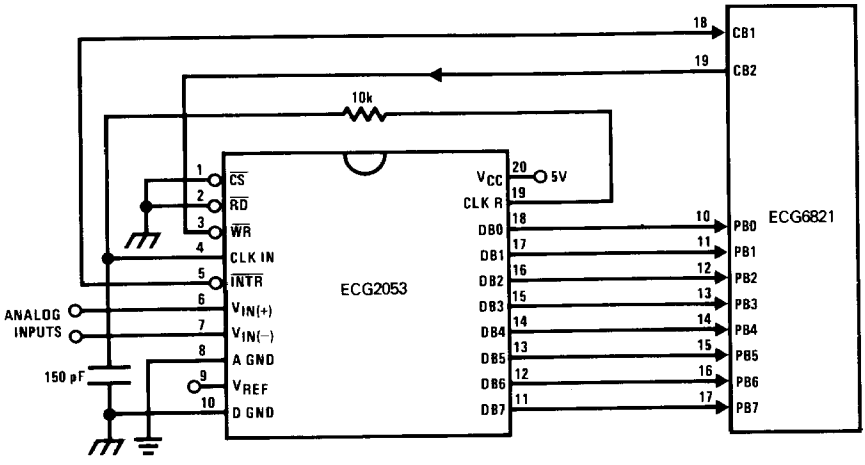
Figure 6. ECG2053 to ECG6800 CPU Interface



Note 1: Numbers in parentheses refer to ECG6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard ECG6800 system common bus code.

Figure 7. ECG2053 to ECG6821 PIA Interface



5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor which is desired.

5.1 Multiple ECG2053 to ECG6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ECG2053, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in Figure 8.

The following schematic may be used to interface (up to) 8 ECG2053s directly to the ECG6800 CPU. This scheme can easily be extended to allow the interface of more converters. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

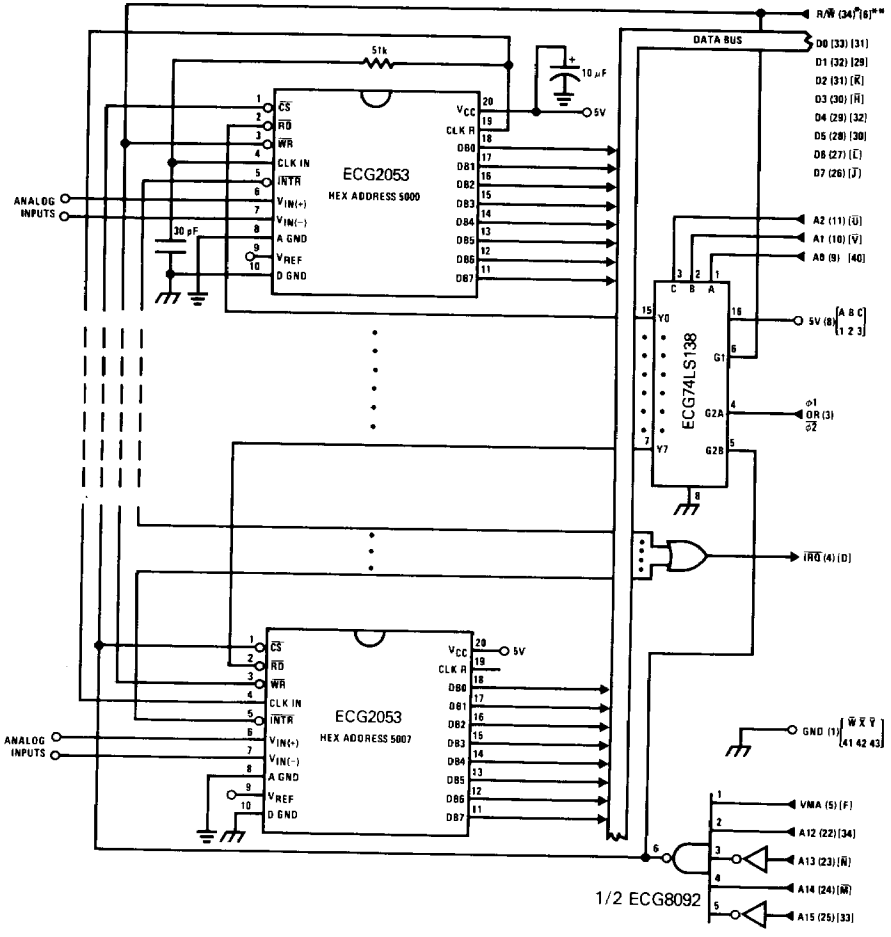
The differential inputs of the ECG2053 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ECG2053 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. Figure 9 is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the ECG8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for 1/4 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} + \underbrace{(V_{os2} - V_{os1} - V_{os3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{os1} + V_{os3} - V_{os2}$. This is the principle of this auto-zeroing scheme.

Figure 8. Interfacing Multiple A/Ds in a ECG6800 System



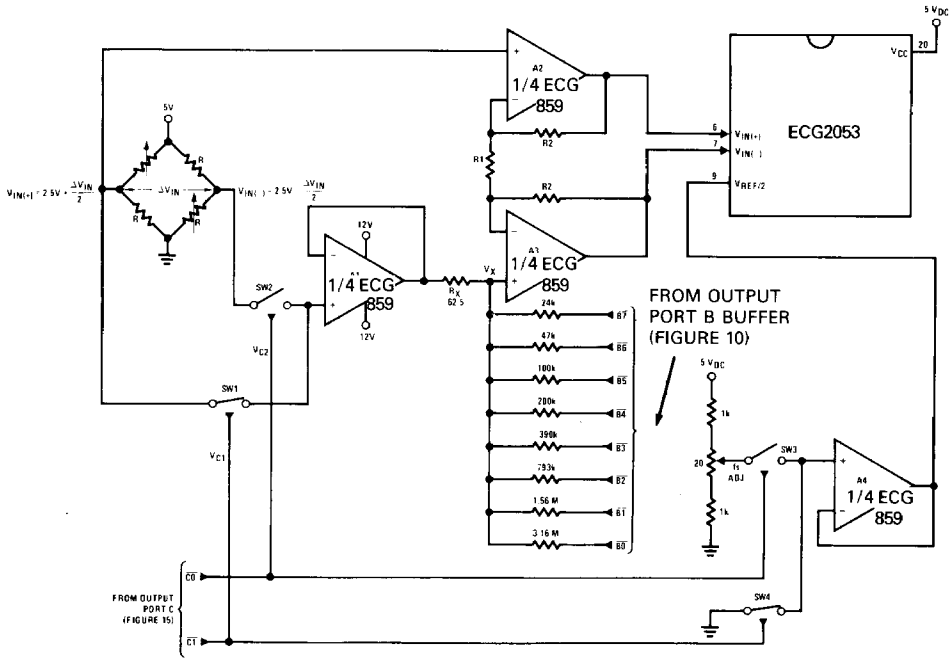
Note 1: Numbers in parentheses refer to ECG6800 CPU pin out.

Note 2: Numbers or letters in brackets refer to standard ECG6800 system common bus code.

The ECG8080A uses the 3 I/O ports of an ECG8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ECG2053 as shown in Figure 10. The PPI is programmed for basic IO operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the ECG8080A and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by insuring that the voltage at the output of A1 is approximately 2.5 V so that a logic "1" (5 V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0 V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ± 12 mV with a resolution of 50 µV which will null the offset error term to 1/4 LSB of full-scale for the ECG2053. It is important that the voltage levels which drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0 V to 5 V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5 V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Figure 9. Gain of 100 Differential Transducer Preamp

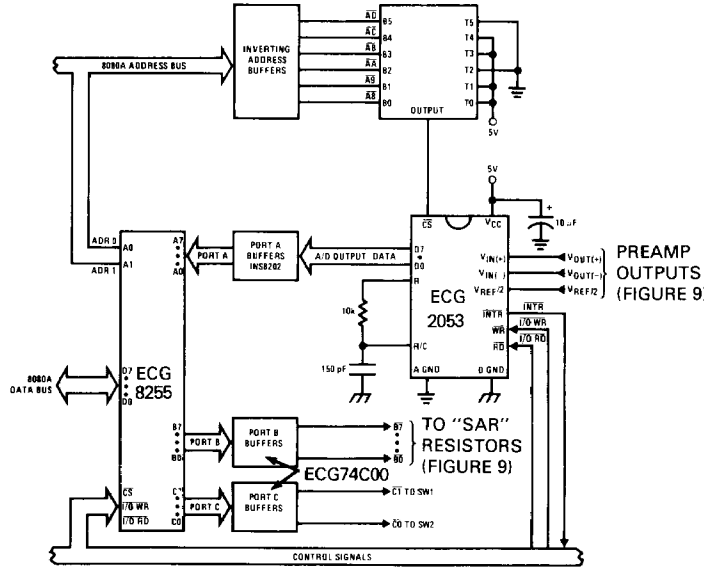


Note 1: R2 = 49.5 R1.

Note 2: Switches are ECG4066B CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

Figure 10. Microprocessor Interface Circuitry for Differential Preamp



It must be noted that the ECG2053 will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

5.3 Multiple A/D Converters in a ECG3880 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. Figure 11 and the appropriate software is a method of determining which of 7 ECG2053 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the ECG74LS373, 8-bit D type flip-flop. When the CPU acknowledges the interrupt, the program is vectored to a data input subroutine. This subroutine will read a peripheral status word from the ECG74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1).

2) The address bus from the CPU and the data bus to the CPU are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at an arbitrarily chosen address.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

Hex Port Address	Peripheral
00	8-Bit Flip-Flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

Figure 11. Multiple A/D's with ECG3880 Microprocessor

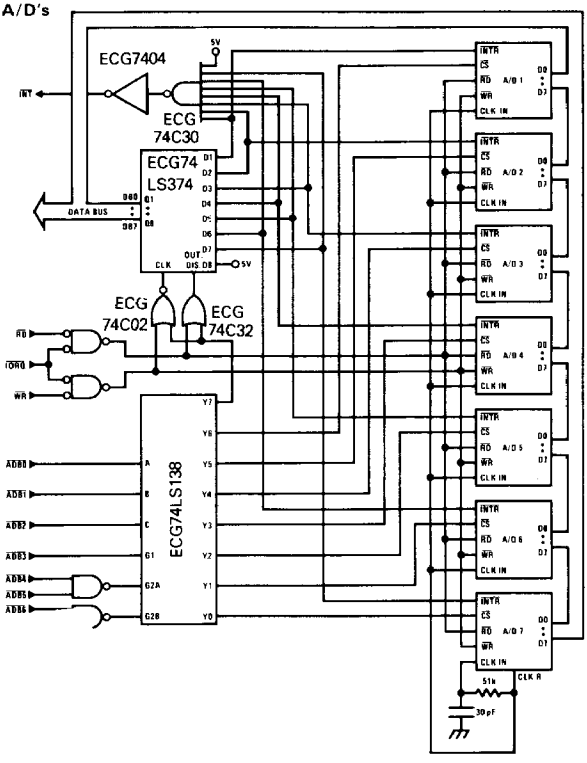


Figure 12. Offsetting the Zero of the ECG2053 and Performing an Input Range (Span) Adjustment

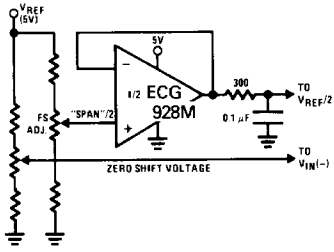


Figure 13. Handling ±5 V Analog Input Range

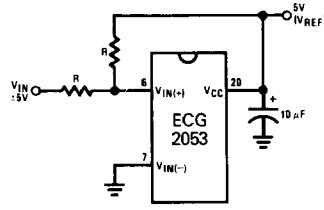


Figure 14. Handling ±10 V Analog Input Range

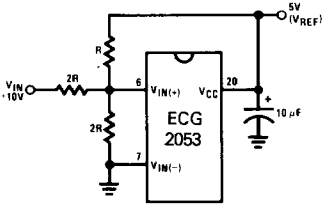
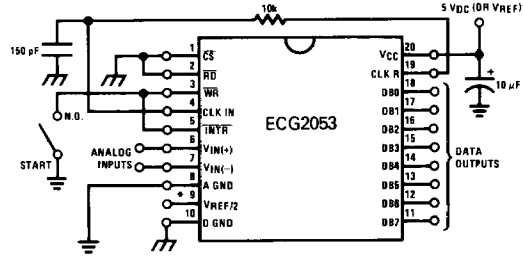


Figure 15. Free Running Connection



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