



# Self-Timed Pipelined Static RAM

2  
SRAMS

### Features

- 64K x 4
- Separate I/O
- Fully registered
  - Address
  - Data in
  - Data out
  - CE, WE
- Asynchronous output enable
- Self-timed write
- Transparent write and write pass-through features
- 167-MHz operation
  - 2 ns set-up time
  - 6 ns cycle time
  - 5 ns clock to output
- 44-pin package
  - PLCC, SOJ
- TTL-compatible inputs and outputs

### Functional Description

The CY7B158 is a fully registered (pipelined) high-performance BiCMOS static

RAM organized to be 65,536 words by 4 bits. Memory expansion is easily accomplished using the active LOW chip enable (CE) input. An asynchronous output enable signal (OE) is provided to control the three-state data outputs. Pipelined RAMs are used in writable control store, DSP, data acquisition, and graphics applications where cycle time and throughput are the critical parameters. The CY7B158 can also be used in cache applications that utilize separate input and output buses.

### Read/Write Operation

The operation of these devices is completely synchronous with the exception of the OE signal. All data, address, and control signals are sampled on each LOW-to-HIGH transition of the clock. When the CE is LOW during this transition, the device is selected for operation. The type of operation is determined by the state of the WE signal during the same transition. WE LOW causes a write operation while WE HIGH causes a read operation. The data input and data output as well as the address register are also loaded on each

LOW-to-HIGH transition of the clock. The outputs, however, are not enabled for the address loaded on the current cycle. The state of the outputs are controlled by the pipelined CE and WE data from the previous cycle and the state of the OE signal. The data loaded into the output register is also from the previous cycle and is in phase with the output control information. This feature causes a single-cycle latency for the first read or write cycle, but allows a word of data to be read or written every 6 nanoseconds. The transparent write feature of the CY7B158 causes written data to pass through to the output register on the next cycle.

### Write-Through Operation

A third mode, called write-through, is possible when CE is HIGH and WE is LOW. It will pass the data from the input register to the output register without changing the memory array. The data can then be accessed from the outputs if OE is LOW. This feature provides an easy-to-use buffer between the input data bus and the output data bus.

