MILITARY 32K x 8 CMOS EPROM

FOR MAINTENANCE PURPOSES ONLY! NOT TO BE USED FOR NEW DESIGNS. SEE WS57C256F FOR NEW DESIGNS!

KEY FEATURES

- **Fast Access Time**
  - 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  - Latch-up Immunity Up to 200 mA
  - ESD Protection Exceeds 2000V
- **Standard EPROM Pinout**
- **Military Operating Range**

GENERAL DESCRIPTION

The WS27C256F is an extremely High Performance 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full military temperature operating range.

The WS27C256F was specifically designed to replace standard EPROMs in military environments. No hardware or software changes are required to replace standard military 27256 EPROMs with the WSI WS27C256F.

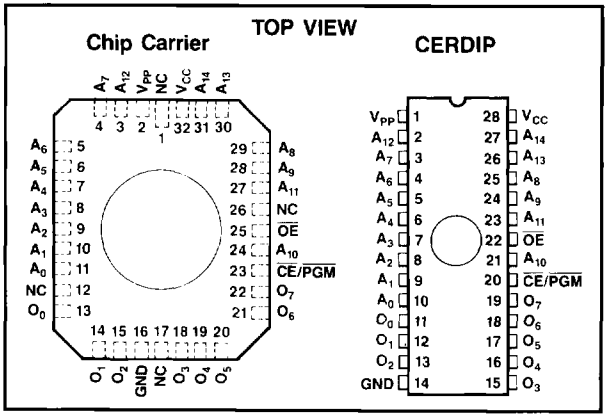
The WS27C256F is configured in the standard EPROM pinout which provides an easy upgrade path from the WS27C64F, and the 128K Bit WS27C128F.

MODE SELECTION

MODE \ PINS	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

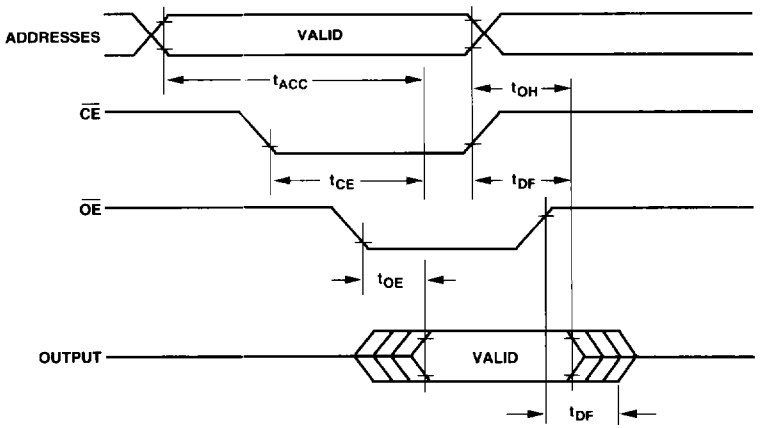
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ (Note 1)		500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$ (Note 2)		5	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		40	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		45	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C256F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

AC READ TIMING DIAGRAM



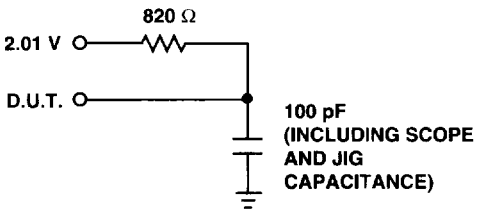
CAPACITANCE[5] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0 V	18	25	pF

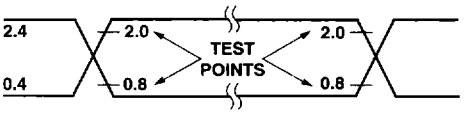
NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

5

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

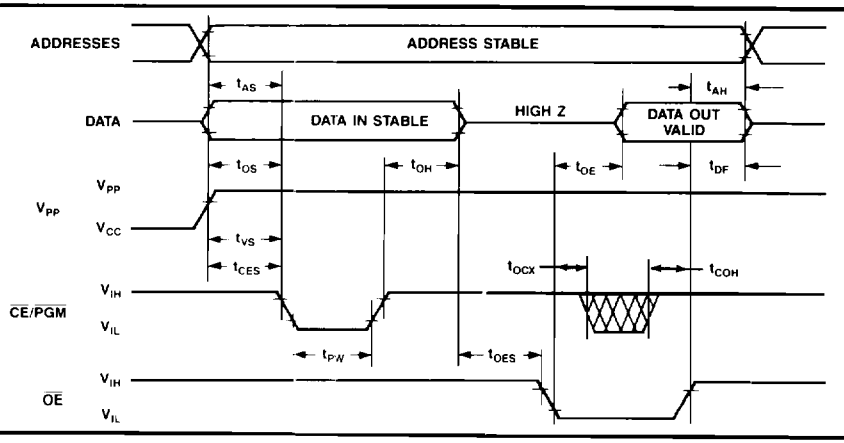
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ / $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

NOTES: 8. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
9. V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
10. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6 V ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{COH}	$\overline{CE}$ High to $\overline{OE}$ High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-90CMB*	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-90DMB*	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: 11. The actual part marking will not include the initials "WS."

*SMD product. See page 5-1 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 6-1

The WS27C256F is programmed using Algorithm B shown on page 6-5.

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