Signetics

74AC/ACT11323

8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

Objective Specification

ACL Products

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Additional Serial Inputs and outputs for expansion**
- **Four operating modes: Shift Left, Shift Right, Load, and Store**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11323 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11323 is an 8-bit universal shift/storage register with 3-State outputs. Its function is similar to the 74AC/ACT11299 with the exception of the synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to I/O_n	C_L = 50pF		7.5	9.0	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	232	232	pF
			Disabled	50	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_O	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	V_{IO} = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP to I/O_n	C_L = 50pF		140	65	MHz

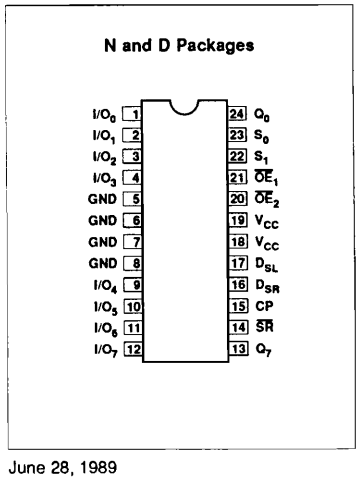
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

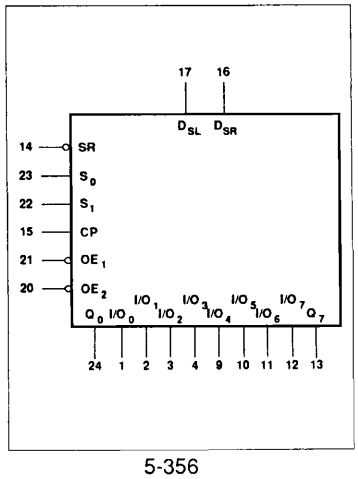
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11323N 74ACT11323N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11323D 74ACT11323D

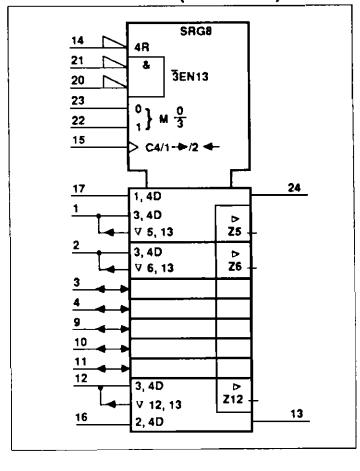
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



and outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. Four modes of operation are possible: hold (store), shift left, shift right, and load data.

The AC/ACT11323 contains eight edge-triggered D-type flip-flops and the inter-stage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{SR}$ overrides the Select inputs and resets the flip-flops on the next rising edge of CP. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A High signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-State buffers and puts the I/O pins in the high-impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	CP	Clock input
17	D_{SL}	Serial data input for left shift
16	D_{SR}	Serial data input for right shift
23, 22	S_0, S_1	Mode select inputs
14	$\overline{SR}$	Synchronous master reset input (active-Low)
21, 20	$\overline{OE}_1$, $\overline{OE}_2$	Output enable inputs (active-Low)
1, 2, 3, 4, 9, 10, 11, 12	I/O_0 -I/O_7	Data inputs/outputs
24, 13	Q_0, Q_7	Serial outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

MODE SELECT TABLE

INPUTS					OPERATING MODE
$\overline{SR}$	$\overline{OE}_n$	S_0	S_1	CP	
L	L	X	X	↑	Synchronous Reset; Q_0 - Q_7 = Low
H	L	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	L	H	↑	Shift Right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	L	H	L	↑	Shift Left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	L	X	Hold
X	H	X	X	X	Outputs Disabled

H = High voltage levle
L = Low voltage levels
X = Don't Care
↑ = Low-to-High clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11323			74ACT11323			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11323				74ACT11323				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.